

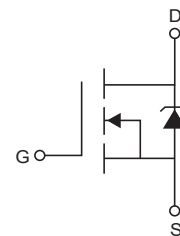
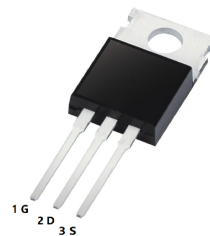
1.Features

- $V_{DS(V)}=100V$
- $I_D=120A$
- $R_{DS(ON)}<4.8m\Omega(V_{GS}=10V)$
- Improved Gate, Avalanche and Dynamic dv/dt Ruggedness
- Fully Characterized Capacitance and Avalanche SOA
- Enhanced body diode dV/dt and dI/dt Capability Lead Free
- Halogen-Free

2.Pinning information

Pin	Symbol	Description
1	G	GATE
2	D	DRAIN
3	S	SOURCE

TO-220



3.Absolute Maximum Ratings

Parameter		Symbol	Rating	Units
Continuous Drain Current, $V_{GS}=10V$ (Silicon Limited)	$T_C=25^{\circ}C$	I_D	127 ①	A
Continuous Drain Current, $V_{GS}=10V$ (Silicon Limited)	$T_C=100^{\circ}C$		90 ①	A
Continuous Drain Current, $V_{GS}=10V$ (Wire Bond Limited)	$T_C=25^{\circ}C$		120	A
Pulsed Drain Current ②		I_{DM}	560	A
Maximum Power Dissipation	$T_C=25^{\circ}C$	P_D	250	W
Linear Derating Factor			1.7	W/ $^{\circ}C$
Gate-to-Source Voltage		V_{GS}	± 20	V
Peak Diode Recovery ④		dv/dt	18	V/ns
Storage Temperature Range		T_J, T_{STG}	-55 to 175	$^{\circ}C$
Soldering Temperature, for 10 seconds (1.6mm from case)			300	$^{\circ}C$
Mounting torque, 6-32 or M3 screw			10lbin (1.1Nm)	



Single Pulse Avalanche Energy ③	$E_{AS(Thermally\ limited)}$	130	mJ
Avalanche Current ①	I_{AR}	See Fig. 18, 20	A
Repetitive Avalanche Energy ⑤	E_{AR}	22a, 22b	mJ

4. Thermal resistance rating

Parameter	Symbol	Typ	Max	Units
Junction-to-Case ⑧	$R_{\theta JC}$		0.6	°C/W
Case-to-Sink, Flat Greased Surface	$R_{\theta CS}$	0.5		°C/W
Junction-to-Ambient ⑧⑨	$R_{\theta JA}$		62	°C/W



5. Electrical Characteristics @ $T_J = 25^\circ\text{C}$ (unless otherwise specified)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Drain-to-Source Breakdown Voltage	$V_{(BR)DSS}$	$I_D=250\mu\text{A}$, $V_{GS}=0\text{V}$	100			V
Breakdown Voltage Temp. Coefficient	$\Delta V_{(BR)DSS}/\Delta T_J$	$I_D=5\text{mA}$, Reference to 25°C ②		0.11		V/ $^\circ\text{C}$
Static Drain-to-Source On-Resistance	$R_{DS(ON)}$	$V_{GS}=10\text{V}$, $I_D=75\text{A}$ ⑤		4.8	6	m Ω
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS}=V_{GS}$, $I_D=150\mu\text{A}$	2		4	V
Drain-to-Source Leakage Current	I_{DSS}	$V_{DS}=100\text{V}$, $V_{GS}=0\text{V}$			20	μA
		$V_{DS}=80\text{V}$, $V_{GS}=0\text{V}$, $T_J=125^\circ\text{C}$			250	μA
Gate-to-Source Forward Leakage	I_{GSS}	$V_{GS}=20\text{V}$			100	nA
Gate-to-Source Reverse Leakage		$V_{GS}=-20\text{V}$			-100	nA
Internal Gate Resistance	R_g			0.7		Ω
Forward Transconductance	g_{FS}	$V_{DS}=50\text{V}$, $I_D=75\text{A}$	150			S
Total Gate Charge	Q_g	$I_D=75\text{A}$, $V_{DS}=50\text{V}$ $V_{GS}=10\text{V}$ ⑤		120	170	nC
Gate-to-Source Charge	Q_{gs}			29		nC
Gate-to-Drain ("Miller") Charge	Q_{gd}			35		nC
Total Gate Charge Sync. (Q_g-Q_{gd})	Q_{sync}	$I_D=75\text{A}$, $V_{DS}=0\text{V}$, $V_{GS}=10\text{V}$		85		nC
Turn-On Delay Time	$t_{D(on)}$	$V_{DD}=65\text{V}$, $I_D=75\text{A}$ $R_G=2.7\Omega$, $V_{GS}=10\text{V}$ ⑤		20		ns
Rise Time	t_r			60		ns
Turn-Off Delay Time	$t_{D(off)}$			55		ns
Fall Time	t_f			57		ns
Input Capacitance	C_{iss}	$V_{GS}=0\text{V}$, $V_{DS}=50\text{V}$ See Fig. 5, $f=1\text{MHz}$		6860		pF
Output Capacitance	C_{oss}			490		pF
Reverse Transfer Capacitance	C_{rss}			220		pF
Effective Output Capacitance (Energy Related)	$C_{oss\text{eff.}(ER)}$	$V_{GS}=0\text{V}$, $V_{DS}=0\text{V}$ to 80V ⑦ See Fig. 11		570		pF
Effective Output Capacitance (Time Related)	$C_{oss\text{eff.}(TR)}$	$V_{GS}=0\text{V}$, $V_{DS}=0\text{V}$ to 80V ⑥		920		pF



Diode Characteristics						
Continuous Source Current (Body Diode)	I_S	MOSFET symbol showing the integral reverse p-n junction diode.			127 ^①	A
Pulsed Source Current (Body Diode) ^②	I_{SM}				560	A
Diode Forward Voltage	V_{SD}	$T_J=25^\circ\text{C}, I_S=75\text{A}, V_{GS}=0\text{V}$ ^⑤			1.3	V
Reverse Recovery Time	t_{rr}	$T_J=25^\circ\text{C}, V_R=85\text{V}$		40		ns
		$T_J=125^\circ\text{C}, I_F=75\text{A}$	49			ns
Reverse Recovery Charge	Q_{rr}	$T_J=25^\circ\text{C}, di/dt=100\text{A}/\mu\text{s}$ ^⑤		58		nC
		$T_J=125^\circ\text{C}$		89		nC
Reverse Recovery Current	I_{RRM}	$T_J=25^\circ\text{C}$		2.5		A
Forward Turn-On Time	t_{on}	Intrinsic turn-on time is negligible (turn-on is dominated by L_S+L_D)				

Notes:

- ① Calculated continuous current based on maximum allowable junction temperature. Bond wire current limit is 120A. Note that current limitations arising from heating of the device leads may occur with some lead mounting arrangements.
- ② Repetitive rating; pulse width limited by max. junction temperature.
- ③ Limited by T_{Jmax} , starting $T_J=25^\circ\text{C}$, $L=0.047\text{mH}$, $R_G=25\Omega$, $I_{AS}=75\text{A}$, $V_{GS}=10\text{V}$. Part not recommended for use above the Eas value and test conditions.
- ④ $I_{SD} \leq 75\text{A}$, $di/dt \leq 600\text{A}/\mu\text{s}$, $V_{DD} \leq V_{(BR)DSS}$, $T_J \leq 175^\circ\text{C}$.
- ⑤ Pulse width $\leq 400\mu\text{s}$; duty cycle $\leq 2\%$.
- ⑥ C_{oss} eff. (TR) is a fixed capacitance that gives the same charging time as C_{oss} while V_{DS} is rising from 0 to 80% V_{DSS} .
- ⑦ C_{oss} eff. (ER) is a fixed capacitance that gives the same energy as C_{oss} while V_{DS} is rising from 0 to 80% V_{DSS} .
- ⑧ R_θ is measured at T_J approximately 90°C .



6.1 Typical Characteristics

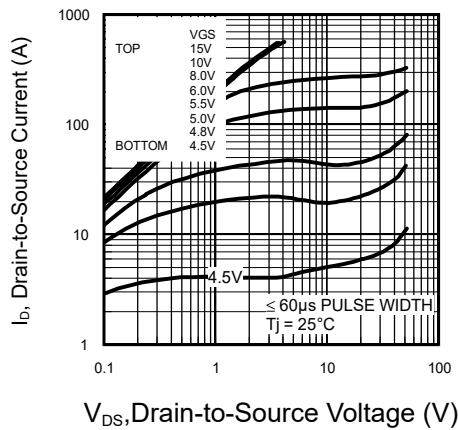


Figure 1: Typical On-Resistance vs. Gate Voltage

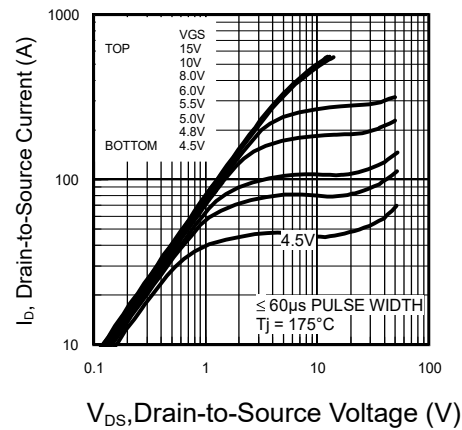


Figure 2: Typical Output Characteristics

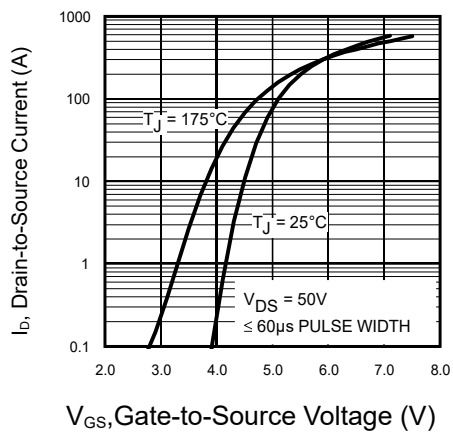


Figure 3: Typical Output Characteristics

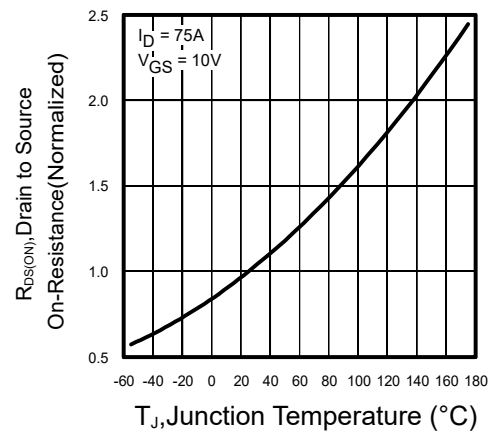


Figure 4: Normalized On-Resistance vs. Temperature

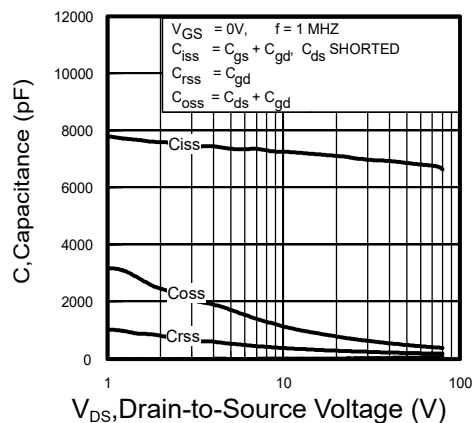


Figure 5: Typical Capacitance vs. Drain-to-Source Voltage

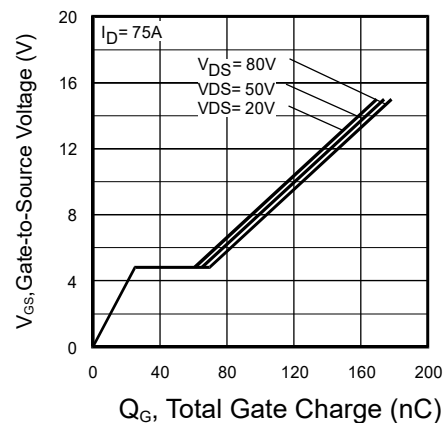


Figure 6: Typical Gate Charge vs.



6.2 Typical Characteristics

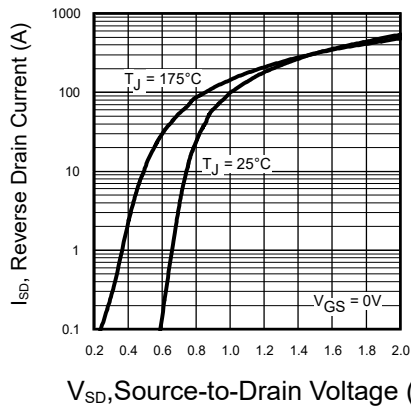


Figure 7: Typical Capacitance vs. Drain-to-Source Voltage

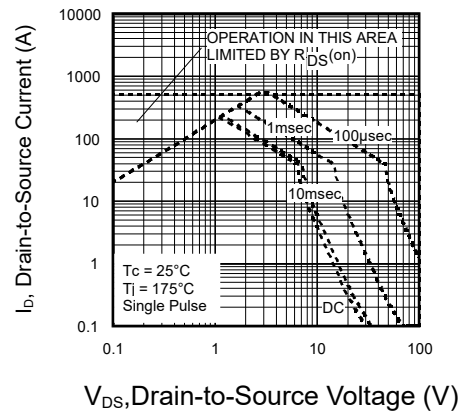


Figure 8: Maximum Safe Operating Area

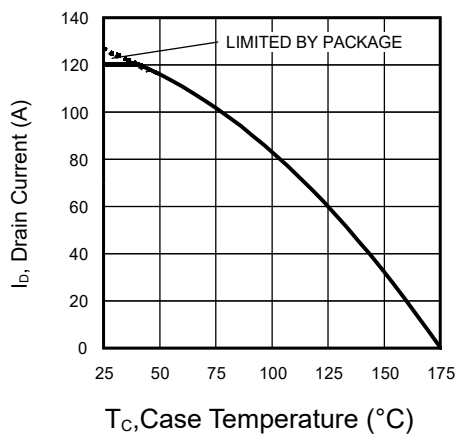


Figure 9: Maximum Drain Current vs. Case Temperature

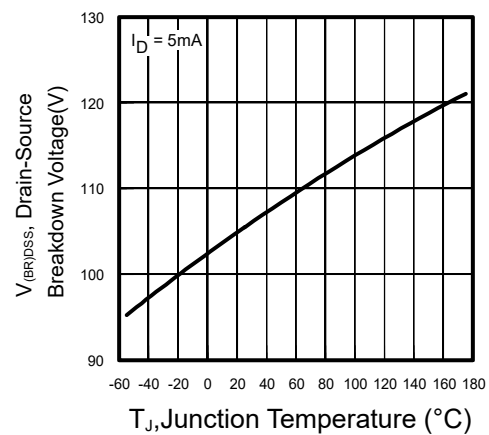


Figure 10: Drain-to-Source Breakdown Voltage

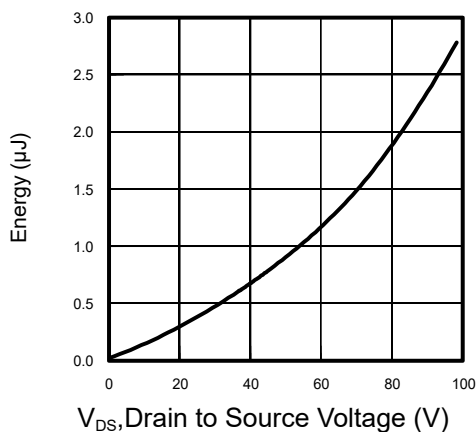


Figure 11: Typical C_{OSS} Stored Energy

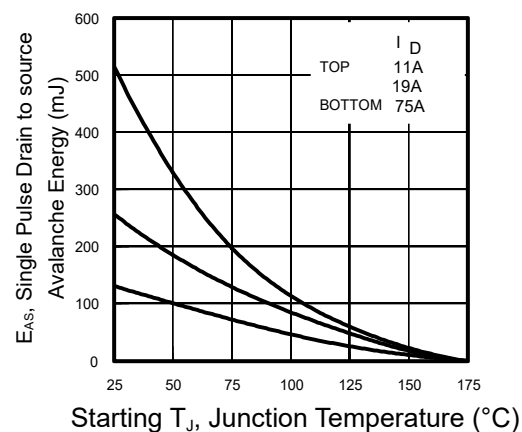


Figure 12: Maximum Avalanche Energy vs. DrainCurrent



6.3 Typical Characteristics

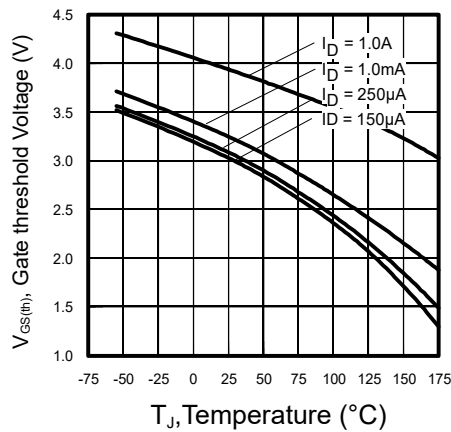


Figure 13: Threshold Voltage vs. Temperature

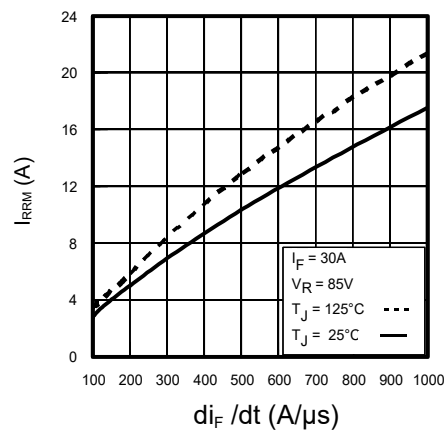


Figure 14: Typical Recovery Current vs. di/dt

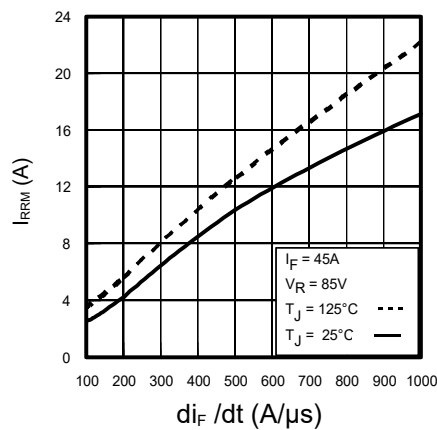


Figure 15: Typical Recovery Current vs. di/dt

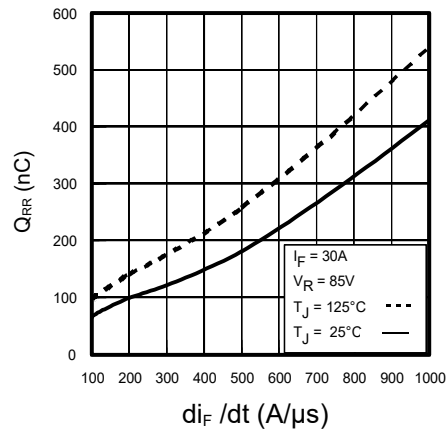


Figure 16: Typical Stored Charge vs. di/dt

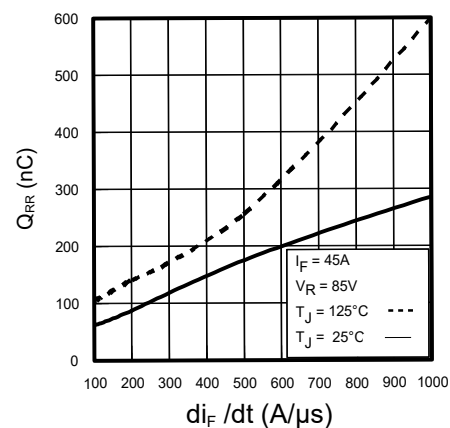


Figure 17: Typical Stored Charge vs. di/dt

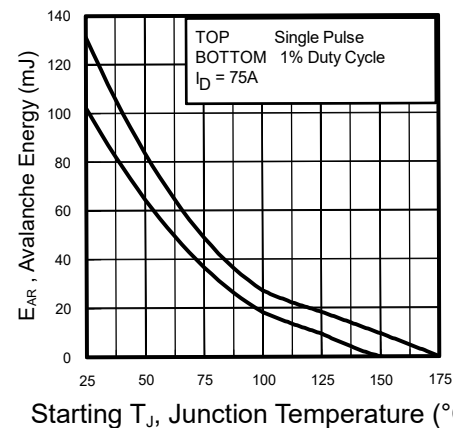


Figure 18: Maximum Avalanche Energy vs. Temperature



6.4Typical Characterisitics

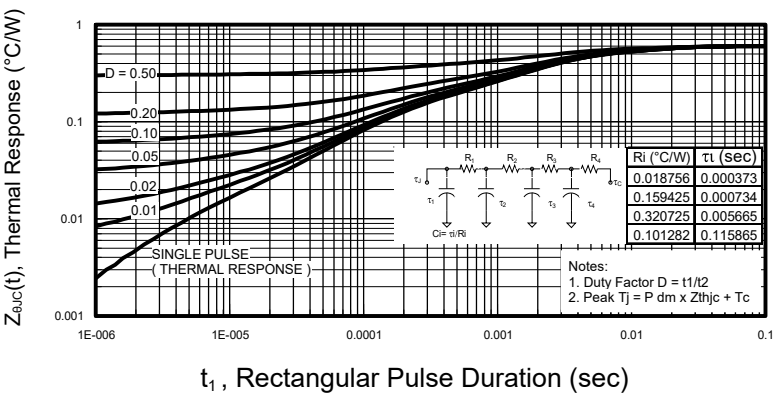


Figure 19: Maximum Effective Transient Thermal Impedance, Junction-to-Case

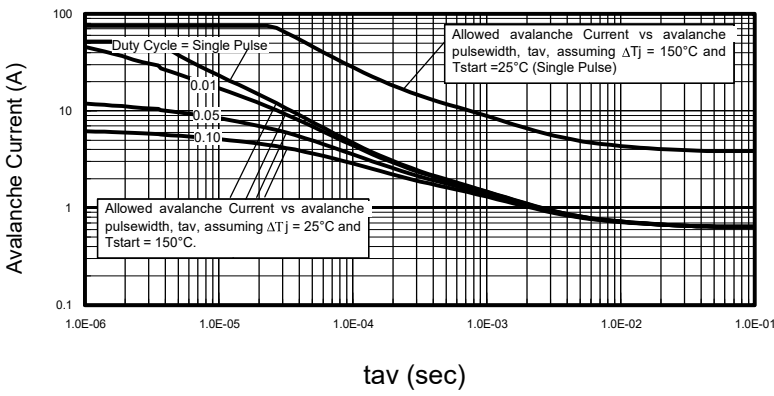


Figure 20: Typical Avalanche Current vs.Pulse width

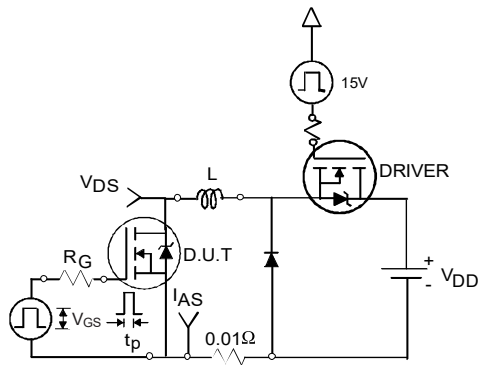


Figure 21a: Unclamped Inductive Test Circuit

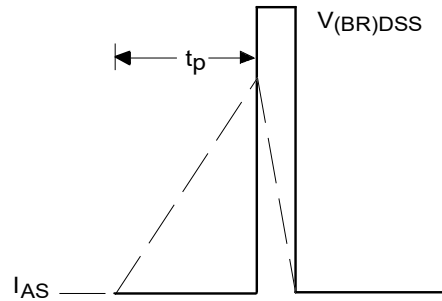


Figure 21b: Unclamped Inductive Waveforms

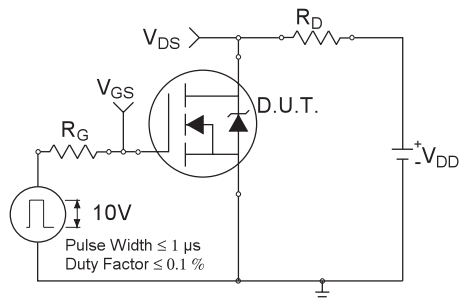


Figure 22a: Switching Time Test Circuit

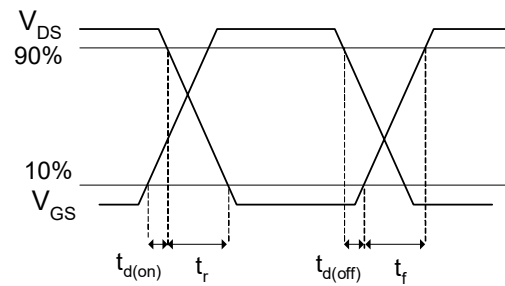


Figure 22b: Switching Time Waveforms

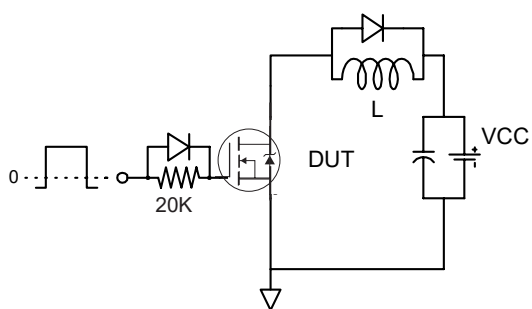


Figure 23a: Gate Charge Test Circuit

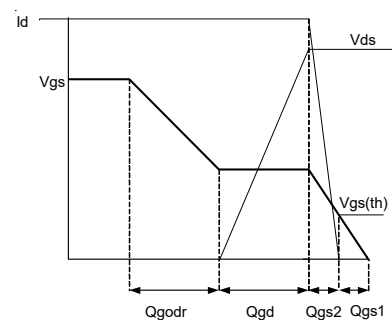


Figure 23b: Gate Charge Waveform



Notes on Repetitive Avalanche Curves , Figures 18, 20:

1. Avalanche failures assumption: Purely a thermal phenomenon and failure occurs at a temperature far in excess of T_{jmax} .

This is validated for every part type.

2. Safe operation in Avalanche is allowed as long as T_{jmax} is not exceeded.

3. Equation below based on circuit and waveforms shown in Figures 23a, 23b.

4. $P_{D(ave)}$ = Average power dissipation per single avalanche pulse.

5. BV = Rated breakdown voltage (1.3 factor accounts for voltage increase during avalanche).

6. I_{av} = Allowable avalanche current.

7. ΔT = Allowable rise in junction temperature, not to exceed T_{jmax} (assumed as 25°C in Figure 18, 20).

t_{av} = Average time in avalanche.

D = Duty cycle in avalanche = $t_{av} \cdot f$

$Z_{thJC}(D, t_{av})$ = Transient thermal resistance, see Figure 19)

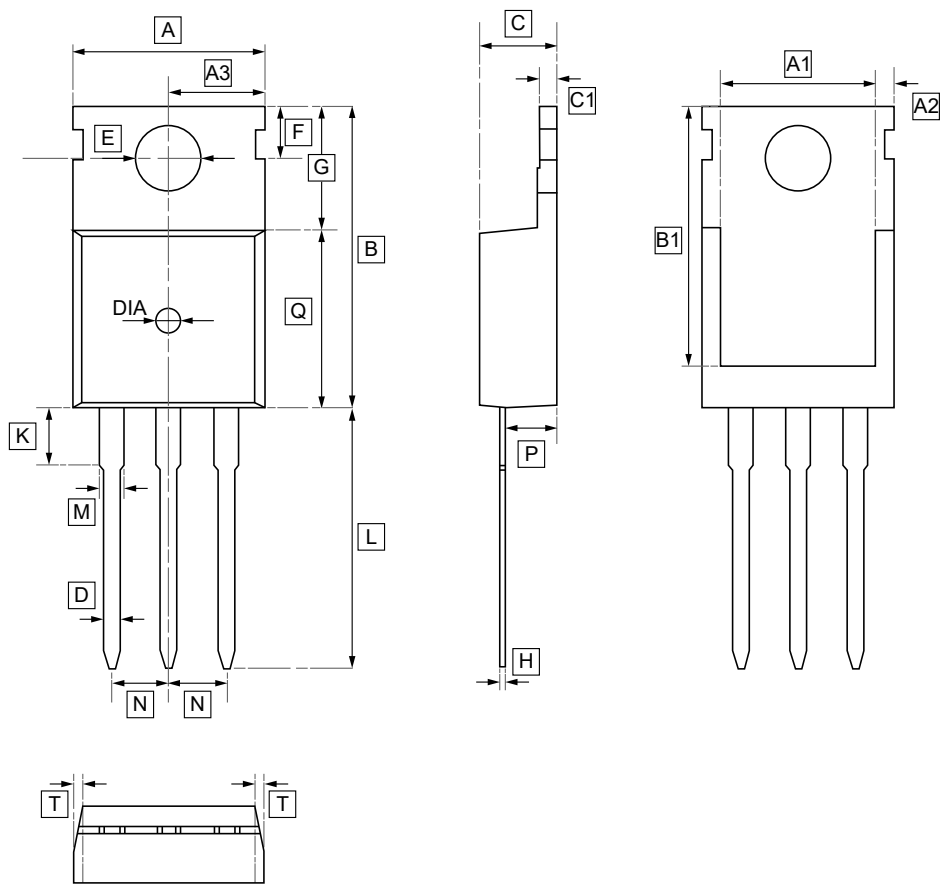
$P_{D(ave)} = 1/2 (1.3 \cdot BV \cdot I_{av}) = \Delta T / Z_{thJC}$

$I_{av} = 2\Delta T / [1.3 \cdot BV \cdot Z_{th}]$

$E_{AS(AR)} = P_{D(ave)} \cdot t_{av}$



8.1 TO-220 Package Outline Dimensions



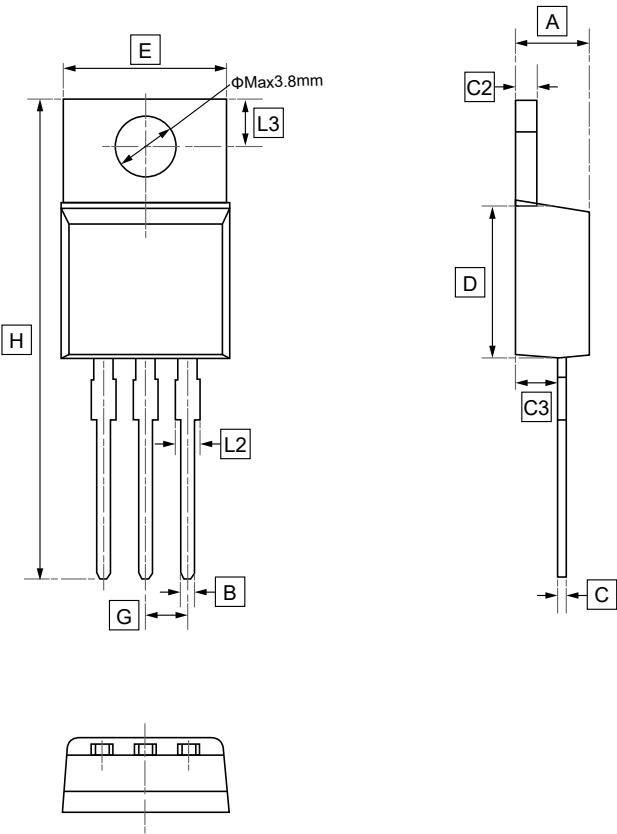
DIMENSIONS (mm are the original dimensions)

Symbol	A	A1	A2	A3	B	B1	C	C1	D	E	F	G
Min	9.7	8.44	1.05	4.8	15.4	12.9	4.28	1.1	0.6	3.4	2.65	5.2
Max	10.3	8.84	1.25	5.2	16.2	13.5	4.68	1.5	1.0	3.8	3.25	5.8

Symbol	H	K	L	L1	M	N	P	Q	T	DIA
Min	0.4	2.9	12.8	2.7	1.15	2.49	2.1	8.7	W:0.35	⌀1.5
Max	0.6	3.3	13.6	3.3	1.35	2.59	2.7	9.3		(deep 0.2)



8.2 TO-220 Package Outline Dimensions

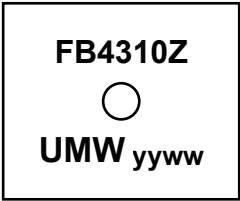


DIMENSIONS (mm are the original dimensions)

Symbol	A	B	C	C2	C3	D	E	G	H	L2	L3
Min	4.30	0.60	0.28	1.17	2.30	8.80	9.80	2.44	28.55	1.10	2.59
Max	4.70	1.00	0.48	1.37	2.70	9.20	10.20	2.64	29.15	1.50	2.89



8.Ordering information



yy: Year Code
ww: Week Code

Order Code	Package	Base QTY	Delivery Mode
UMW IRFB4310Z	TO-220	1000	Tube and box



9.Disclaimer

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