OPA2376AIDR-HX/OPA2376AIDGKR-HX Low-Noise, Low Quiescent Current, Precision Operational Amplifier

Description

The OPA2376AIDR-HX/OPA2376AIDGKR-HX family represents a new generation of low-noise operational amplifiers featuring e-trim™ technology, which delivers exceptional DC precision and AC performance. With rail-to-rail input and output capabilities, a low offset voltage (maximum 25 µV), minimal noise (7.5 nV/√Hz), and a maximum quiescent current of 950 µA, this series is highly appealing for various precision and portable applications. Furthermore, the device boasts a reasonably wide supply range with excellent power supply rejection ratio (PSRR), making it suitable for applications that operate directly from batteries without the need for regulation.

The OPA2376AIDR-HX/OPA2376AIDGKR-HX is offered in the 2 Applications SOIC-8, and VSSOP-8 packages. All versions are specified for operation from –40°C to +125°C

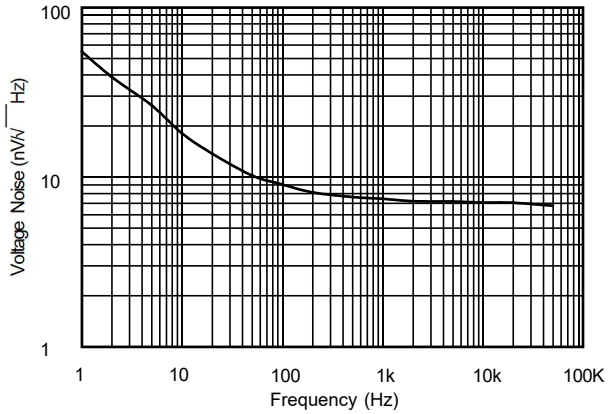
Features

- Low Noise: 7.5 nV/√Hz at 1 kHz
- 0.1 Hz to 10 Hz Noise: 0.8 µVPP
- Quiescent Current: 760 µA (typical)
- Low Offset Voltage: 5 µV (typ)
- Gain Bandwidth Product: 5.5 MHz Rail-to-Rail Input and Output
- Single-Supply Operation
- Supply Voltage: 2.2 V to 5.5 V Space-Saving
- Packages: VSSOP, SOIC

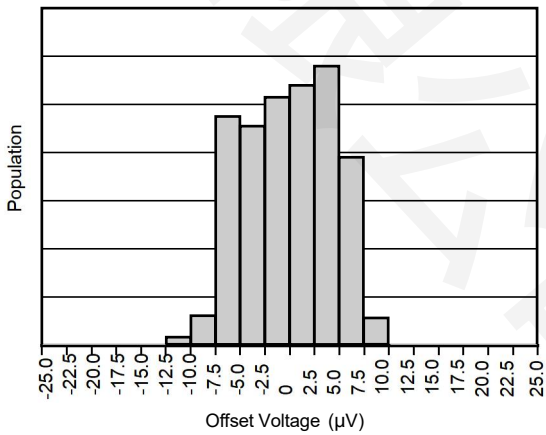
Applications

- ADC Buffer
- Audio Equipment
- Medical Instrumentation
- Handheld Test Equipment
- Active Filtering
- Sensor Signal Conditioning

Input Noise Voltage Spectral Density

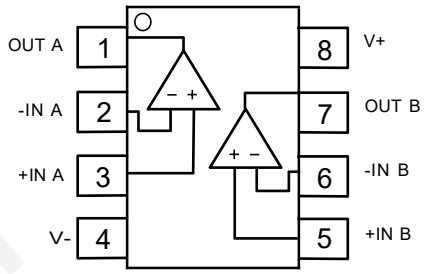


Offset Voltage Production Distribution



Pin Configuration and Functions

8-Pin SOIC and 8-Pin VSSOP



Top View

OPA2376AIDR-HX(SOIC) /OPA2376AIDGKR-HX(VSSOP)

NAME	PIN	I/O	DESCRIPTION
+IN A	3	I	Input signal A^+
–IN A	2	I	Input signal $A^–$
+IN B	5	I	Input signal B^+
–IN B	6	I	Input signal $B^–$
OUT A	1	O	Output signal A
OUT B	7	O	Output signal B
V^+	8	__	Supply voltage$^+$
$V^–$	4	__	Supply voltage$^–$

Specifications

1.Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
Voltage	Supply, V_S = (V^+) (V)		7	V
	Signal input pin(2)	(V) 0.5	(V^+) + 0.5	V
Current	Signal input pin(2)	10	10	mA
	Output short-circuit (3)		Continuous	
Temperature	Operating range, T_A	40	150	°C
	Junction, T_J		150	
	Storage, T_{stg}	65	150	

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) Input terminals are diode-clamped to the power-supply rails. Input signals that can swing more than 0.5 V beyond the supply rails should be current limited to 10 mA or less.
(3) Short-circuit to ground, one amplifier per package.

2.ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins(1)	±4000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins(2)	±1000	
		Machine model	±200	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

3.Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
(V^+) (V)	Supply voltage	2.2 (±1.1)		5.5 (±2.75)	V
T_A	Operating temperature	40		150	℃

4.Thermal Information: OPA2376AIDR-HX/OPA2376AIDGKR-HX

THERMAL METRIC		OPA2376AIDR-HX/OPA2376AIDGKR-HX		UNIT
		SOIC	VSSOP	
		8 PINS	8 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	111.1	171.2	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	54.7	63.9	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	51.7	92.8	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	10.5	9.2	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	51.2	91.2	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	n/a	n/a	°C/W

5.Electrical Characteristics

At T_A = 25°C, R_L = 10 kΩ connected to V_S / 2, V_{CM} = V_S / 2, and V_{OUT} = V_S / 2, unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
OFFSET VOLTAGE						
V_{OS}	Input offset voltage			5	25	μV
dV_{OS}/dT	Input offset voltage versus temperature	T_A = –40°C to +85°C		0.26	1	μV/°C
		T_A = –40°C to +125°C		0.32	2	μV/°C
PSRR	Input offset voltage versus power supply	T_A = 25°C, V_S = 2.2 V to 5.5 V, V_{CM} < (V^+) – 1.3 V		5	20	μV/V
		T_A = –40°C to +125°C, V_S = 2.2 V to 5.5 V, V_{CM} < (V^+) – 1.3 V		5		μV/V
	Channel separation, dc (dual, quad)			0.5		mV/V
INPUT BIAS CURRENT						
I_B	Input bias current	T_A = 25°C		0.2	10	pA
		T_A = –40°C to +125°C		See *Typical Characteristics*		pA
I_{OS}	Input offset current			0.2	10	pA
NOISE						
	Input voltage noise	f = 0.1 Hz to 10 Hz		0.8		μV_{PP}
e_n	Input voltage noise density	f = 1 kHz		7.5		$nV/\sqrt{Hz}$
i_n	Input current noise	f = 1 kHz		2		$fA/\sqrt{Hz}$
INPUT VOLTAGE RANGE						
V_{CM}	Common-mode voltage range		(V^-) – 0.1		(V^+) + 0.1	V
CMRR	Common-mode rejection ratio	(V^-) < V_{CM} < (V^+) – 1.3 V	76	90		dB
INPUT CAPACITANCE						
	Differential			6.5		pF
	Common-mode			13		pF
OPEN-LOOP GAIN						
A_{OL}	Open-loop voltage gain	50 mV < V_O < (V^+) – 50 mV, R_L = 10 kΩ	120	134		dB
		100 mV < V_O < (V^+) – 100 mV, R_L = 2 kΩ	120	126		dB
FREQUENCY RESPONSE C_L = 100 pF, V_S = 5.5 V						
GBW	Gain-bandwidth product			5.5		MHz
SR	Slew rate	G = 1		2		V/μs
t_S	Settling time	To 0.1%, 2-V step , G = 1		1.6		μs
		To 0.01%, 2-V step , G = 1		2		μs
	Overload recovery time	V_{IN} × gain > V_S		0.33		μs
THD+N	Total harmonic distortion + noise	V_O = 1 V_{RMS}, G = 1, f = 1 kHz, R_L = 10 kΩ		0.00027%		

Electrical Characteristics (continued)

At T_A = 25°C, R_L = 10 kΩ connected to V_S / 2, V_{CM} = V_S / 2, and V_{OUT} = V_S / 2, unless otherwise noted.

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
OUTPUT							
Voltage output swing from rail		T_A = 25°C, R_L = 10 kΩ	VSSOP-8 packages only		10	20	mV
		T_A = –40°C to +125°C, R_L = 10 kΩ				40	mV
		T_A = 25°C, R_L = 2 kΩ	VSSOP-8 packages only		40	50	mV
		T_A = –40°C to +125°C, R_L = 2 kΩ				80	mV
I_{SC}	Short-circuit current				+30, –50		mA
C_{LOAD}	Capacitive load drive				See *Typical Characteristics*		
R_O	Open-loop output impedance				150		Ω
POWER SUPPLY							
V_S	Specified voltage range			2.2		5.5	V
	Operating voltage range				2 to 5.5		V
I_Q	Quiescent current per amplifier	T_A = 25°C, I_O = 0, V_S = 5.5 V, V_{CM} < (V^+) – 1.3 V			760	950	µA
		T_A = –40°C to +125°C				1	mA
TEMPERATURE							
	Specified range			–40		125	°C
	Operating range			–40		150	°C

6.Typical Characteristics

At T_A = 25°C, V_S = 5 V, R_L = 10 kΩ connected to V_S / 2, V_{CM} = V_S / 2, and V_{OUT} = V_S / 2, unless otherwise noted.

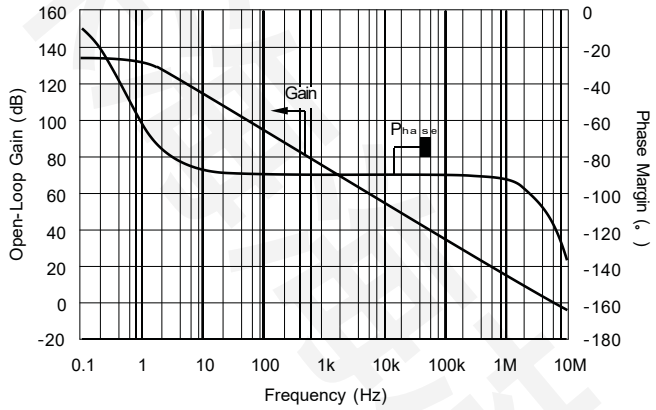


Figure 1. Open-Loop Gain and Phase vs Frequency

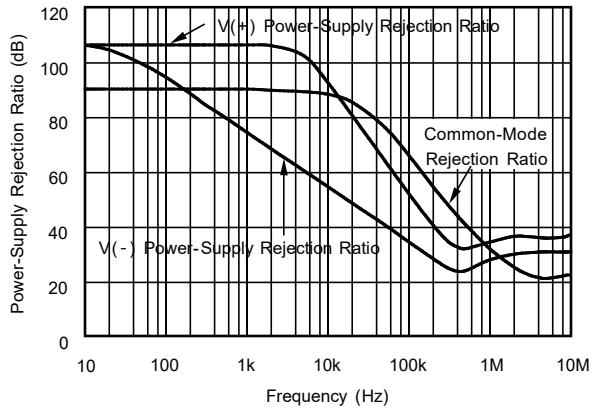


Figure 2. Power-Supply and Common-Mode Rejection Ratio vs Frequency

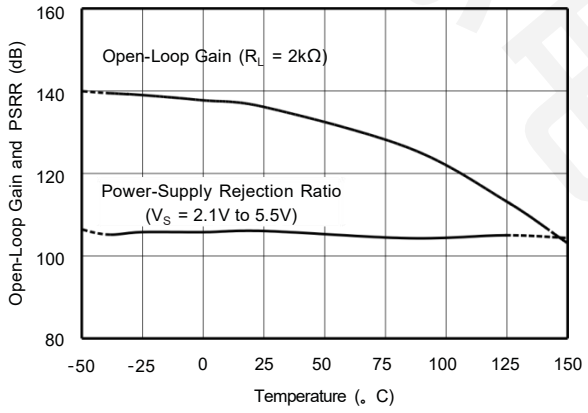


Figure 3. Open-Loop Gain and Power-Supply Rejection Ratio vs Temperature

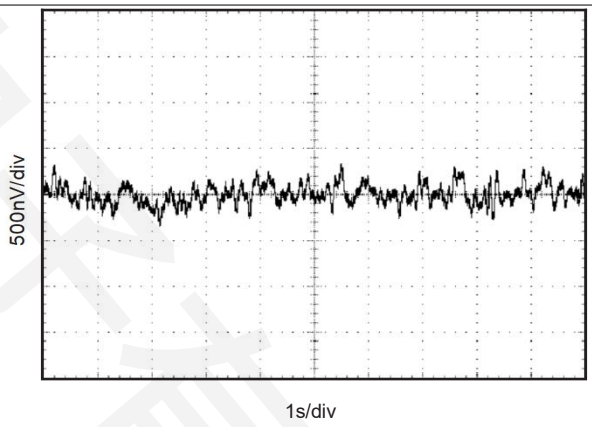


Figure 4. 0.1-Hz to 10-Hz Input Voltage Noise

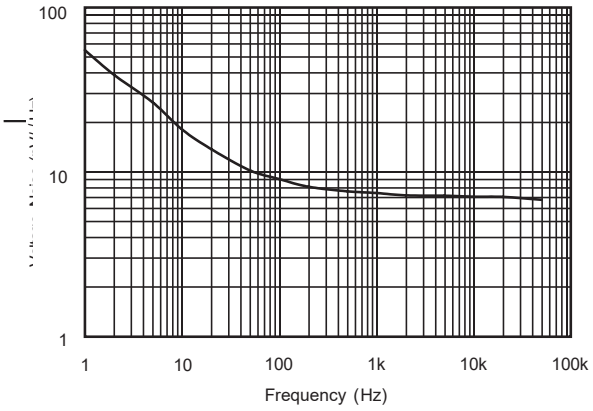


Figure 5. Input Voltage Noise Spectral Density

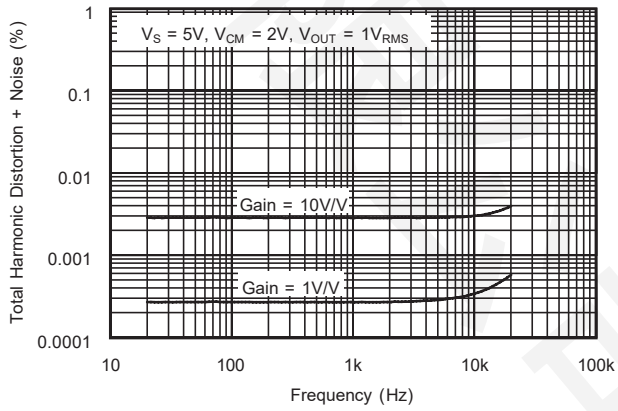


Figure 6. Total Harmonic Distortion + Noise vs Frequency

Typical Characteristics (continued)

At T_A = 25°C, V_S = 5 V, R_L = 10 kΩ connected to V_S / 2, V_{CM} = V_S / 2, and V_{OUT} = V_S / 2, unless otherwise noted.

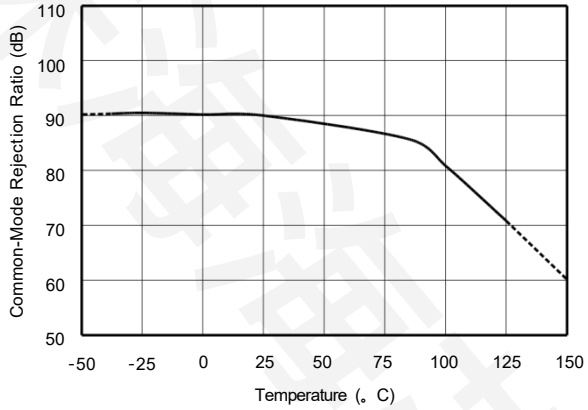


Figure 7. Common-Mode Rejection Ratio vs Temperature

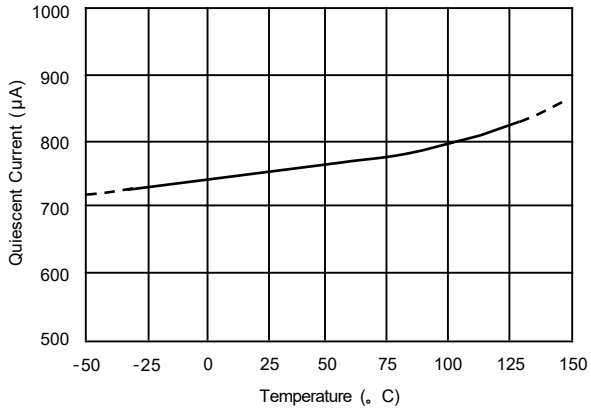


Figure 8. Quiescent Current vs Temperature

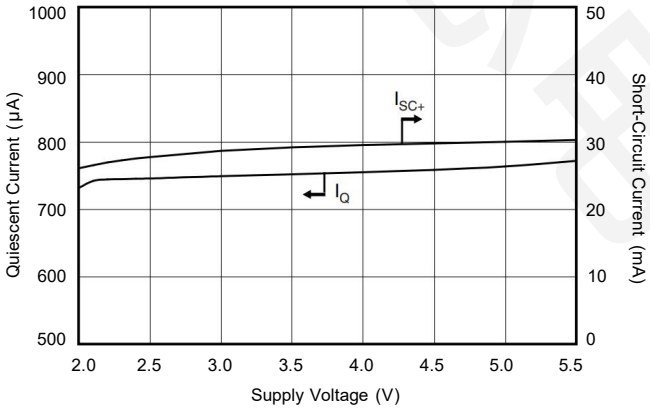


Figure 9. Quiescent and Short-Circuit Current vs Supply Voltage

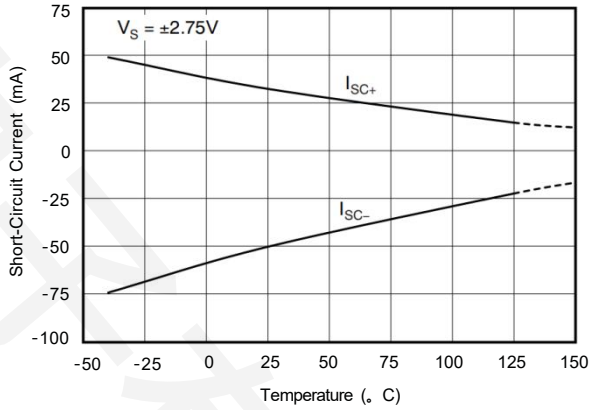


Figure 10. Short-Circuit Current vs Temperature

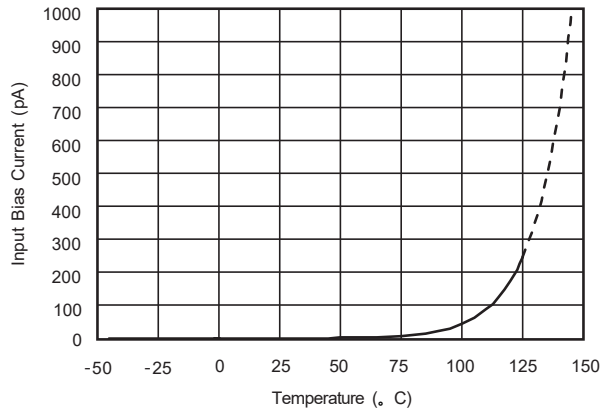


Figure 11. Input Bias Current vs Temperature

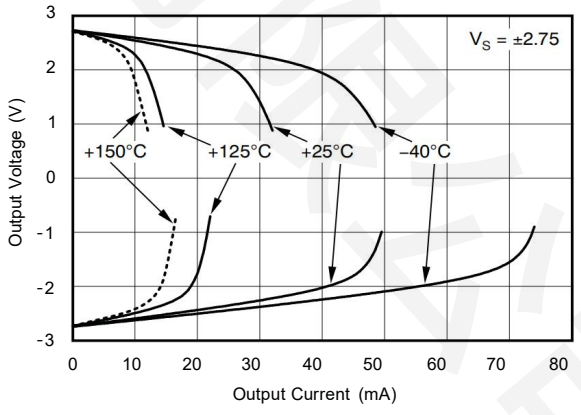


Figure 12. Output Voltage vs Output Current

Typical Characteristics (continued)

At T_A = 25°C, V_S = 5 V, R_L = 10 kΩ connected to V_S / 2, V_{CM} = V_S / 2, and V_{OUT} = V_S / 2, unless otherwise noted.

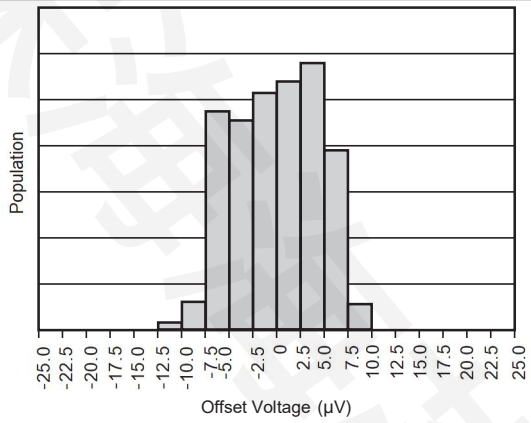


Figure 13. Offset Voltage Production Distribution

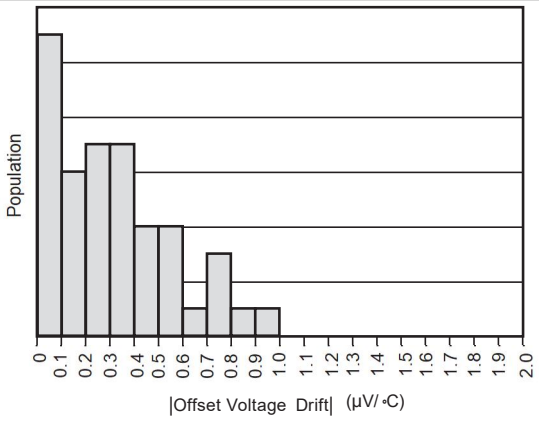


Figure 14. Offset Voltage Drift Production Distribution (–40°C to 125°C)

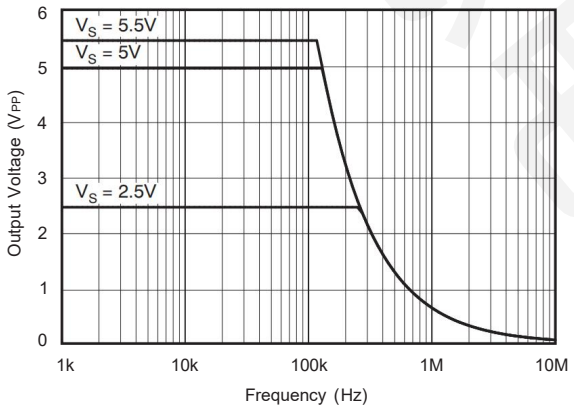


Figure 15. Maximum Output Voltage vs Frequency

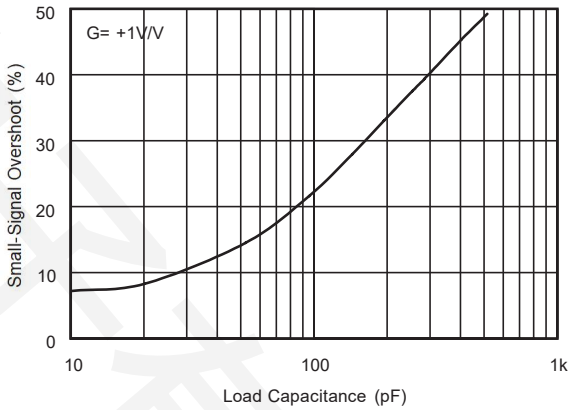


Figure 16. Small-Signal Overshoot vs Load Capacitance

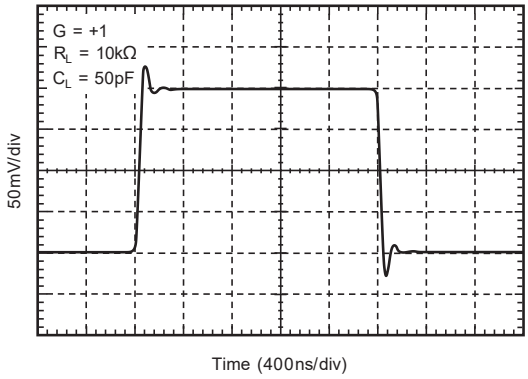


Figure 17. Small-Signal Pulse Response

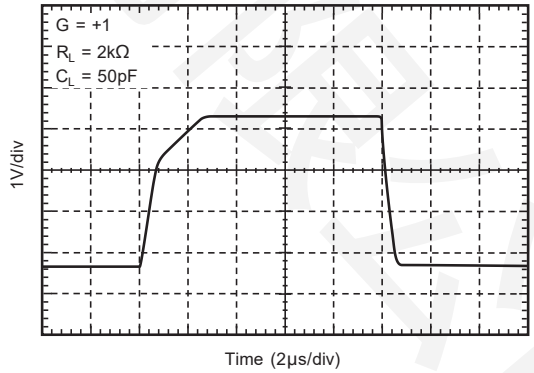


Figure 18. Large-Signal Pulse Response

Typical Characteristics (continued)

At T_A = 25°C, V_S = 5 V, R_L = 10 kΩ connected to V_S / 2, V_{CM} = V_S / 2, and V_{OUT} = V_S / 2, unless otherwise noted.

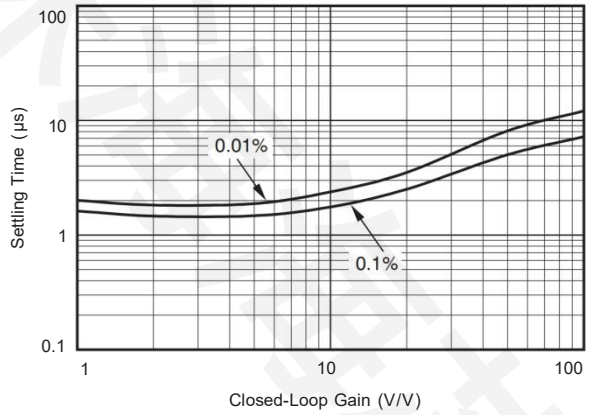


Figure 19. Settling Time vs Closed-Loop Gain

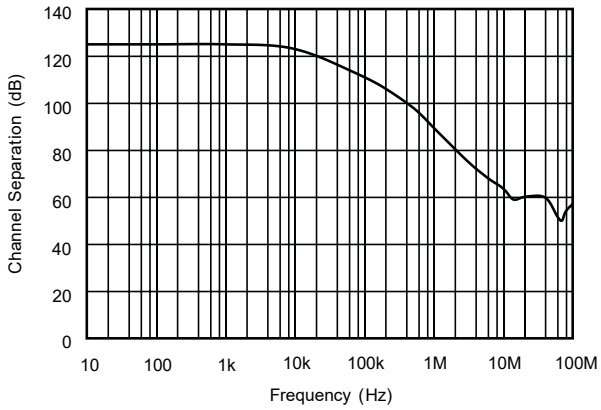


Figure 20. Channel Separation vs Frequency

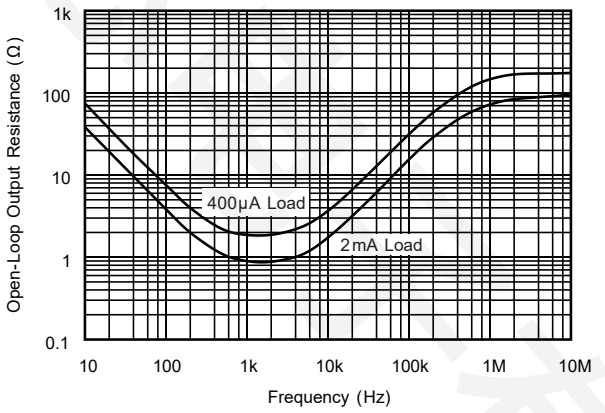


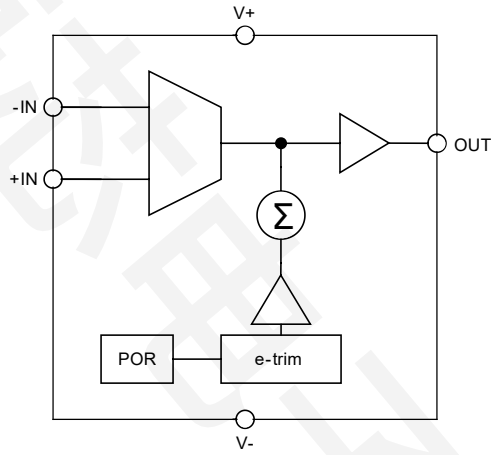
Figure 21. Open-Loop Output Resistance vs Frequency

Detailed Description

1.Overview

The OPA2376AIDR-HX/OPA2376AIDGKR-HX family belongs to a new generation of low-noise operational amplifiers with *e-trim*, giving customers outstanding dc precision and ac performance. Low noise, rail-to-rail input and output, and low offset, drawing a low quiescent current, make these devices ideal for a variety of precision and portable applications. In addition, this device has a wide supply range with excellent PSRR, making it a suitable option for applications that are battery-powered without regulation.

2.Functional Block Diagram



3.Feature Description

The OPA2376AIDR-HX/OPA2376AIDGKR-HX family of precision amplifiers offers excellent dc performance as well as excellent ac performance. Operating from a single power-supply the OPA2376AIDR-HX/OPA2376AIDGKR-HX is capable of driving large capacitive loads, has a wide input common-mode voltage range, and is well-suited to drive the inputs of SAR ADCs as well as 24-bit and higher resolution converters. Including internal ESD protection, the OPA2376AIDR-HX/OPA2376AIDGKR-HX family is offered in a variety of industry- standard packages, including a wafer chip-scale package for applications that require space savings.

3.1.Operating Voltage

The OPA2376AIDR-HX/OPA2376AIDGKR-HX family of amplifiers operates over a power-supply range of 2.2 V to 5.5 V (±1.1 V to ±2.75 V). Many of the specifications apply from –40°C to +125°C. Parameters that can exhibit significant variance with regard to operating voltage or temperature are presented in the *Typical Characteristics*.

3.2.Input Offset Voltage and Input Offset Voltage Drift

Each amplifier is trimmed in production, thereby minimizing errors associated with input offset voltage and input offset voltage drift.

3.3.Capacitive Load and Stability

The OPA2376AIDR-HX/OPA2376AIDGKR-HX series of amplifiers may be used in applications where driving a capacitive load is required. As with all op amps, there may be specific instances where the OPA2376AIDR-HX/OPA2376AIDGKR-HX can become unstable, leading to oscillation. The particular op amp circuit configuration, layout, gain, and output loading are some of the factors to consider when establishing whether an amplifier will be stable in operation. An op amp in the unity-gain (+1-V/V) buffer configuration and driving a capacitive load exhibits a greater tendency to be unstable than an amplifier operated at a higher noise gain. The capacitive load, in conjunction with the op amp output resistance, creates a pole within the feedback loop that degrades the phase margin. The degradation of the phase margin increases as the capacitive loading increases.

Feature Description (continued)

The OPA2376AIDR-HX/OPA2376AIDGKR-HX in a unity-gain configuration can directly drive up to 250 pF of pure capacitive load. Increasing the gain enhances the ability of the amplifier to drive greater capacitive loads; see the typical characteristic Figure 16. In unity-gain configurations, capacitive load drive can be improved by inserting a small (10-Ω to 20-Ω) resistor, R_S, in series with the output, as shown in Figure 22. This resistor significantly reduces ringing while maintaining dc performance for purely capacitive loads. However, if there is a resistive load in parallel with the capacitive load, a voltage divider is created, introducing a gain error at the output and slightly reducing the output swing. The error introduced is proportional to the ratio R_S / R_L, and is generally negligible at low output current levels.

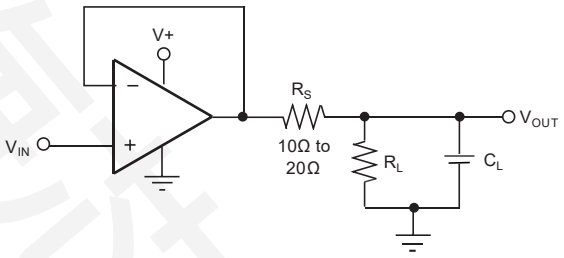


Figure 22. Improving Capacitive Load Drive

3.4.Common-Mode Voltage Range

The input common-mode voltage range of the OPA2376AIDR-HX/OPA2376AIDGKR-HX series extends 100 mV beyond the supply rails. The offset voltage of the amplifier is very low, from approximately (V^-) to (V^+) – 1 V, as shown in Figure 23. The offset voltage increases as common-mode voltage exceeds (V^+) –1 V. Common-mode rejection is specified from (V^-) to (V^+) – 1.3 V.

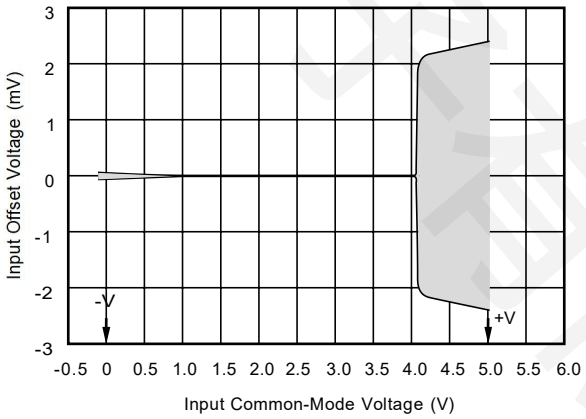


Figure 23. Offset and Common-Mode Voltage

Feature Description (continued)

3.5.Input and ESD Protection

The OPA2376AIDR-HX/OPA2376AIDGKR-HX family incorporates internal electrostatic discharge (ESD) protection circuits on all pins. In the case of input and output pins, this protection primarily consists of current steering diodes connected between the input and power-supply pins. These ESD protection diodes also provide in-circuit, input overdrive protection, as long as the current is limited to 10 mA as stated in the *Absolute Maximum Ratings*. Figure 24 shows how a series input resistor may be added to the driven input to limit the input current. The added resistor contributes thermal noise at the amplifier input and its value should be kept to a minimum in noise-sensitive applications.

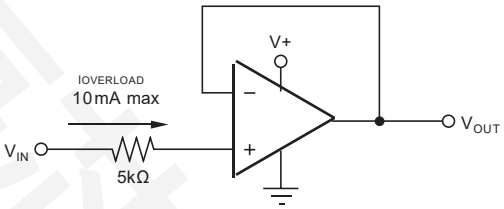


Figure 24. Input Current Protection

4.Device Functional Modes

The OPA2376AIDR-HX/OPA2376AIDGKR-HX has a single functional mode and is operational when the power-supply voltage is greater than 2.2 V (±1.1 V). The maximum power supply voltage for the OPA2376AIDR-HX/OPA2376AIDGKR-HX is 5.5 V (±2.75 V).

Application and Implementation

1.Application Information

The OPA2376AIDR-HX/OPA2376AIDGKR-HX family of operational amplifiers is built using *e-trim*, a proprietary technique in which offset voltage is adjusted during the final steps of manufacturing. This technique compensates for performance shifts that can occur during the molding process. Through *e-trim*, the OPA2376AIDR-HX/OPA2376AIDGKR-HX family delivers excellent offset voltage (5 μV, typical). Additionally, the amplifier boasts a fast slew rate, low drift, low noise, and excellent PSRR and A_{OL}. These 5.5-MHz CMOS op amps operate on 760-μA (typical) quiescent current.

1.1. Basic Amplifier Configurations

The OPA2376AIDR-HX/OPA2376AIDGKR-HX family is unity-gain stable. It does not exhibit output phase inversion when the input is overdriven. A typical single-supply connection is shown in Figure 25. The OPA2376AIDR-HX/OPA2376AIDGKR-HX is configured as a basic inverting amplifier with a gain of –10 V/V. This single-supply connection has an output centered on the common-mode voltage, V_{CM}. For the circuit shown, this voltage is 2.5 V, but may be any value within the common-mode input voltage range.

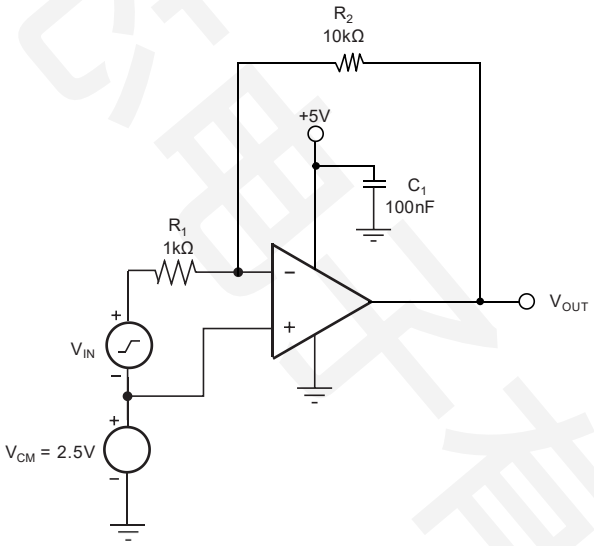


Figure 25. Basic Single-Supply Connection

Application Information

1.Phantom-Powered Microphone

The circuit shown in Figure 26 depicts how a remote microphone amplifier can be powered by a phantom source on the output side of the signal cable. The cable serves double duty, carrying both the differential output signal from and dc power to the microphone amplifier stage.

An OPA2376AIDR-HX/OPA2376AIDGKR-HX serves as a single-ended input to a differential output amplifier with a 6-dB gain. Common-mode bias for the two op amps is provided by the dc voltage developed across the electret microphone element. A

48-V phantom supply is reduced to 5.1 V by the series 6.8-kΩ resistors on the output side of the cable, and the 4.7-kΩ resistor and zener diode on the input side of the cable. AC coupling blocks the different dc voltage levels from each other on each end of the cable.

An INA163 instrumentation amplifier provides differential inputs and receives the balanced audio signals from the cable. The INA163 gain may be set from 0 dB to 80 dB by selecting the R_G value. The INA163 circuit is typical of the input circuitry used in mixing consoles.

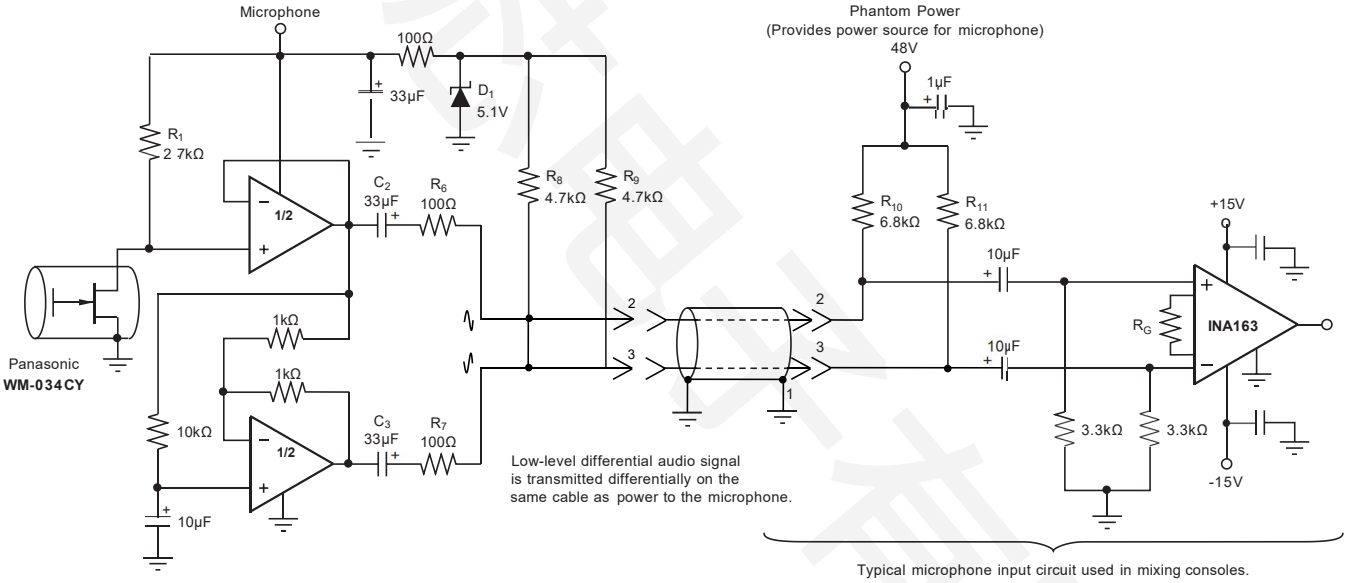
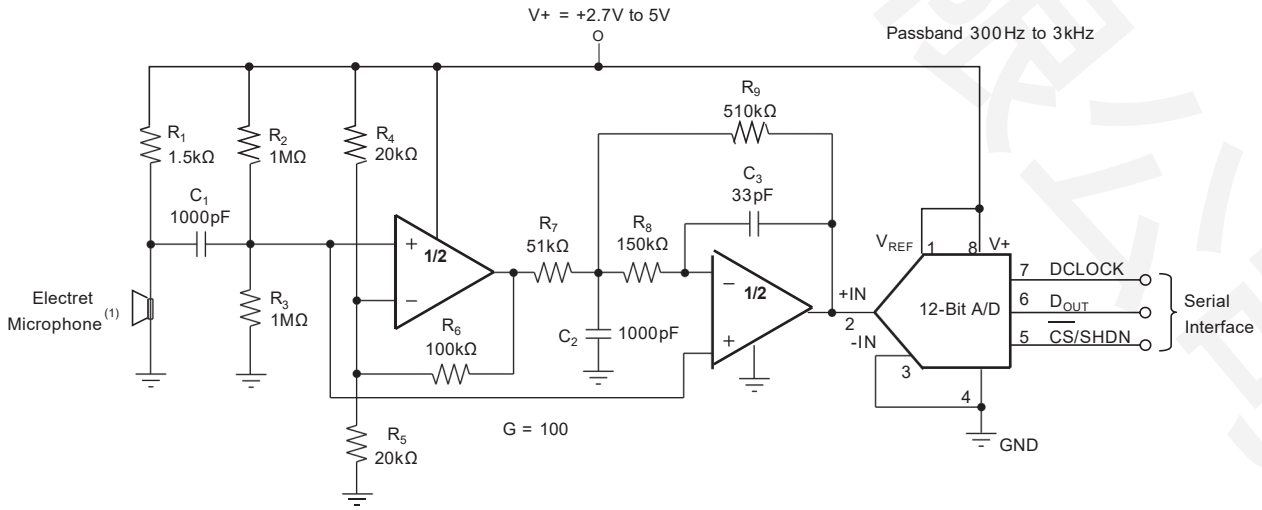


Figure 26. Phantom-Powered Electret Microphone



(1) Electret microphone powered by R_1.

Figure 27. OPA2376AIDR-HX/OPA2376AIDGKR-HX as a Speech Bandpass-Filtered, Data Acquisition System

2.Typical Application

Low-pass filters are commonly employed in signal processing applications to reduce noise and prevent aliasing. The OPA2376AIDR-HX/OPA2376AIDGKR-HX is ideally suited to construct high-speed, high-precision active filters. Figure 28 shows a second-order, low-pass filter commonly encountered in signal processing applications.

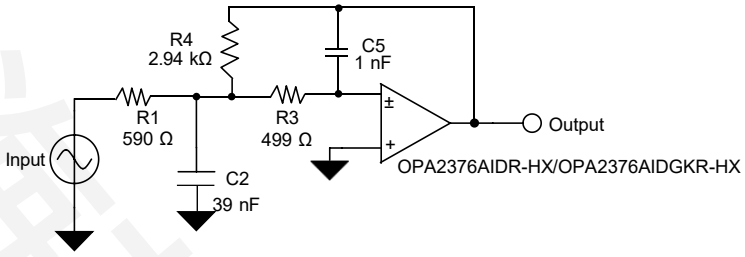


Figure 28. Typical Application Schematic

2.1 Design Requirements

Use the following parameters for this design example:

- Gain = 5 V/V (inverting gain)
- Low-pass cutoff frequency = 25 kHz
- Second-order Chebyshev filter response with 3-dB gain peaking in the passband

2.1.1 Detailed Design Procedure

The infinite-gain multiple-feedback circuit for a low-pass network function is shown in Figure 30. Use Equation 1 to calculate the voltage transfer function.

$$\frac{\text{Output}}{\text{Input}}(s) = \frac{-1/R_1R_3C_2C_5}{s^2 + (s/C_2)(1/R_1 + 1/R_3 + 1/R_4) + 1/R_3R_4C_2C_5} \quad (1)$$

This circuit produces a signal inversion. For this circuit, the gain at dc and the low-pass cutoff frequency are calculated by Equation 2:

$$\text{Gain} = \frac{R_4}{R_1}$$

Typical Application (continued)

2.2.Application Curve

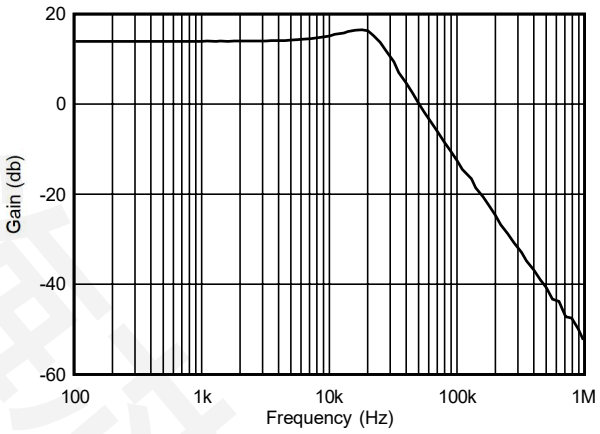


Figure 29. Low-Pass Filter Transfer Function

Power Supply Recommendations

The OPA2376AIDR-HX/OPA2376AIDGKR-HX are specified for operation from 2.2 V to 5.5 V (±1.1 V to ±2.75 V); many specifications apply from –40°C to +125°C. Parameters that can exhibit significant variance with regard to operating voltage or temperature are presented in the *Typical Characteristics*.

Layout

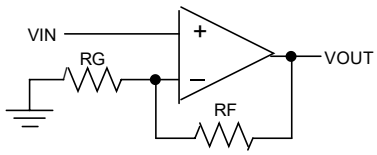
1.Layout Guidelines

For best operational performance of the device, use good PCB layout practices, including:

- Noise can propagate into analog circuitry through the power pins of the circuit as a whole, and the op amp itself. Bypass capacitors can reduce the coupled noise by providing low-impedance power sources local to the analog circuitry.
  - Connect low-ESR, 0.1-µF ceramic bypass capacitors between each supply pin and ground, placed as close to the device as possible. A single bypass capacitor from V+ to ground is applicable for single-supply applications.
- Separate grounding for analog and digital portions of circuitry is one of the simplest and most effective methods of noise suppression. One or more layers on multilayer PCBs are usually devoted to ground planes. A ground plane helps distribute heat, and reduces EMI noise pickup. Physically separate the digital and analog grounds, paying attention to the flow of the ground current.
- To reduce parasitic coupling, run the input traces as far away from the supply or output traces as possible. If these traces cannot be kept separate, crossing the sensitive trace perpendicular is better than opposed to in parallel with the noisy trace.
- Place the external components as close to the device as possible. As shown in Figure 30, keeping RF and RG close to the inverting input minimizes parasitic capacitance.
- Keep the length of the input traces as short as possible. The input traces are the most sensitive part of the circuit.
- Consider a driven, low-impedance guard ring around the critical traces. A guard ring can significantly reduce leakage currents from nearby traces that are at different potentials.
- Clean the PCB following board assembly for best performance.
- Any precision-integrated circuit may experience performance shifts due to moisture ingress into the plastic package. Following any aqueous PCB cleaning process, bake the PCB assembly to remove moisture introduced into the device packaging during the cleaning process. A low-temperature, post-cleaning bake at 85°C for 30 minutes is sufficient for most circumstances.

Layout Guidelines (continued)

2.Layout Example



(Schematic Representation)

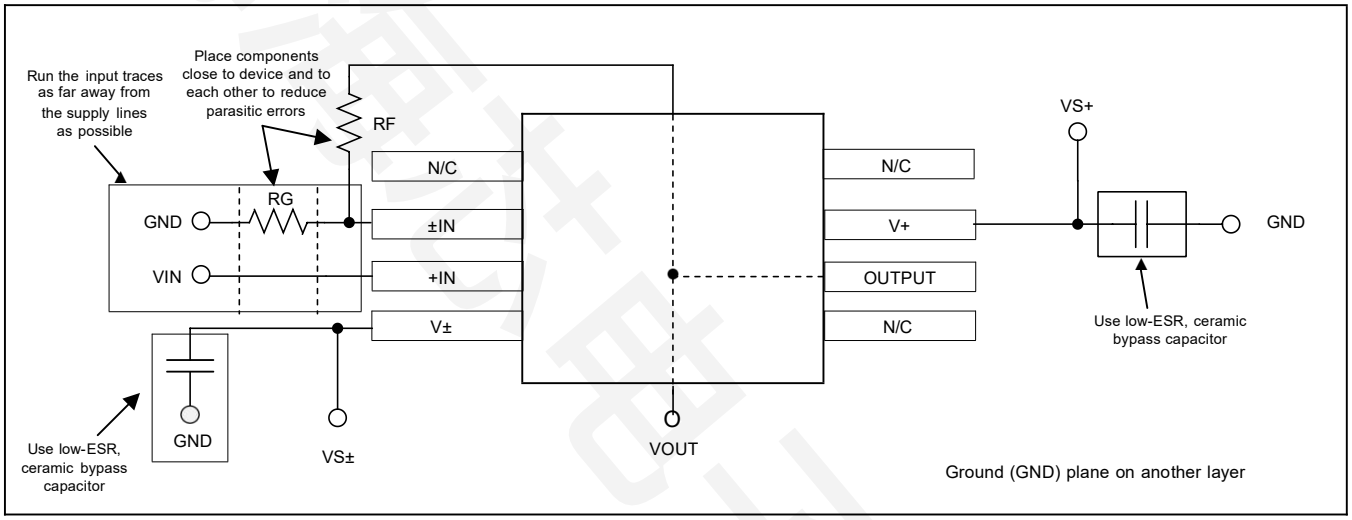
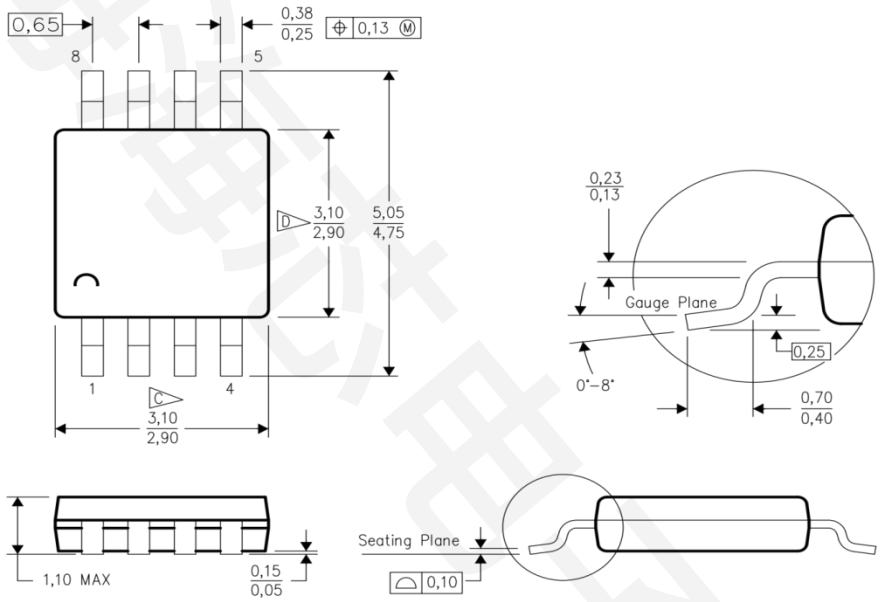


Figure 30. Layout Example

Package Details

OPA2376AIDGKR-HX

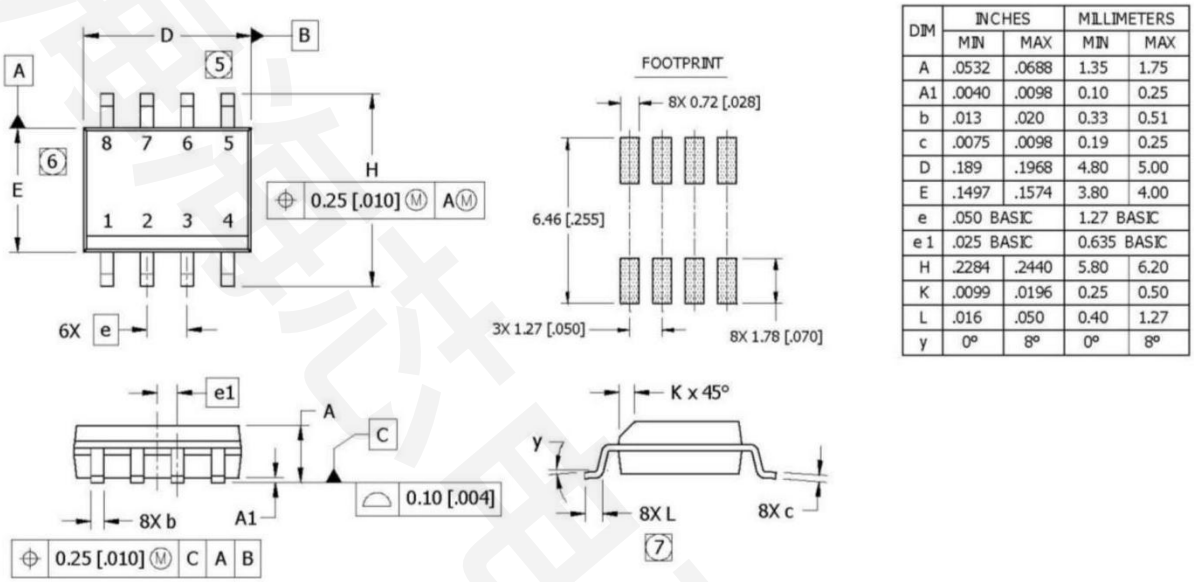
VSSOP-8



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 per end.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.50 per side.
E. Falls within JEDEC MO–187 variation AA, except interlead flash.

OPA2376AIDR-HX

SOIC-8



DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	.0532	.0688	1.35	1.75
A1	.0040	.0098	0.10	0.25
b	.013	.020	0.33	0.51
c	.0075	.0098	0.19	0.25
D	.189	.1968	4.80	5.00
E	.1497	.1574	3.80	4.00
e	.050 BASIC		1.27 BASIC	
e1	.025 BASIC		0.635 BASIC	
H	.2284	.2440	5.80	6.20
K	.0099	.0196	0.25	0.50
L	.016	.050	0.40	1.27
y	0°	8°	0°	8°

NOTES:
1. DIMENSIONING & TOLERANCING PER ASME Y14.5M-1994.
2. CONTROLLING DIMENSION: MILLIMETER
3. DIMENSIONS ARE SHOWN IN MILLIMETERS [INCHES].
4. OUTLINE CONFORMS TO JEDEC OUTLINE MS-012AA.

5. DIMENSION DOES NOT INCLUDE MOLD PROTRUSIONS. MOLD PROTRUSIONS NOT TO EXCEED 0.15 [.006].
6. DIMENSION DOES NOT INCLUDE MOLD PROTRUSIONS. MOLD PROTRUSIONS NOT TO EXCEED 0.25 [.010].
7. DIMENSION IS THE LENGTH OF LEAD FOR SOLDERING TO A SUBSTRATE.