OPA2140AIDR-HX High-Precision, Low-Noise, Rail-to-Rail Output, 11-MHz, JFET Op Amps

Description

The OPA2140AIDR-HX operational amplifier (op amp) features a series of low-power JFET input amplifiers that demonstrate exceptional drift characteristics and minimal input bias current. The rail-to-rail output swing and input range, which encompasses V–, empower designers to capitalize on the low-noise advantages of JFET amplifiers while effectively interfacing with contemporary single-supply precision analog-to-digital converters (ADCs) and digital -to-analog converters (DACs).

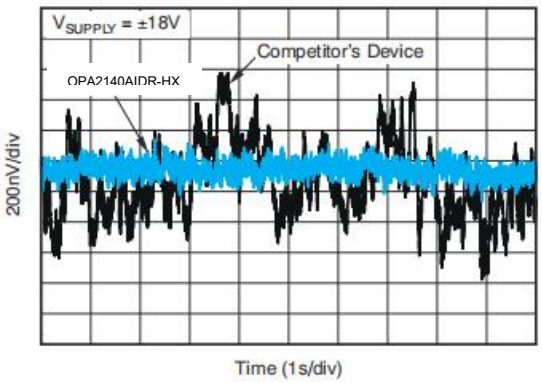
This device operates on a single supply voltage ranging from 4.5 V to 36 V or dual supplies of ±2.25 V to ±18 V. All versions are fully specified for operation in challenging environments, with a temperature range from –40°C to +125°C.The OPA2140AIDR-HX (dual) is available in an 8-pin SOIC package.

Features

- Very-low offset drift: 1 μV/°C maximum
- Very-low offset: 120 μV
- Low input bias current: 10 pA maximum
- Very-low 1/f noise: 250 nV_{PP}, 0.1 Hz to 10 Hz
- Low noise: 5.1 nV/√Hz
- Slew rate: 20 V/μs
- Low supply current: 2 mA maximum
- Input voltage range includes V– supply
- Single-supply operation: 4.5 V to 36 V
- Dual-supply operation: ±2.25 V to ±18 V
- No phase reversal
- Packages: – Industry-standard SOIC

Applications

- Intra-dc interconnect (metro)
- Semiconductor test
- Chemistry and gas analyzer
- DC power supply, ac source, electronic load
- Data acquisition (DAQ)
- Lab and field instrumentation



0.1-Hz to 10-Hz Noise

Pin Configuration and Functions

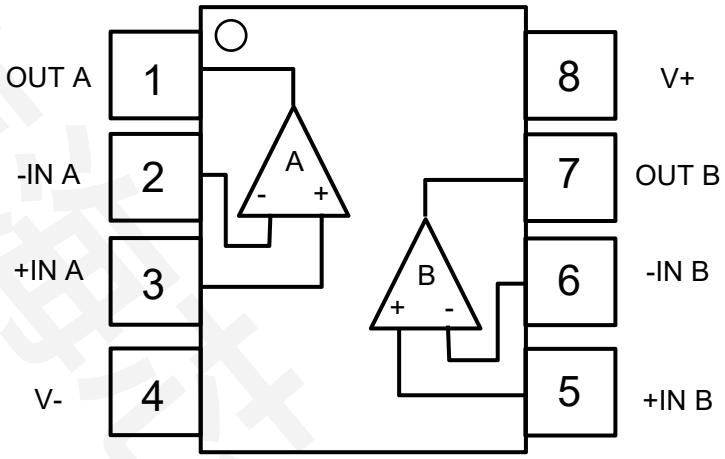


Figure 1. OPA2140AIDR-HX: 8-Pin SOIC(Top View)

Table 1. Pin Functions: OPA2140AIDR-HX

PIN		TYPE	DESCRIPTION
NAME	SOIC		
+IN A	3	Input	Noninverting input, channel A
+IN B	5	Input	Noninverting input, channel B
+IN C	—	Input	Noninverting input, channel C
+IN D	—	Input	Noninverting input, channel D
–IN A	2	Input	Inverting input, channel A
–IN B	6	Input	Inverting input, channel B
–IN C	—	Input	Inverting input, channel C
–IN D	—	Input	Inverting input, channel D
OUT A	1	Output	Output, channel A
OUT B	7	Output	Output, channel B
OUT C	—	Output	Output, channel C
OUT D	—	Output	Output, channel D
V+	8	—	Positive (highest) power supply
V–	4	—	Negative (lowest) power supply

Specifications

1. Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

			MIN	MAX	UNIT
V_S	Supply voltage, (V+) – (V–)	Dual supply		±20	V
		Single supply		40	
	Signal input pins(2)	Voltage	(V–) – 0.5	(V+) + 0.5	V
		Current		±10	mA
	Output short-circuit(3)		Continuous		
T_A	Ambient temperature		–55	150	°C
T_J	Junction temperature			150	°C
T_{stg}	Storage temperature		–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) Input pins are diode-clamped to the power-supply rails. Input signals that can swing more than 0.5 V beyond the supply rails must be current limited to 10 mA or less.
(3) Short-circuit to Vs / 2 (ground in symmetrical dual-supply setups), one amplifier per package.

2. ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

3. Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

			MIN	NOM	MAX	UNIT
V_S	Supply voltage, (V+) – (V–)	Dual supply	±2.25		±18	V
		Single supply	4.5		36	
T_A	Ambient temperature		–40		125	°C

4. Thermal Information: OPA2140AIDR-HX

THERMAL METRIC (1)		OPA2140AIDR-HX SOIC 8 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	160	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	75	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	60	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	9	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	50	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	°C/W

5. Electrical Characteristics

at T_A = 25°C, V_S = 4.5 V (±2.25) to 36 V (±18 V), R_L = 2 kΩ connected to midsupply, and V_{CM} = V_{OUT} = midsupply (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
OFFSET VOLTAGE							
V_{OS}	Input offset voltage				±30	±120	μV
		V_S = ±18 V, T_A = –40°C to +125°C				±220	
		V_S = ±2.25 V to ±18 V, T_A = –40°C to +125°C				±4	μV/V
dV_{OS}/dT	Input offset voltage drift	V_S = ±18 V, T_A = –40°C to +125°C			±0.35	±1	μV/°C
PSRR	Power-supply rejection ratio	V_S = ±2.25 V to ±18 V, T_A = –40°C to +125°C			±0.1	±0.5	μV/V
INPUT BIAS CURRENT							
I_B	Input bias current				±0.5	±10	pA
		T_A = –40°C to +125°C				±3	nA
I_{OS}	Input offset current				±0.5	±10	pA
		T_A = –40°C to +125°C				±1	nA
NOISE							
E_n	Input voltage noise	f = 0.1 Hz to 10 Hz			250		nV_{PP}
		f = 0.1 Hz to 10 Hz			42		nV_{RMS}
e_n	Input voltage noise density	f = 10 Hz			8		nV/√Hz
		f = 100 Hz			5.8		
		f = 1 kHz			5.1		
I_n	Input current noise density	f = 1 kHz			0.8		fA/√Hz
INPUT VOLTAGE RANGE							
V_{CM}	Common-mode voltage	T_A = –40°C to +125°C		(V–) – 0.1		(V+) – 3.5	V
CMRR	Common-mode rejection ratio	V_S = ±18 V, V_{CM} = (V–) – 0.1 V to (V+) – 3.5 V		126	140		dB
			T_A = –40°C to +125°C	120			
INPUT IMPEDANCE							
Z_{ID}	Differential				10^{13} || 10		Ω || pF
Z_{IC}	Common-mode	V_{CM} = (V–) –0.1 V to (V+) –3.5 V			10^{13} || 7		Ω || pF
OPEN-LOOP GAIN							
A_{OL}	Open-loop voltage gain	V_O = (V–) + 0.35 V to (V+) – 0.35 V, R_L = 10 kΩ		120	126		dB
		V_O = (V–) + 0.35 V to (V+) – 0.35 V, R_L = 2 kΩ		114	126		
			T_A = –40°C to +125°C	108			
FREQUENCY RESPONSE							
BW	Gain bandwidth product				11		MHz
SR	Slew rate				20		V/μs
t_s	Settling time	12 bits			0.88		μs
		16 bits			1.6		
t_{OR}	Overload recovery time				600		ns
THD+N	Total harmonic distortion + noise	1 kHz, G = +1, V_O = 3.5 V_{RMS}			0.00005%		
OUTPUT							
V_O	Voltage output	R_L = 10 kΩ, A_{OL} ≥ 108 dB		(V–) + 0.2		(V+) – 0.2	V
		R_L = 2 kΩ, A_{OL} ≥ 108 dB		(V–) + 0.35		(V+) – 0.35	
I_{SC}	Short-circuit current	Source			36		mA
		Sink			–30		
C_{LOAD}	Capacitive load drive			See *Typical Characteristics*			
Z_O	Open-loop output impedance	f = 1 MHz, I_O = 0 A (See *Typical Characteristics*)			16		Ω

6. Electrical Characteristics (continued)

at T_A = 25°C, V_S = 4.5 V (±2.25) to 36 V (±18 V), R_L = 2 kΩ connected to midsupply, and V_{CM} = V_{OUT} = midsupply (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
POWER SUPPLY						
I_Q	Quiescent current per amplifier	I_O = 0 mA		1.8	2	mA
		T_A = –40°C to +125°C			2.7	
CHANNEL SEPARATION						
	Channel separation	At dc		0.02		µV/V
		At 100 kHz		10		

7. Typical Characteristics

at T_A = 25°C, V_S = ±18 V, R_L = 2 kΩ connected to midsupply, and V_{CM} = V_{OUT} = midsupply (unless otherwise noted)

8. Typical Characteristics

at T_A = 25°C, V_S = ±18 V, R_L = 2 kΩ connected to midsupply, and V_{CM} = V_{OUT} = midsupply (unless otherwise noted)

Table 2. Table of Graphs (continued)

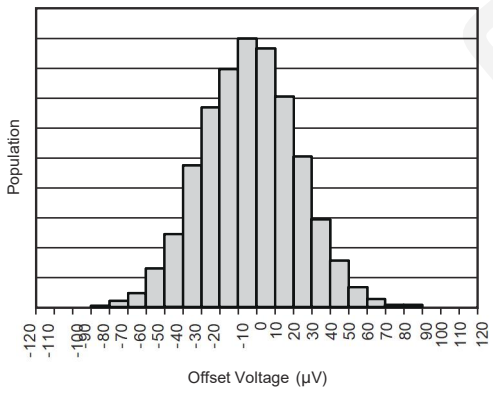


Figure 2. Offset Voltage Production Distribution

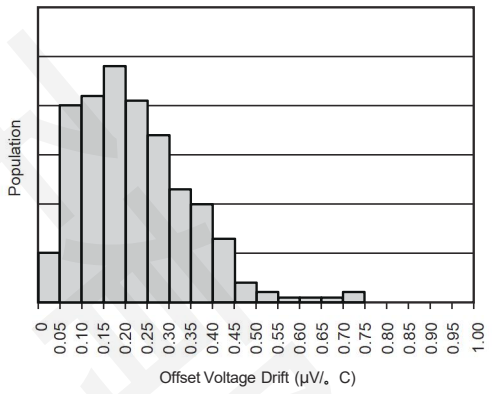


Figure 3. Offset Voltage Drift Distribution

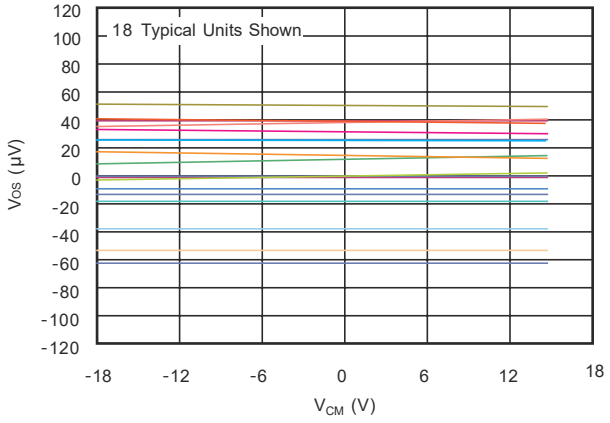


Figure 4. Offset Voltage vs Common-Mode Voltage

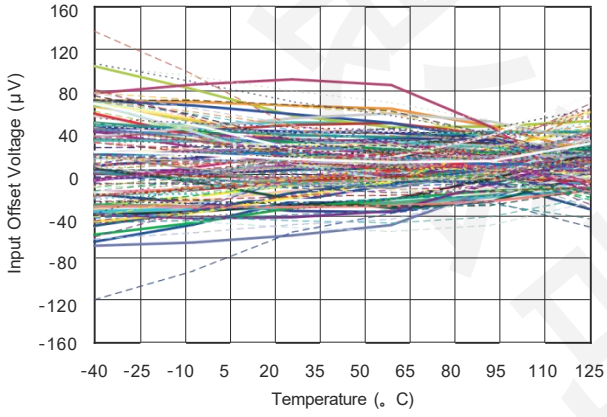


Figure 5. Input Offset Voltage vs Temperature (144 Amplifiers)

8. Typical Characteristics (continued)

at T_A = 25°C, V_S = ±18 V, R_L = 2 kΩ connected to midsupply, and V_{CM} = V_{OUT} = midsupply (unless otherwise noted)

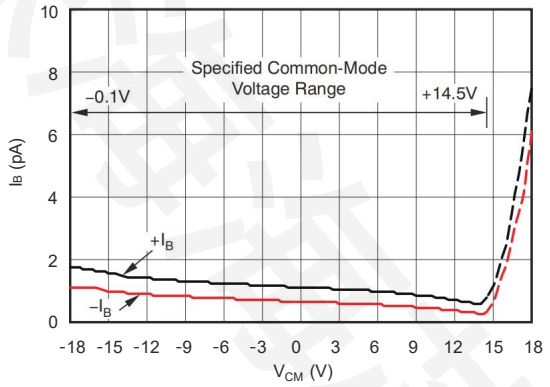


Figure 6. I_B vs Common-Mode Voltage

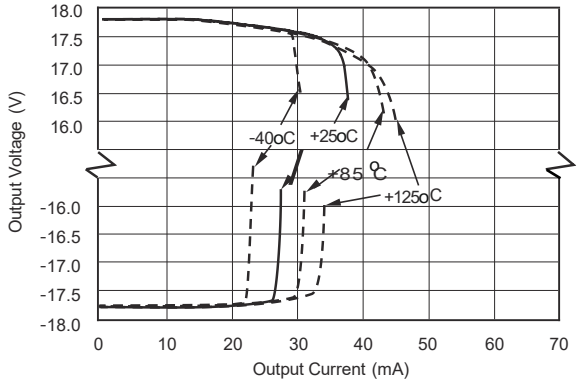


Figure 7. Output Voltage Swing vs Output Current (Maximum Supply)

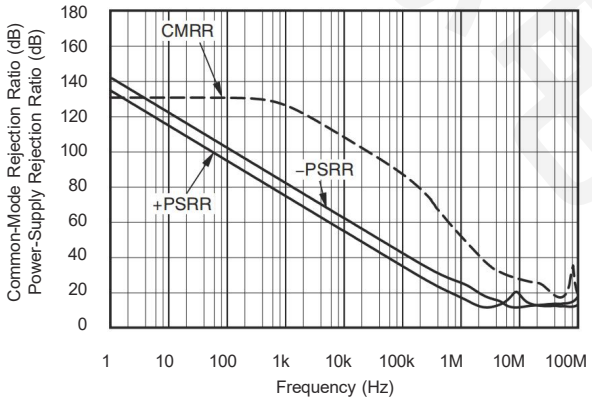


Figure 8. CMRR and PSRR vs Frequency (Referred to Input)

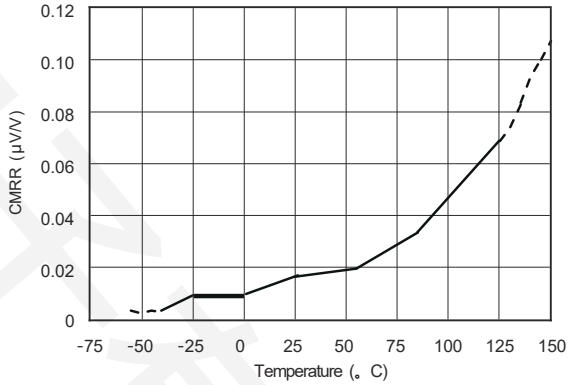


Figure 9. Common-Mode Rejection Ratio vs Temperature

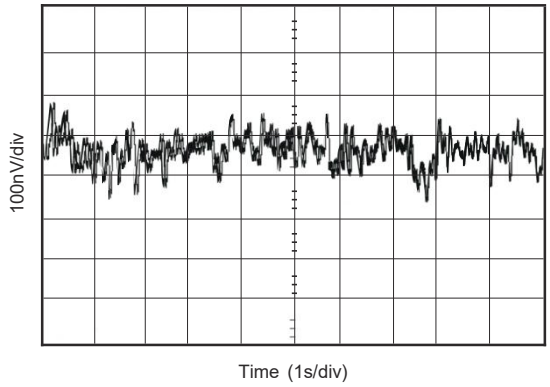


Figure 10. 0.1-Hz to 10-Hz Noise

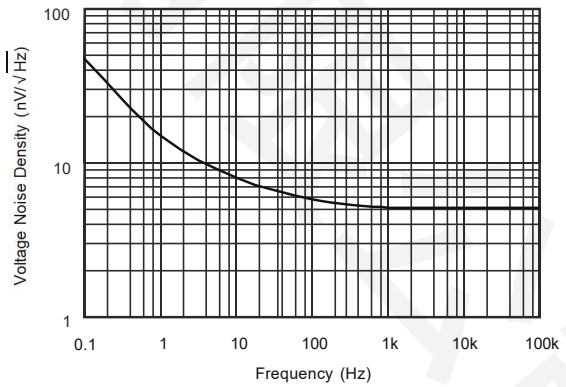


Figure 11. Input Voltage Noise Density vs Frequency

8. Typical Characteristics (continued)

at T_A = 25°C, V_S = ±18 V, R_L = 2 kΩ connected to midsupply, and V_{CM} = V_{OUT} = midsupply (unless otherwise noted)

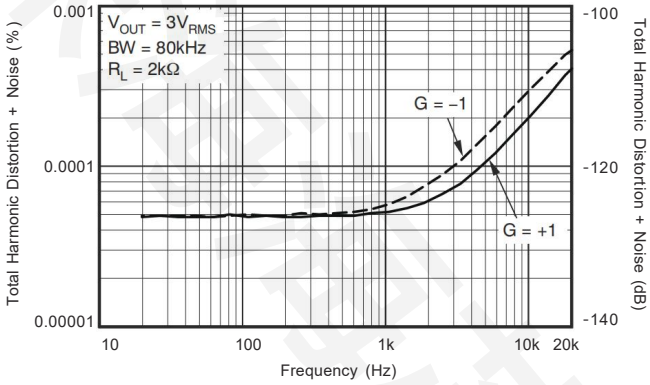


Figure 12. THD+N Ratio vs Frequency

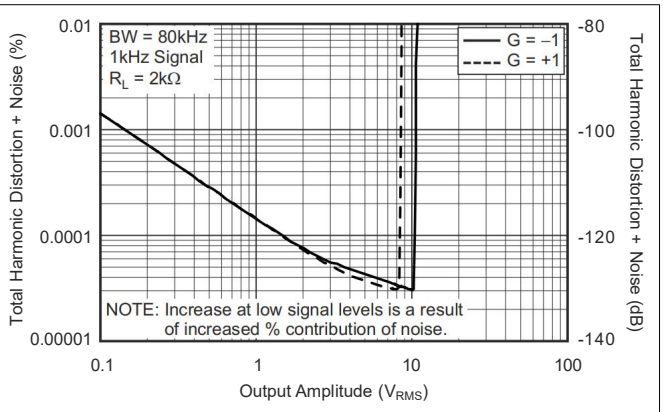


Figure 13. THD+N Ratio vs Output Amplitude

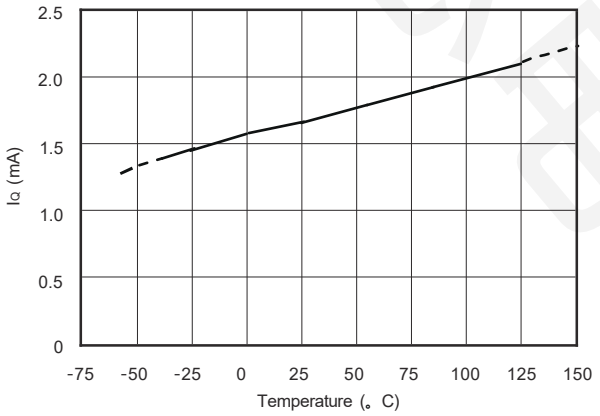


Figure 14. Quiescent Current vs Temperature

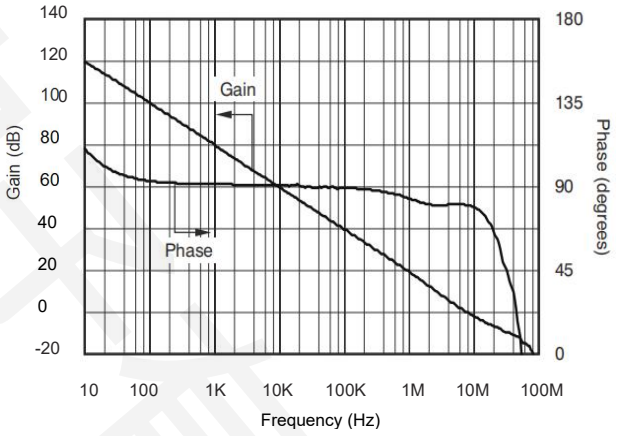


Figure 15. Gain and Phase vs Frequency

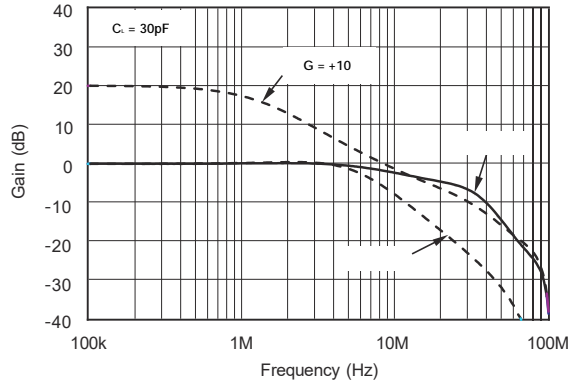


Figure 16. Closed-Loop Gain vs Frequency

8. Typical Characteristics (continued)

at T_A = 25°C, V_S = ±18 V, R_L = 2 kΩ connected to midsupply, and V_{CM} = V_{OUT} = midsupply (unless otherwise noted)

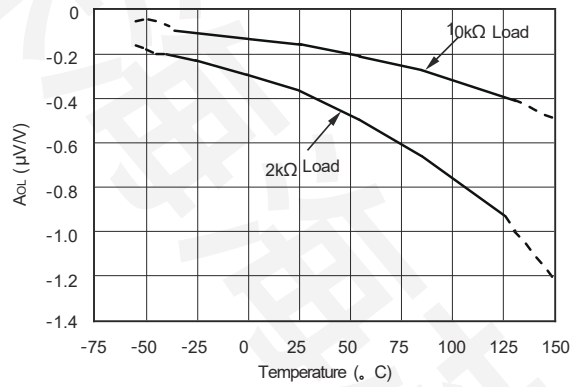


Figure 17. Open-Loop Gain vs Temperature

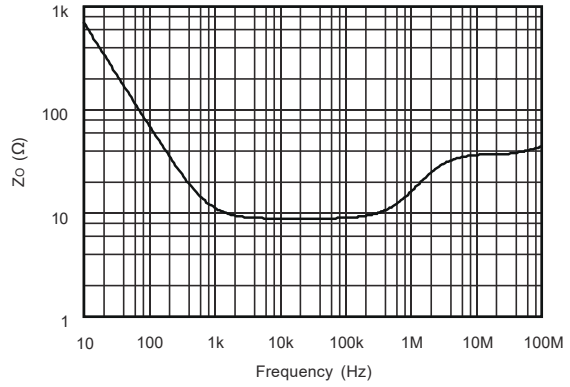


Figure 18. Open-Loop Output Impedance vs Frequency

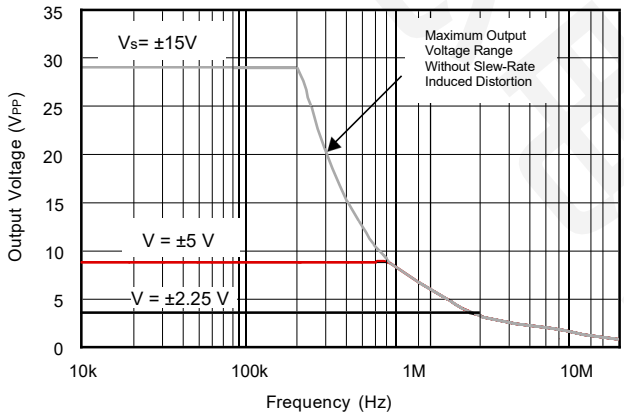


Figure 19. Maximum Output Voltage vs Frequency

8. Typical Characteristics (continued)

at T_A = 25°C, V_S = ±18 V, R_L = 2 kΩ connected to midsupply, and V_{CM} = V_{OUT} = midsupply (unless otherwise noted)

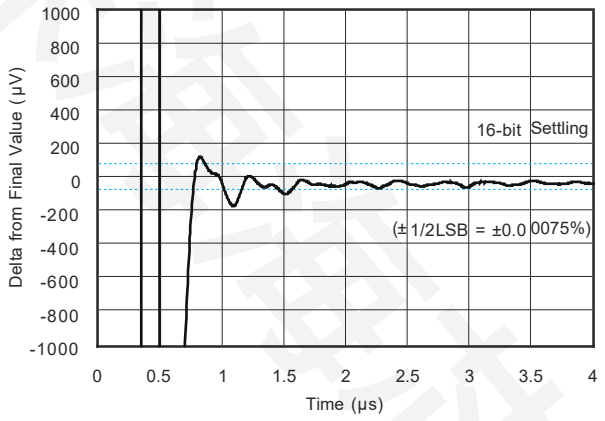


Figure 20. Large-Signal Positive Settling Time (10-V Step)

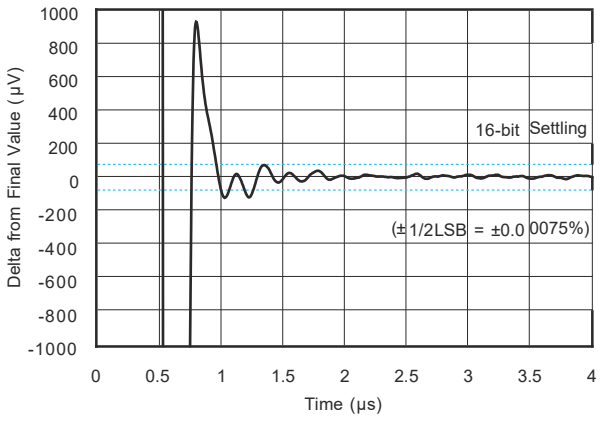


Figure 21. Large-Signal Negative Settling Time (10-V Step)

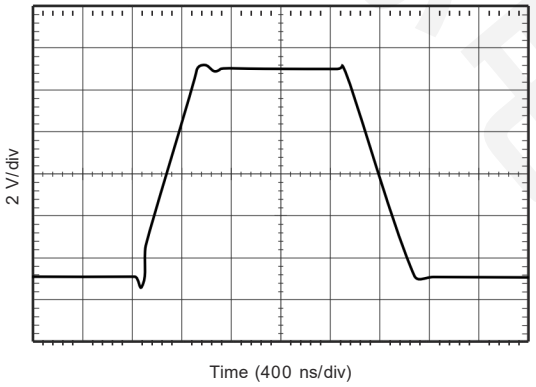


Figure 22. Large-Signal Step Response

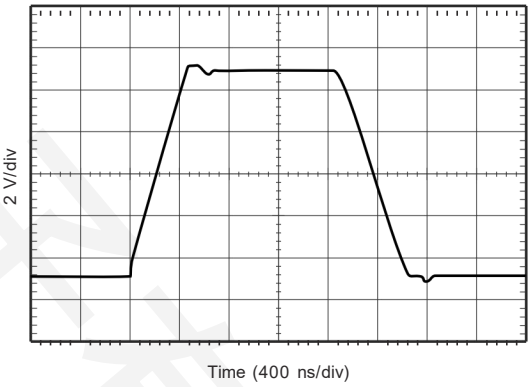


Figure 23. Large-Signal Step Response

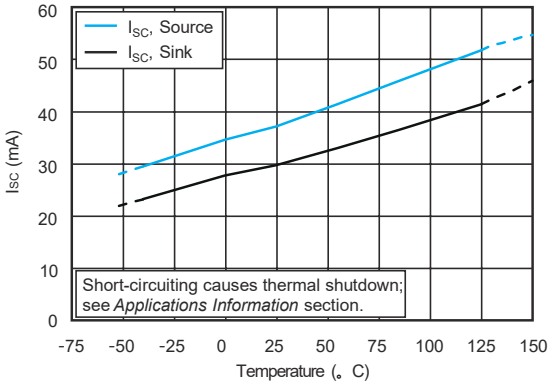


Figure 24. Short Circuit Current vs Temperature

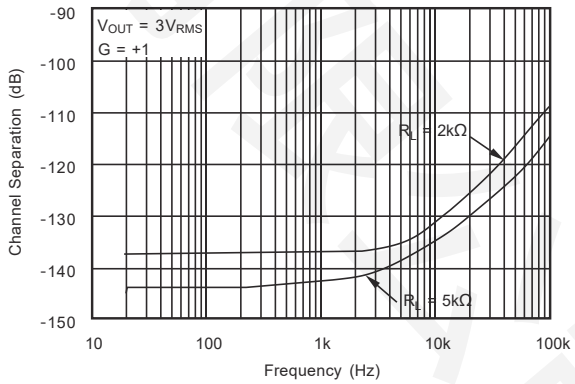


Figure 25. Channel Separation vs Frequency

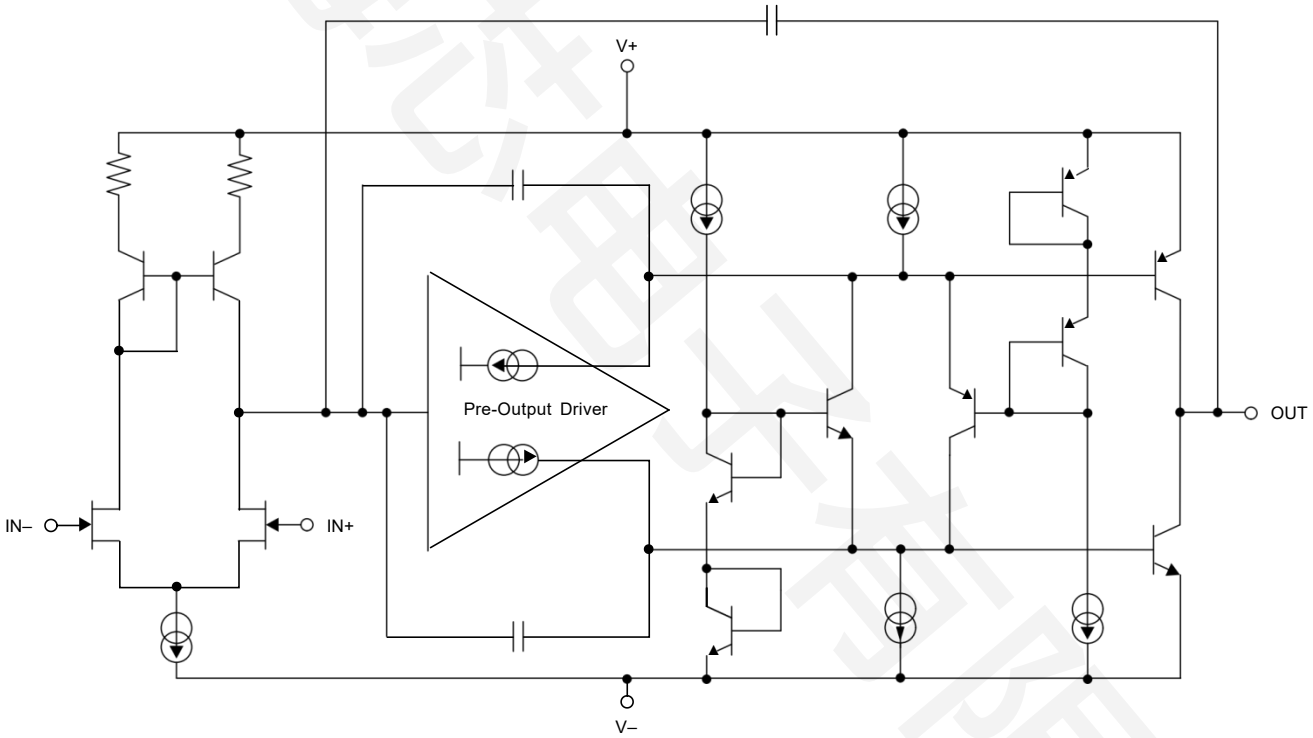
Detailed Description

1. Overview

The OPA2140AIDR-HX of operational amplifiers is a series of low-power JFET input amplifiers that feature excellent drift performance and low input bias current. The rail-to-rail output swing and input range that includes V– allow designers to use the low-noise characteristics of JFET amplifiers while also interfacing to modern, single-supply, precision analog-to-digital converters (ADCs) and digital-to-analog converters (DACs). The OPA2140AIDR-HX achieves 11-MHz unity-gain bandwidth and 20-V/μs slew rate, and consumes only 1.8 mA (typical) of quiescent current. These devices operate on a single 4.5-V to 36-V supply or dual ±2.25-V to ±18-V supplies.

Section 2 shows the simplified diagram of the OPA2140AIDR-HX.

2. Functional Block Diagram



3. Feature Description

3.1. Operating Voltage

The OPA2140AIDR-HX of op amps can be used with single or dual supplies from an operating range of V_S = 4.5 V (±2.25 V) and up to V_S = 36 V (±18 V). These devices do not require symmetrical supplies, but only a minimum supply voltage of 4.5 V (±2.25 V). For V_S less than ±3.5 V, the common-mode input range does not include midsupply. Supply voltages higher than 40 V can permanently damage the device.Key parameters are specified over the operating temperature range, T_A = –40°C to 125°C.

3.2. Capacitive Load and Stability

The dynamic characteristics of the OPA2140AIDR-HX have been optimized for commonly encountered gains, loads, and operating conditions. The combination of low closed-loop gain and high capacitive loads decreases the phase margin of the amplifier and can lead to gain peaking or oscillations. As a result, heavier capacitive loads must be isolated from the output. The simplest way to achieve this isolation is to add a small resistor (R_{OUT} equal to 50 Ω, for example) in series with the output.

3.3. Output Current Limit

The output current of the OPA2140AIDR-HX series is limited by internal circuitry to 36 mA/–30 mA (sourcing/sinking), to protect the device if the output is accidentally shorted. This short circuit current depends on temperature, as shown in Figure 24.

3.4. Noise Performance

The op amp contributes both a voltage noise component and a current noise component. The voltage noise is commonly modeled as a time-varying component of the offset voltage. The current noise is modeled as the time-varying component of the input bias current and reacts with the source resistance to create a voltage component of noise. Therefore, the lowest noise op amp for a given application depends on the source impedance. For low source impedance, current noise is negligible, and voltage noise generally dominates. The OPA2140AIDR-HX has both low voltage noise and extremely low current noise because of the FET input of the op amp. As a result, the current noise contribution of the OPA2140AIDR-HX is negligible for any practical source impedance, which makes these devices the better choice for applications with high source impedance.

3.5. Basic Noise Calculations

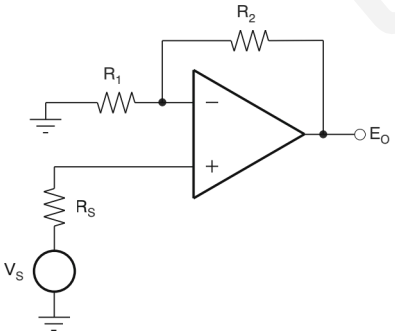
Low-noise circuit design requires careful analysis of all noise sources. External noise sources can dominate in many cases; consider the effect of source resistance on overall op amp noise performance. Total noise of the circuit is the root-sum-square combination of all noise components.

The resistive portion of the source impedance produces thermal noise proportional to the square root of the resistance. The source impedance is usually fixed; consequently, select the op amp and the feedback resistors to minimize the respective contributions to the total noise.

In circuit configurations with gain, the feedback network resistors also contribute noise. In general, the current noise of the op amp reacts with the feedback resistors to create additional noise components. However, the extremely low current noise of the OPA2140AIDR-HX means that the current noise contribution can be neglected.

The feedback resistor values can generally be chosen to make these noise sources negligible. Low impedance feedback resistors load the output of the amplifier.The equations for total noise are shown for both configurations.

A) Noise in Noninverting Gain Configuration



Noise at the output:

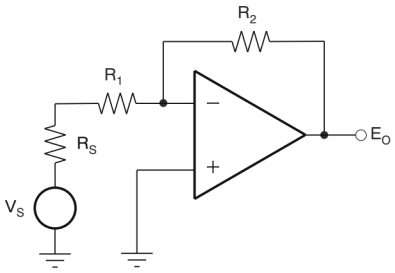
$$E_O^2 = \left(1 + \frac{R_2}{R_1}\right)^2 e_n^2 + \left(\frac{R_2}{R_1}\right)^2 e_1^2 + e_2^2 + \left(1 + \frac{R_2}{R_1}\right)^2 e_s^2$$

Where $e_S = \sqrt{4kTR_S}$ = thermal noise of R_S

$e_1 = \sqrt{4kTR_1}$ = thermal noise of R_1

$e_2 = \sqrt{4kTR_2}$ = thermal noise of R_2

B) Noise in Inverting Gain Configuration



Noise at the output:

$$E_O^2 = \left(1 + \frac{R_2}{R_1 + R_S}\right)^2 e_n^2 + \left(\frac{R_2}{R_1 + R_S}\right)^2 e_1^2 + e_2^2 + \left(\frac{R_2}{R_1 + R_S}\right)^2 e_s^2$$

Where $e_S = \sqrt{4kTR_S}$ = thermal noise of R_S

$e_1 = \sqrt{4kTR_1}$ = thermal noise of R_1

$e_2 = \sqrt{4kTR_2}$ = thermal noise of R_2

For the OPA2140AIDR-HX of operational amplifiers at 1 kHz, e_n = 5.1 nV/√Hz.

Figure 26. Noise Calculation in Gain Configurations

3.6. Phase-Reversal Protection

The OPA2140AIDR-HX has internal phase-reversal protection. Many FET- and bipolar- input op amps exhibit a phase reversal when the input is driven beyond the linear common-mode range. This condition is most often encountered in noninverting circuits when the input is driven beyond the specified common-mode voltage range, causing the output to reverse into the opposite rail.The input circuitry of the OPA2140AIDR-HX prevents phase reversal with excessive common-mode voltage; instead, the output limits into the appropriate rail.

3.7. Thermal Protection

The OPA2140AIDR-HX of op amps are capable of driving 2-kΩ loads with power-supply voltages of up to ±18V over the specified temperature range. In a single-supply configuration, where the load is connected to the negative supply voltage, the minimum load resistance is 2.8 kΩ at a supply voltage of 36 V. For lower supply voltages (either single-supply or symmetrical supplies), a lower load resistance can be used, as long as the output current does not exceed 13 mA; otherwise, the device short circuit current protection circuit can activate. Internal power dissipation increases when operating at high supply voltages. Copper leadframe construction used in the OPA2140AIDR-HX devices improves heat dissipation compared to conventional materials. Printed-circuit-board (PCB) layout can also help reduce a possible increase in junction temperature (TJ). Wide copper traces help dissipate the heat by acting as an additional heatsink. Temperature rise can be further minimized by soldering the devices directly to the PCB rather than using a socket.

Although the output current is limited by internal protection circuitry, accidental shorting of one or more output channels of a device can result in excessive heating. For instance, when an output is shorted to mid-supply, the typical short-circuit current of 36 mA leads to an internal power dissipation of over 600 mW at a supply of ±18 V. Total power dissipation (PD) includes both the quiescent power dissipation (PDQ) and the power dissipation due to the load (PDL).

$$T_J = T_A + (P_{DQ} + P_{DL}) \times R_{\theta JA} \quad (1)$$

To prevent excessive heating, the OPA2140AIDR-HX has an internal thermal shutdown circuit that shuts down the device if the die temperature exceeds approximately 180°C. When this thermal shutdown circuit activates, a built-in hysteresis of 15°C makes sure that the die temperature must drop to approximately 165°C before the device switches on again.

Additional consideration is needed for the combination of maximum operating voltage, maximum operating temperature, load, and package type.

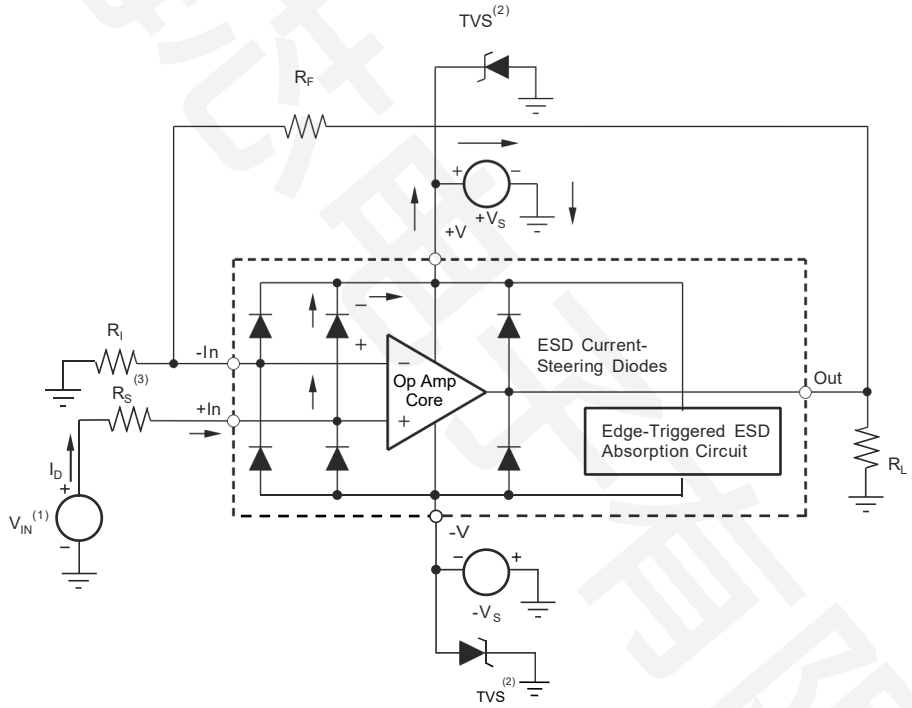
Moreover, resistive loading of the output causes additional power dissipation and thus self-heating, which also must be considered when establishing the maximum supply voltage or operating temperature. In symmetrical, bipolar supplies, the worst case dc condition is given by V OUT = ±VS/4.

As shown by Equation 1, the junction temperature depends on the thermal properties of the package, as expressed by RΘJA. If the device then begins to drive a heavy load, the junction temperature can rise and trip the thermal-shutdown circuit. Proper PCB layout is essential to realize this improved thermal behavior. For more information on PCB layout best practices, see Application and Implementation Section 4.1.

3.8. Electrical Overstress

Designers often ask questions about the capability of an operational amplifier to withstand electrical overstress. These questions tend to focus on the device inputs, but can involve the supply voltage pins or even the output pin. Each of these different pin functions have electrical stress limits determined by the voltage breakdown characteristics of the particular semiconductor fabrication process and specific circuits connected to the pin. Additionally, internal electrostatic discharge (ESD) protection is built into these circuits to protect them from accidental ESD events both before and during product assembly.

A good understanding of this basic ESD circuitry and the relevance to an electrical overstress event is helpful. Figure 27 shows an illustration of the ESD circuits contained in the OPA2140AIDR-HX (indicated by the dashed line area). The ESD protection circuitry involves several current-steering diodes connected from the input and output pins and routed back to the internal power-supply lines, where the diodes meet at an absorption device internal to the operational amplifier. This protection circuitry is intended to remain inactive during normal circuit operation.



(1) V_{IN} = +V_S + 500 mV.
(2) TVS: $+V_{S(max)} > V_{TVSBR\ (Min)} > +V_S$
(3) Suggested value approximately 1 kΩ.

Figure 27. Equivalent Internal ESD Circuitry Relative to a Typical Circuit Application

An ESD event produces a short duration, high-voltage pulse that is transformed into a short duration, high- current pulse when discharging through a semiconductor device. The ESD protection circuits are designed to provide a current path around the operational amplifier core to prevent damage. The energy absorbed by the protection circuitry is then dissipated as heat.

When an ESD voltage develops across two or more of the amplifier device pins, current flows through one or more of the steering diodes. Depending on the path that the current takes, the absorption device can activate. The absorption device has a trigger, or threshold voltage, that is above the normal operating voltage of the OPA2140AIDR-HX but below the device breakdown voltage level. When this threshold is exceeded, the absorption device quickly activates and clamps the voltage across the supply rails to a safe level.

When the operational amplifier connects into a circuit, as Figure 27 shows, the ESD protection components are intended to remain inactive and not become involved in the application circuit operation. However, circumstances can arise where an applied voltage exceeds the operating voltage range of a given pin. If this condition occurs, there is a risk that some of the internal ESD protection circuits can be biased on and conduct current. Any such current flow occurs through steering diode paths and rarely involves the absorption device.

Figure 27 shows a specific example where the input voltage, V_{IN}, exceeds the positive supply voltage ($+V_S$) by 500 mV or more. Much of what happens in the circuit depends on the supply characteristics. If $+V_S$ can sink the current, one of the upper input steering diodes conducts and directs current to $+V_S$. Excessively high current levels can flow with increasingly higher V_{IN}. As a result, the data sheet specifications recommend that applications limit the input current to 10 mA.

If the supply is not capable of sinking the current, V_{IN} can begin sourcing current to the operational amplifier, and then take over as the source of positive supply voltage. The danger in this case is that the voltage can rise to levels that exceed the operational amplifier absolute maximum ratings.

Another common question involves what happens to the amplifier if an input signal is applied to the input while the power supplies $+V_S$ or $–V_S$ are at 0 V. Again, the answer depends on the supply characteristic while at 0 V, or at a level below the input signal amplitude. If the supplies appear as high impedance, then the operational amplifier supply current can be supplied by the input source through the current steering diodes. This state is not a normal bias condition; the amplifier most likely does not operate normally. If the supplies are low impedance, then the current through the steering diodes can become quite high. The current level depends on the ability of the input source to deliver current, and any resistance in the input path.

If there is an uncertainty about the ability of the supply to absorb this current, external Zener diodes can be added to the supply pins; see Figure 27. Select the Zener voltage so that the diode does not turn on during normal operation. However, the Zener voltage must be low enough so that the Zener diode conducts if the supply pin begins to exceed the safe operating supply voltage level.

3.9. EMI Rejection

The electromagnetic interference (EMI) rejection ratio, or EMIRR, describes the EMI immunity of operational amplifiers. An adverse effect that is common to many op amps is a change in the offset voltage as a result of RF signal rectification. An op amp that is more efficient at rejecting this change in offset as a result of EMI has a higher EMIRR and is quantified by a decibel value. Measuring EMIRR can be performed in many ways, but this section provides the EMIRR IN+, which specifically describes the EMIRR performance when the RF signal is applied to the noninverting input pin of the op amp. In general, only the noninverting input is tested for EMIRR for the following three reasons:

- Op amp input pins are known to be the most sensitive to EMI, and typically rectify RF signals better than the supply or output pins.
- The noninverting and inverting op amp inputs have symmetrical physical layouts and exhibit nearly matching EMIRR performance
- EMIRR is easier to measure on noninverting pins than on other pins because the noninverting input terminal can be isolated on a PCB. This isolation allows the RF signal to be applied directly to the noninverting input terminal with no complex interactions from other components or connecting PCB traces. Figure 28

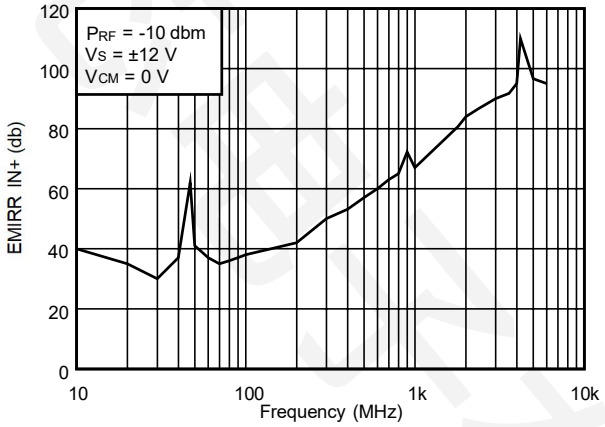


Figure 28. OPA2140AIDR-HX EMIRR

The EMIRR IN+ of the OPA2140AIDR-HX is plotted versus frequency as shown in .If available, any dual and quad op amp device versions have nearly similar EMIRR IN+ performance. The OPA2140AIDR-HX unity-gain bandwidth is 11 MHz. EMIRR performance below this frequency denotes interfering signals that fall within the op amp bandwidth.

Table 3 lists the EMIRR IN+ values for the OPA2140AIDR-HX at particular frequencies commonly encountered in real- world applications. Applications listed in Table 3 can be centered on or operated near the particular frequency shown. This information can be of special interest to designers working with these types of applications, or working in other fields likely to encounter RF interference from broad sources, such as the industrial, scientific, and medical (ISM) radio band.

Table 3. OPA2140AIDR-HX EMIRR IN+ for Frequencies of Interest

FREQUENCY	APPLICATION OR ALLOCATION	EMIRR IN+
400 MHz	Mobile radio, mobile satellite, space operation, weather, radar, ultra-high frequency (UHF) applications	53.1 dB
900 MHz	Global system for mobile communications (GSM) applications, radio communication, navigation, GPS (to 1.6 GHz), GSM, aeronautical mobile, UHF applications	72.2 dB
1.8 GHz	GSM applications, mobile personal communications, broadband, satellite, L-band (1 GHz to 2 GHz)	80.7 dB
2.4 GHz	802.11b, 802.11g, 802.11n, Bluetooth®, mobile personal communications, industrial, scientific and medical (ISM) radio band, amateur radio and satellite, S-band (2 GHz to 4 GHz)	86.8 dB
3.6 GHz	Radiolocation, aero communication and navigation, satellite, mobile, S-band	91.7 dB
5 GHz	802.11a, 802.11n, aero communication and navigation, mobile communication, space and satellite operation, C-band (4 GHz to 8 GHz)	96.6 dB

3.10 EMIRR +IN Test Configuration

Figure 29 shows the circuit configuration for testing the EMIRR IN+. An RF source is connected to the op amp noninverting input terminal using a transmission line. The op amp is configured in a unity gain buffer topology with the output connected to a low-pass filter (LPF) and a digital multimeter (DMM). A large impedance mismatch at the op amp input causes a voltage reflection; however, this effect is characterized and accounted for when determining the EMIRR IN+. The resulting DC offset voltage is sampled and measured by the multimeter. The LPF isolates the multimeter from residual RF signals that can interfere with multimeter accuracy.

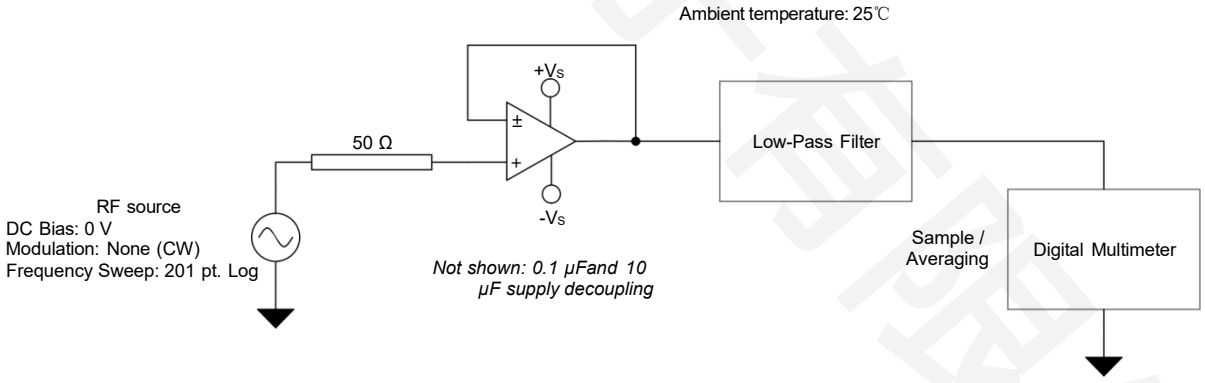


Figure 29. EMIRR +IN Test Configuration

4 Device Functional Modes

The OPA2140AIDR-HX has a single functional mode and is operational when the power-supply voltage is greater than 4.5 V (±2.25 V). The maximum power supply voltage for the OPA2140AIDR-HX is 36 V (±18 V).

Application and Implementation

Note: Information in the following applications sections is not part of the component specification, and does not warrant its accuracy or completeness.Customers are responsible for determining suitability of components for their purposes,as well as validating and testing their design implementation to confirm system functionality.

1. Application Information

The OPA2140AIDR-HX are unity-gain stable, operational amplifiers with very low noise, input bias current, and input offset voltage. Applications with noisy or high-impedance power supplies require decoupling capacitors placed close to the device pins. In most cases, 0.1-μF capacitors are adequate. Designers can easily use the rail-to-rail output swing and input range that includes V– to take advantage of the low-noise characteristics of JFET amplifiers while also interfacing to modern, single-supply, precision data converters.

2. Design Requirements

Low-pass filters are commonly employed in signal processing applications to reduce noise and prevent aliasing. The OPA2140AIDR-HX are an excellent choice to construct high-speed, high-precision active filters.

Use the following parameters for this design example:

- Gain = 5 V/V (inverting gain)
- Low-pass cutoff frequency = 25 kHz
- Second-order Chebyshev filter response with 3-dB gain peaking in the pass band

2.1. Detailed Design Procedure

The infinite-gain multiple-feedback circuit for a low-pass network function is shown in. Use Equation 2 to calculate the voltage transfer function.

$$\frac{\text{Output}}{\text{Input}}(s) = \frac{-1/R_1R_3C_2C_5}{s^2 + (s/C_2)(1/R_1+1/R_3+1/R_4)+1/R_3R_4C_2C_5} \quad (2)$$

This circuit produces a signal inversion. For this circuit, the gain at DC and the low-pass cutoff frequency are calculated by Equation 3:

$$\text{Gain} = \frac{R_4}{R_1}$$

$$f_C = \frac{1}{2\pi}\sqrt{(1/R_3R_4C_2C_5)} \quad (3)$$

2.2. Application Curve

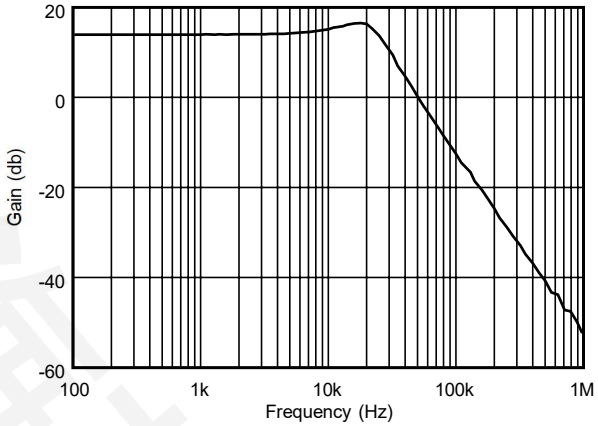


Figure 30. OPA2140AIDR-HX Second-Order, 25-kHz, Chebyshev, Low-Pass Filter

3. Power Supply Recommendations

The OPA2140AIDR-HX is specified for operation from 4.5 V to 36 V (±2.25 V to ±18 V); many specifications apply from –40°C to 125°C. Parameters that can exhibit significant variance with regard to operating voltage or temperature are presented in *Section 6*

CAUTION
Supply voltages larger than 40 V can permanently damage the device.

Place 0.1-µF bypass capacitors close to the power-supply pins to reduce errors coupling in from noisy or high-impedance power supplies. For more detailed information on bypass capacitor placement, see Application and Implementation *Section 4*.

4. Layout

4.1. Layout Guidelines

For best operational performance of the device, use good PCB layout practices, including:

- Noise can propagate into analog circuitry through the power pins of the circuit as a whole and op amp itself. Bypass capacitors are used to reduce the coupled noise by providing low-impedance power sources local to the analog circuitry.
  - Connect low-ESR, 0.1-µF ceramic bypass capacitors between each supply pin and ground, placed as close to the device as possible. A single bypass capacitor from V+ to ground is applicable for single-supply applications.
- Separate grounding for analog and digital portions of circuitry is one of the simplest and most-effective methods of noise suppression. One or more layers on multilayer PCBs are usually devoted to ground planes. A ground plane helps distribute heat and reduces EMI noise pickup. Make sure to physically separate digital and analog grounds paying attention to the flow of the ground current. For more detailed information.

- To reduce parasitic coupling, run the input traces as far away from the supply or output traces as possible. If these traces cannot be kept separate, crossing the sensitive trace perpendicular is much better as opposed to in parallel with the noisy trace.
- Place the external components as close to the device as possible.keeping RF and RG close to the inverting input minimizes parasitic capacitance.
- Keep the length of input traces as short as possible. Always remember that the input traces are the most sensitive part of the circuit.
- Consider a driven, low-impedance guard ring around the critical traces. A guard ring can significantly reduce leakage currents from nearby traces that are at different potentials.
- For best performance, recommends cleaning the PCB following board assembly.
- Any precision integrated circuit can experience performance shifts due to moisture ingress into the plastic package. Following any aqueous PCB cleaning process, recommends baking the PCB assembly to remove moisture introduced into the device packaging during the cleaning process. A low temperature, post cleaning bake at 85°C for 30 minutes is sufficient for most circumstances.

Device and Documentation Support

1. Filter Design Tool

The filter design tool is a simple, powerful, and easy-to-use active filter design program.

Available as a web-based tool from the Design tools and simulation web page, the filter design tool allows the user to design, optimize, and simulate complete multistage active filter solutions within minutes.

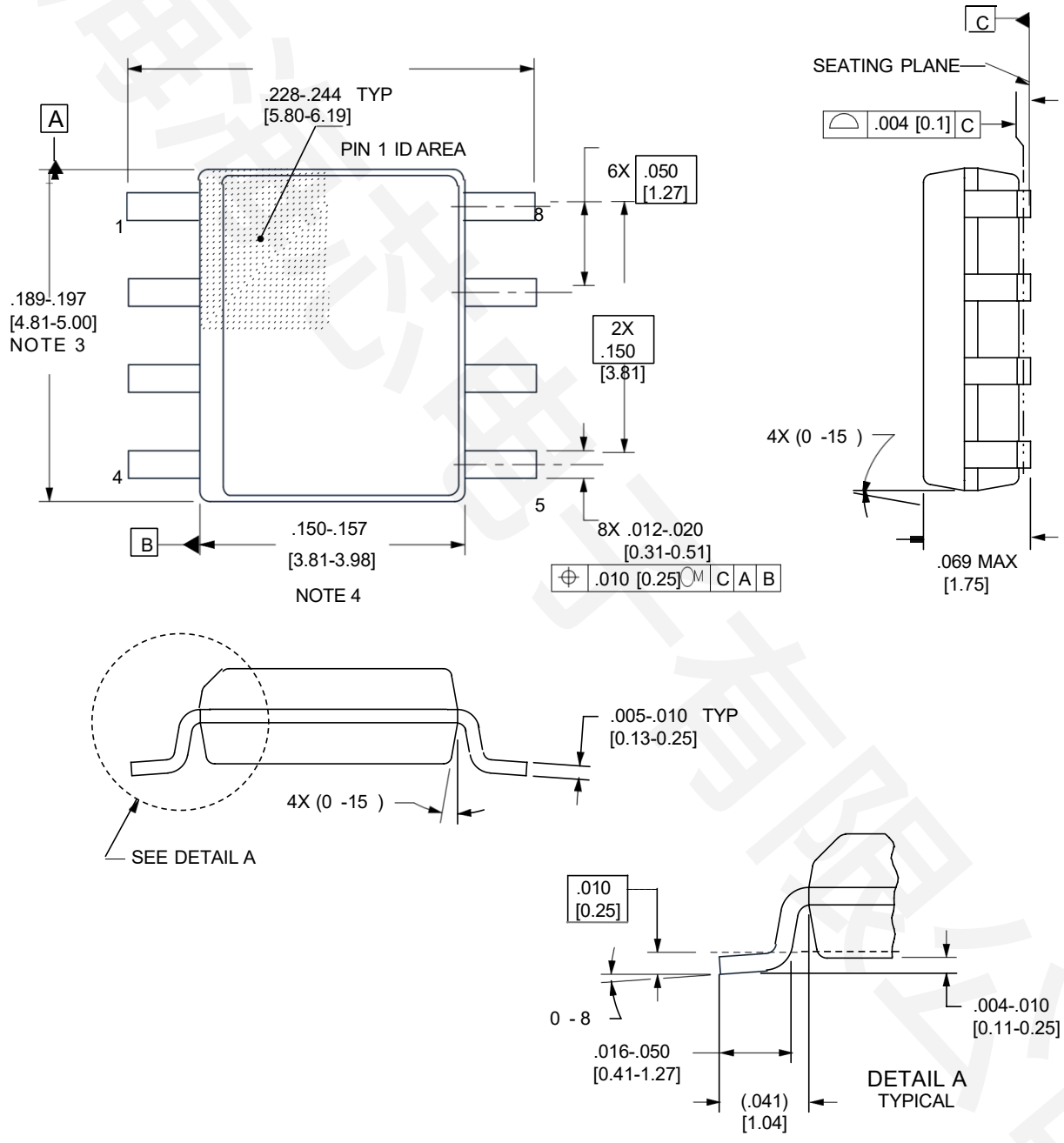
2. Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

PACKAGE OUTLINE

SOIC



NOTES:
1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.