74HC4020D-HX 14-stage binary ripple counter

Description

The 74HC4020D-HX is a 14-stage binary ripple counter featuring a clock input ($\overline{CP}$), an overriding asynchronous master reset input (MR), and 12 buffered parallel outputs (Q0, Q3 to Q13). The counter increments on the HIGH-to-LOW transition of the $\overline{CP}$. A HIGH signal on the MR input clears all stages of the counter and forces all outputs to LOW, regardless of the state of $\overline{CP}$. Each stage of the counter consists of a static toggle flip-flop. The inputs are equipped with clamp diodes, allowing for the use of current-limiting resistors to interface inputs with voltages exceeding V CC.

Featuresv

- ★ Wide supply voltage range from 2.0 V to 6.0 V
- ★ CMOS low power dissipation
- ★ High noise immunity
- ★ Latch-up performance exceeds 100 mA per JESD 78 Class II Level B
- ★ Complies with JEDEC standards:
  - JESD8C (2.7 V to 3.6 V)
  - JESD7A (2.0 V to 6.0 V)
- ★ Input levels:
  - For 74HC4020D-HX: CMOS level
- ★ ESD protection:
  - HBM: ANSI/ESDA/JEDEC JS-001 class 2 exceeds 2000 V
  - CDM: ANSI/ESDA/JEDEC JS-002 class C3 exceeds 1000 V
- ★ SO16 package
- ★ Specified from -40 °C to +85 °C and from -40 °C to +125 °C

Applications

- ★ Frequency dividing circuits
- ★ Time delay circuits
- ★ Control counters

Ordering information

Table 1. Ordering information

Type number	Package		
	Temperature range	Name	Description
74HC4020D-HX	-40 °C to +125 °C	SO16	plastic small outline package; 16 leads; body width 3.9 mm

Functional diagram

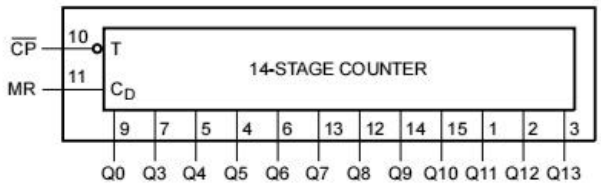


Fig. 1. Functional diagram

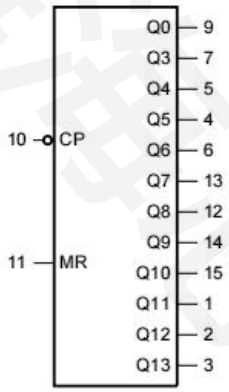


Fig. 2. Logic symbol

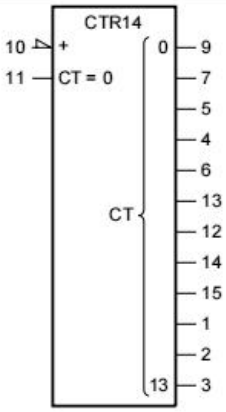


Fig. 3. IEC logic symbol

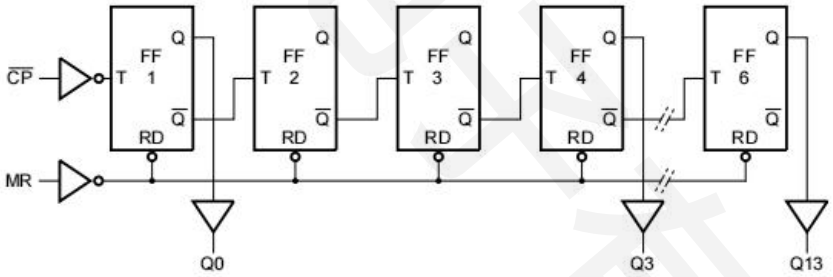
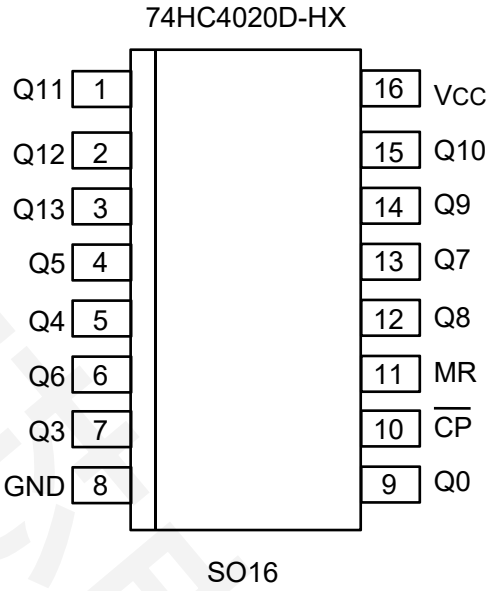


Fig. 4. Logic diagram

Pinning information

1. Pinning



(1) This is not a supply pin. There is no electrical or mechanical requirement to solder the pad. In case soldered, the solder land should remain floating or connected to V_{CC}.

2. Pin description

Table 2. Pin description

Symbol	Pin	Description
Q0, Q3 to Q13	9, 7, 5, 4, 6, 13, 12, 14, 15, 1, 2, 3	output
GND	8	ground (0 V)
$\overline{CP}$	10	clock input (HIGH-to-LOW, edge-triggered)
MR	11	master reset input (active HIGH)
V_{CC}	16	positive supply voltage

Functional description

Table 3. Function table

H = HIGH voltage level; L = LOW voltage level; X = don't care;
↑ = LOW-to-HIGH clock transition; ↓ = HIGH-to-LOW clock transition.

Input		Output
CP	MR	Q0, Q3 to Q13
↑	L	no change
↓	L	count
X	H	L

1. Timing diagram

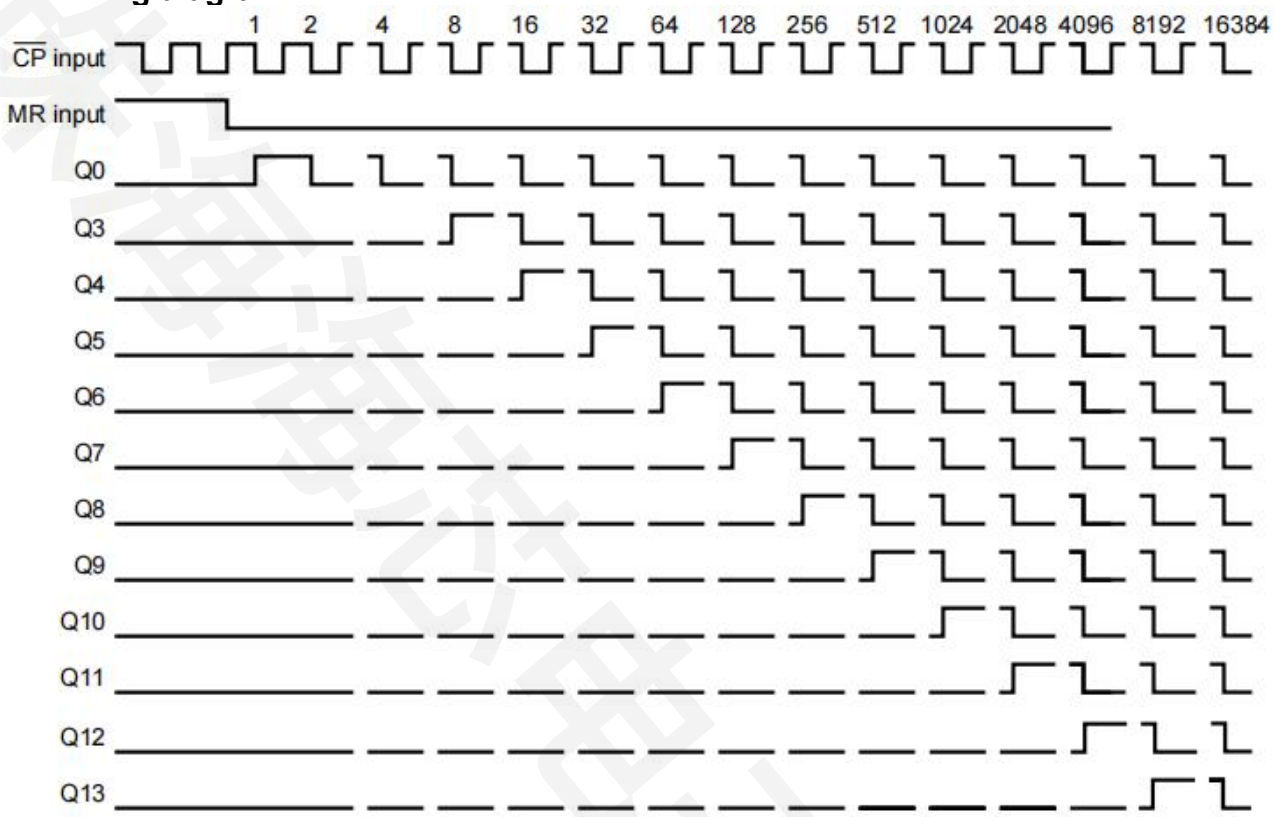


Fig. 5. Timing diagram

Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	supply voltage		-0.5	+7	V
I_{IK}	input clamping current	V_I < -0.5 V or V_I > V_{CC} + 0.5 V	-	±20	mA
I_{OK}	output clamping current	V_I < -0.5 V or V_I > V_{CC} + 0.5 V	-	±20	mA
I_O	output current	-0.5 V < V_O < V_{CC} + 0.5 V	-	±25	mA
I_{CC}	supply current		-	±50	mA
I_{GND}	ground current		-	±50	mA
T_{stg}	storage temperature		-65	+150	°C
P_{tot}	total power dissipation	T_{amb} = -40 °C to +125 °C [1]	-	500	mW

[1] For SO16 package: P_{tot} derates linearly with 12.4 mW/K above 110 °C.

Recommended operating conditions

Table 5. Recommended operating conditions

Symbol	Parameter	Conditions	74HC4020D-HX			Unit
			Min	Typ	Max	
V_{CC}	supply voltage		2.0	5.0	6.0	V
V_I	input voltage		0	-	V_{CC}	V
V_O	output voltage		0	-	V_{CC}	V
$\Delta t/\Delta V$	input transition rise and fall rate	except for Schmitt trigger inputs				
		V_{CC} = 2.0 V	-	-	625	ns/V
		V_{CC} = 4.5 V	-	1.67	139	ns/V
		V_{CC} = 6.0 V	-	-	83	ns/V
T_{amb}	ambient temperature		-40	+25	+125	°C

Static characteristics

Table 6. Static characteristics

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	25 °C			-40 °C to +85 °C		-40 °C to +125 °C		Unit
			Min	Typ	Max	Min	Max	Min	Max	
74HC4020D-HX										
V_{IH}	HIGH-level input voltage	V_{CC} = 2.0 V	1.5	1.2	-	1.5	-	1.5	-	V
		V_{CC} = 4.5 V	3.15	2.4	-	3.15	-	3.15	-	V
		V_{CC} = 6.0 V	4.2	3.2	-	4.2	-	4.2	-	V
V_{IL}	LOW-level input voltage	V_{CC} = 2.0 V	-	0.8	0.5	-	0.5	-	0.5	V
		V_{CC} = 4.5 V	-	2.1	1.35	-	1.35	-	1.35	V
		V_{CC} = 6.0 V	-	2.8	1.8	-	1.8	-	1.8	V
V_{OH}	HIGH-level output voltage	V_I = V_{IH} or V_{IL}								
		I_O = -20 μA; V_{CC} = 2.0 V	1.9	2.0	-	1.9	-	1.9	-	V
		I_O = -20 μA; V_{CC} = 4.5 V	4.4	4.5	-	4.4	-	4.4	-	V
		I_O = -20 μA; V_{CC} = 6.0 V	5.9	6.0	-	5.9	-	5.9	-	V
		I_O = -4.0 mA; V_{CC} = 4.5 V	3.98	4.32	-	3.84	-	3.7	-	V
		I_O = -5.2 mA; V_{CC} = 6.0 V	5.48	5.81	-	5.34	-	5.2	-	V
V_{OL}	LOW-level output voltage	V_I = V_{IH} or V_{IL}								
		I_O = 20 μA; V_{CC} = 2.0 V	-	0	0.1	-	0.1	-	0.1	V
		I_O = 20 μA; V_{CC} = 4.5 V	-	0	0.1	-	0.1	-	0.1	V
		I_O = 20 μA; V_{CC} = 6.0 V	-	0	0.1	-	0.1	-	0.1	V
		I_O = 4.0 mA; V_{CC} = 4.5 V	-	0.15	0.26	-	0.33	-	0.4	V
		I_O = 5.2 mA; V_{CC} = 6.0 V	-	0.16	0.26	-	0.33	-	0.4	V
I_I	input leakage current	V_I = Vcc or GND; V_{CC} = 6.0 V	-	-	±0.1	-	±1	-	±1	μA
I_{CC}	supply current	V_I = Vcc or GND; I_O = 0 A; V_{CC} = 6.0 V	-	-	8.0	-	80	-	160	μA
C_I	input capacitance		-	3.5	-	-	-	-	-	pF

Dynamic characteristics

Table 7. Dynamic characteristics

GND (ground = 0 V); C_L = 50 pF unless otherwise specified; for test circuit, see Fig. 8

Symbol	Parameter	Conditions	25 °C			-40 °C to +85 °C		-40 °C to +125 °C		Unit
			Min	Typ	Max	Min	Max	Min	Max	
74HC4020D-HX										
t_{pd}	propagation delay	CP to Q0; see Fig. 6 [1]								
		V_{CC} = 2.0 V	-	39	140	-	175	-	210	ns
		V_{CC} = 4.5 V	-	14	28	-	35	-	42	ns
		V_{CC} = 5.0 V; C_L = 15 pF	-	11	-	-	-	-	-	ns
		V_{CC} = 6.0 V	-	11	24	-	30	-	36	ns
		Qn to Qn+1; see Fig. 7								
		V_{CC} = 2.0 V	-	22	75	-	95	-	110	ns
		V_{CC} = 4.5 V	-	8	15	-	19	-	22	ns
		V_{CC} = 5.0 V; C_L = 15 pF	-	6	-	-	-	-	-	ns
		V_{CC} = 6.0 V	-	6	13	-	16	-	19	ns
t_{PHL}	HIGH to LOW propagation delay	MR to Qn; see Fig. 6								
		V_{CC} = 2.0 V	-	55	170	-	215	-	225	ns
		V_{CC} = 4.5 V	-	20	34	-	43	-	51	ns
		V_{CC} = 5.0 V; C_L = 15 pF	-	17	-	-	-	-	-	ns
		V_{CC} = 6.0 V	-	16	29	-	37	-	43	ns
t_t	transition time	Qn; see Fig. 6 [2]								
		V_{CC} = 2.0 V	-	19	75	-	95	-	110	ns
		V_{CC} = 4.5 V	-	7	15	-	19	-	22	ns
		V_{CC} = 6.0 V	-	6	13	-	16	-	19	ns
t_W	pulse width	CP HIGH or LOW; see Fig. 6								
		V_{CC} = 2.0 V	80	14	-	100	-	120	-	ns
		V_{CC} = 4.5 V	16	4	-	20	-	24	-	ns
		V_{CC} = 6.0 V	14	3	-	17	-	20	-	ns
		MR HIGH; see Fig. 6								
		V_{CC} = 2.0 V	80	17	-	100	-	120	-	ns
		V_{CC} = 4.5 V	16	6	-	20	-	24	-	ns
		V_{CC} = 6.0 V	14	5	-	17	-	20	-	ns
t_{rec}	recovery time	MR to $\overline{CP}$; see Fig. 6								
		V_{CC} = 2.0 V	50	6	-	65	-	75	-	ns
		V_{CC} = 4.5 V	10	2	-	13	-	15	-	ns
		V_{CC} = 6.0 V	9	2	-	11	-	13	-	ns
f_{max}	maximum frequency	see Fig. 6								
		V_{CC} = 2.0 V	6.0	30	-	4.8	-	4.0	-	MHz
		V_{CC} = 4.5 V	30	92	-	24	-	20	-	MHz
		V_{CC} = 5.0 V; C_L = 15 pF	-	101	-	-	-	-	-	MHz
		V_{CC} = 6.0 V	35	109	-	28	-	24	-	MHz
C_{PD}	power dissipation capacitance	[3]	-	19	-	-	-	-	-	pF

[1] t_{pd} is the same as t_{PHL} and t_{PLH}.

[2] t_t is the same as t_{THL} and t_{TLH}.

[3] C_{PD} is used to determine the dynamic power dissipation (P_D in µW).

$P_D = C_{PD} \times V_{CC}^2 \times f_i + \Sigma (C_L \times V_{CC}^2 \times f_o)$ where:

f_i = input frequency in MHz;

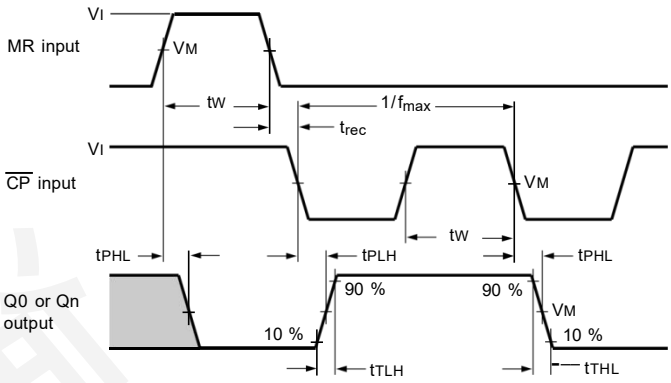
f_o = output frequency in MHz;

$\Sigma (C_L \times V_{CC}^2 \times f_o)$ = sum of outputs;

C_L = output load capacitance in pF;

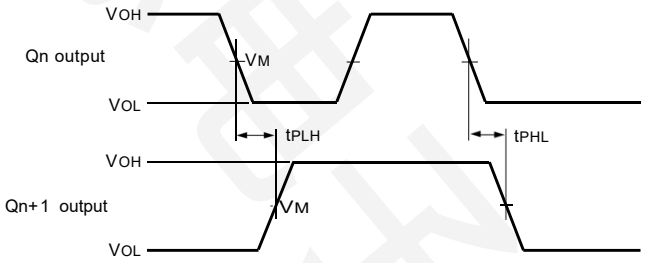
V_{CC} = supply voltage in V.

Waveforms and test circuit



Measurement points are given in Table 8.
V_{OL} and V_{OH} are typical voltage output levels that occur with the output load.

Fig. 6. Clock timing, propagation delays and pulse widths

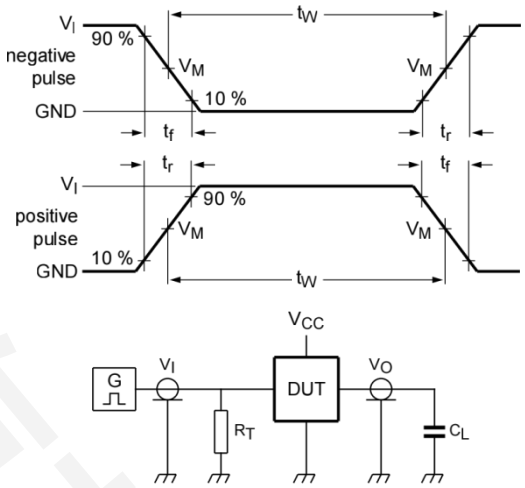


Measurement points are given in Table 8.
V_{OL} and V_{OH} are typical voltage output levels that occur with the output load.

Fig. 7. Waveforms showing the output Qn to output Qn+1 propagation delays

Table 8. Measurement points

Type	Input	Output
	V_M	V_M
74HC4020D-HX	0.5 × V_{CC}	0.5 × V_{CC}



Test data is given in Table 9.

Definitions test circuit:

R_T = Termination resistance should be equal to output impedance Z_o of the pulse generator;

C_L = Load capacitance including jig and probe capacitance.

Fig. 8. Test circuit for measuring switching times

Table 9. Test data

Type	Input		Load
	V_I	t_r, t_f	C_L
74HC4020D-HX	V_{CC}	6 ns	15 pF, 50 pF

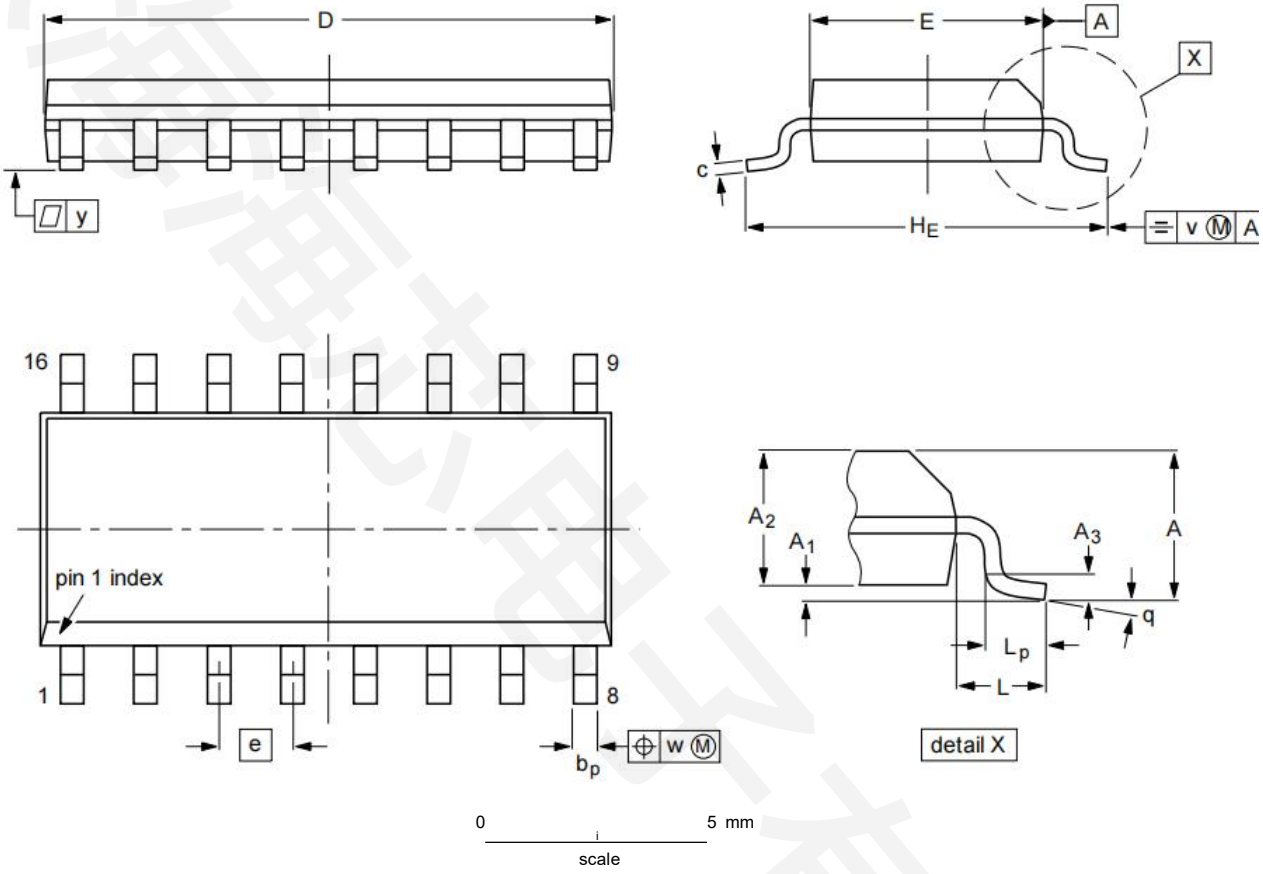
Abbreviations

Table 10. Abbreviations

Acronym	Description
CDM	Charged Device Model
CMOS	Complementary Metal Oxide Semiconductor
DUT	Device Under Test
ESD	ElectroStatic Discharge
HBM	Human Body Model
TTL	Transistor-Transistor Logic

Package outline

SO16



Dimensions (inch dimensions are derived from the original mm dimensions)

Unit		A	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_E	L	L_p	v	w	y	θ
mm	max	1.75	0.25		0.25	0.51	0.25	10.0	4.0	1.27	6.2	1.05	1.27	0.2	0.25	0.1	8°
	nom			1.25													
	min		0.10			0.31	0.10	9.8	3.8		5.8		0.4				0°
inches	max	0.069	0.010		0.01	0.020	0.010	0.394	0.16	0.05	0.244	0.041	0.05	0.008	0.01	0.004	8°
	nom			0.049													
	min		0.004			0.012	0.004	0.386	0.15		0.228		0.016				0°

Fig. 9. Package outline SO16