

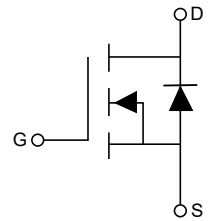
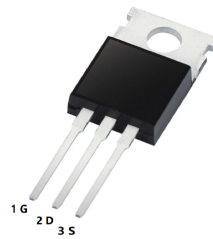
1.Features

- $V_{DS(V)}=40V$
- $I_D=75A$
- $R_{DS(ON)}<2m\Omega(V_{GS}=10V)$
- $R_{DS(ON)}<2.3m\Omega(V_{GS}=4.5V)$

2.Pinning information

Pin	Symbol	Description
1	G	GATE
2	D	DRAIN
3	S	SOURCE

TO-220



3.Absolute Maximum Ratings

Parameter		Symbol	Rating	Units
Continuous Drain Current, $V_{GS}=10V$ (Silicon Limited)	$T_C=25^{\circ}C$	I_D	270	A
Continuous Drain Current, $V_{GS}=10V$ (See Fig. 9)	$T_C=100^{\circ}C$		190	A
Continuous Drain Current, $V_{GS}=10V$ (Package Limited)	$T_C=25^{\circ}C$		75	A
Pulsed Drain Current ①		I_{DM}	1080	A
Maximum Power Dissipation	$T_C=25^{\circ}C$	P_D	300	W
Linear Derating Factor			2	W/ $^{\circ}C$
Gate-to-Source Voltage		V_{GS}	± 20	V
Single Pulse Avalanche Energy (Thermally Limited) ②		E_{AS}	540	mJ
Single Pulse Avalanche Energy Tested Value ⑦		$E_{AS(tested)}$	1160	mJ
Avalanche Current ①		I_{AR}	See Fig.14a, 14b,16,17	A
Repetitive Avalanche Energy ⑥		E_{AR}		mJ
Storage Temperature Range		T_J, T_{STG}	-55 to 175	$^{\circ}C$
Soldering Temperature, for 10 seconds			300(1.6mm from case)	$^{\circ}C$
Mounting torque, 6-32 or M3 screw			10 lbf•in (1.1N•m)	



4.Thermal resistance rating

Parameter	Symbol	Typ	Max	Units
Junction-to-Case	$R_{\theta JC}$		0.5 ^⑩	°C/W
Case-to-Sink, Flat Greased Surface	$R_{\theta CS}$	0.5		°C/W
Junction-to-Ambient	$R_{\theta JA}$		62	°C/W
Junction-to-Ambient (PCB Mount, steady state) ^⑧	$R_{\theta JA}$		40	°C/W



5. Electrical Characteristics @ $T_J = 25^\circ\text{C}$ (unless otherwise specified)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Drain-to-Source Breakdown Voltage	$V_{(BR)DSS}$	$I_D=250\mu\text{A}$, $V_{GS}=0\text{V}$	40			V
Breakdown Voltage Temp. Coefficient	$\Delta V_{(BR)DSS}/\Delta T_J$	$I_D=1\text{mA}$, Reference to 25°C		0.031		$\text{V}/^\circ\text{C}$
Static Drain-to-Source On-Resistance	$R_{DS(ON)}$	$V_{GS}=10\text{V}$, $I_D=75\text{A}$ ④		1.5	2	$\text{m}\Omega$
Static Drain-to-Source On-Resistance	$R_{DS(ON)}$	$V_{GS}=10\text{V}$, $I_D=75\text{A}$ ④		1.8	2.3	$\text{m}\Omega$
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS}=V_{GS}$, $I_D=250\mu\text{A}$	2		4	V
Forward Transconductance	g_{FS}	$V_{DS}=10\text{V}$, $I_D=75\text{A}$	130			S
Drain-to-Source Leakage Current	I_{DSS}	$V_{DS}=40\text{V}$, $V_{GS}=0\text{V}$			20	μA
		$V_{DS}=40\text{V}$, $V_{GS}=0\text{V}$, $T_J=125^\circ\text{C}$			250	μA
Gate-to-Source Forward Leakage	I_{GSS}	$V_{GS}=20\text{V}$			200	nA
Gate-to-Source Reverse Leakage		$V_{GS}=-20\text{V}$			-200	nA
Total Gate Charge	Q_g	$I_D=75\text{A}$, $V_{DS}=32\text{V}$, $V_{GS}=10\text{V}$ ④		160	240	nC
Gate-to-Source Charge	Q_{gs}			41	62	nC
Gate-to-Drain ("Miller") Charge	Q_{gd}			66	99	nC
Turn-On Delay Time	$t_{D(on)}$	$V_{DD}=20\text{V}$, $I_D=75\text{A}$ $R_G=2.5\Omega$, $V_{GS}=10\text{V}$ ④		13		ns
Rise Time	t_r			120		ns
Turn-Off Delay Time	$t_{D(off)}$			130		ns
Fall Time	t_f			130		ns
Internal Drain Inductance	L_D	Between lead, 6mm (0.25in.) from package and center of die contact		4.5		nH
Internal Source Inductance	L_S			7.5		
Input Capacitance	C_{iss}	$V_{GS}=0\text{V}$, $V_{DS}=25\text{V}$, $f=1.0\text{MHz}$ See Fig. 5		6450		pF
Output Capacitance	C_{oss}			1690		pF
Reverse Transfer Capacitance	C_{rss}			840		pF
Output Capacitance	C_{oss}	$V_{GS}=0\text{V}$, $V_{DS}=1\text{V}$, $f=1\text{MHz}$		5350		pF
Output Capacitance	C_{oss}	$V_{GS}=0\text{V}$, $V_{DS}=32\text{V}$, $f=1\text{MHz}$		1520		pF
Effective Output Capacitance	$C_{oss\text{eff.}}(\text{ER})$	$V_{GS}=0\text{V}$, $V_{DS}=0\text{V to } 32\text{V}$		2210		pF



Diode Characteristics						
Continuous Source Current (Body Diode)	I_S	MOSFET symbol showing the integral reverse p-n junction diode.			270	A
Pulsed Source Current (Body Diode) ①	I_{SM}				1080	A
Diode Forward Voltage	V_{SD}	$T_J=25^\circ\text{C}, I_S=75\text{A}, V_{GS}=0\text{V}$ ④			1.3	V
Reverse Recovery Time	t_{rr}	$T_J=25^\circ\text{C}, I_S=75\text{A}, V_{DD}=20\text{V}$ $di/dt=100\text{A}/\mu\text{s}$ ④		56	84	ns
Reverse Recovery Charge	Q_{rr}			67	100	nC
Forward Turn-On Time	t_{on}	Intrinsic turn-on time is negligible (turn-on is dominated by L_S+L_D)				

Notes:

- ① Repetitive rating; pulse width limited by max. junction temperature.(See fig. 11).
- ② Limited by T_{Jmax} , starting $T_J=25^\circ\text{C}$, $L=0.24\text{mH}$, $R_G=25\Omega$, $I_{AS}=75\text{A}$, $V_{GS}=10\text{V}$.Part not recommended for use above this value.
- ③ $I_{SD} \leq 75\text{A}$, $di/dt \leq 220\text{A}/\mu\text{s}$, $V_{DD} \leq V_{(BR)DSS}$, $T_J \leq 175^\circ\text{C}$.
- ④ Pulse width $\leq 1\text{ms}$; duty cycle $\leq 2\%$.
- ⑤ C_{oss} eff. is a fixed capacitance that gives the same charging time as C_{oss} while V_{DS} is rising from 0 to 80% V_{DSS} .
- ⑥ Limited by T_{Jmax} , see Fig.12a, 12b, 15, 16 for typical repetitive avalanche performance.
- ⑦ This value determined from sample failure population. 100% tested to this value in production.
- ⑧ This is applied to D² Pak, when mounted on 1" square PCB (FR-4 or G-10 Material). For recommended footprint and soldering techniques refer to application note #AN-994.
- ⑨ Max $R_{DS(ON)}$ for D2Pak and TO-262 (SMD) devices.
- ⑩ TO-220 device will have an R_{th} value of $0.45^\circ\text{C}/\text{W}$.



6.1 Typical Characteristics

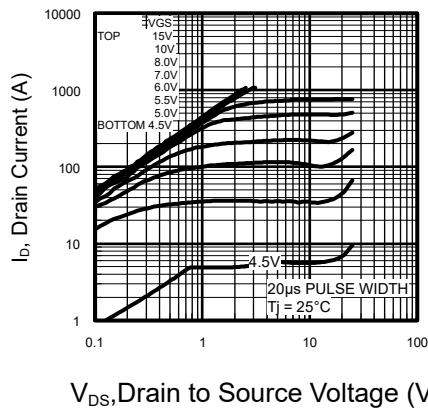


Figure 1: Typical Output Characteristics

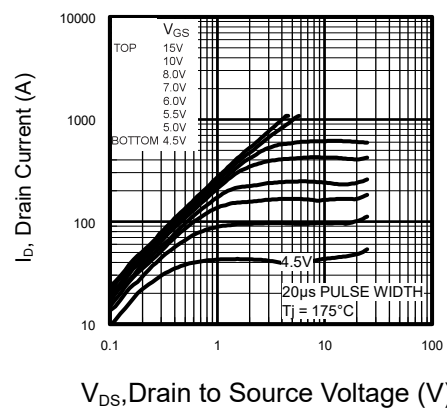


Figure 2: Typical Output Characteristics

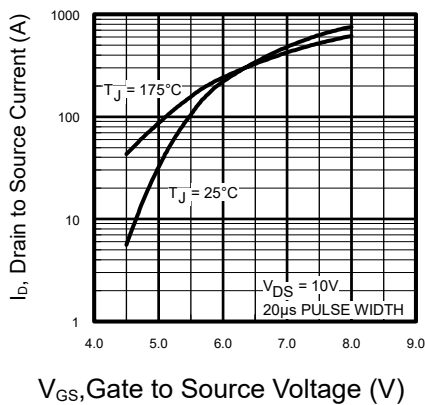


Figure 3: Typical Transfer Characteristics

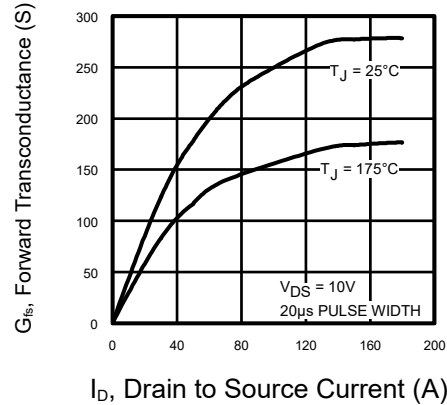


Figure 4: Typical Forward Transconductance vs. Drain Current

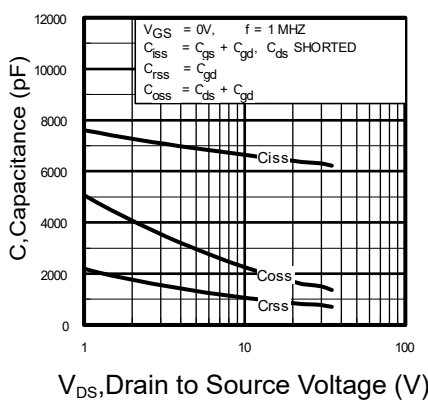


Figure 5: Typical Capacitance vs. Drain-to-Source Voltage

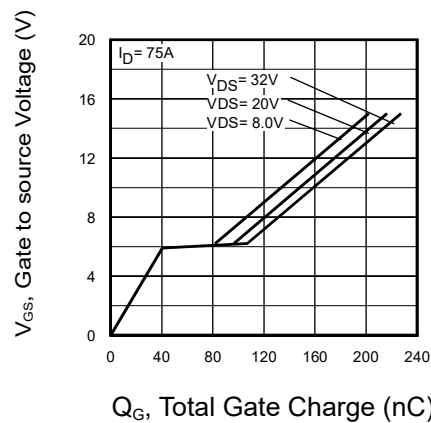


Figure 6: Typical Gate Charge vs. Gate-to-Source Voltage



6.2 Typical Characteristics

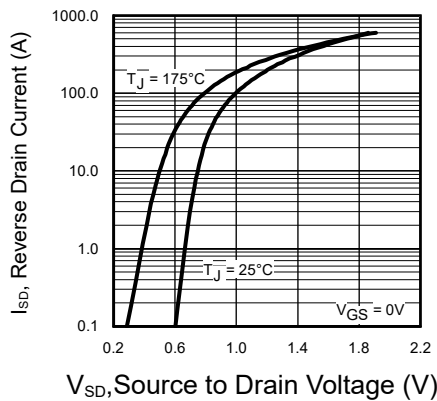


Figure 7: Typical Source-Drain Diode Forward Voltage

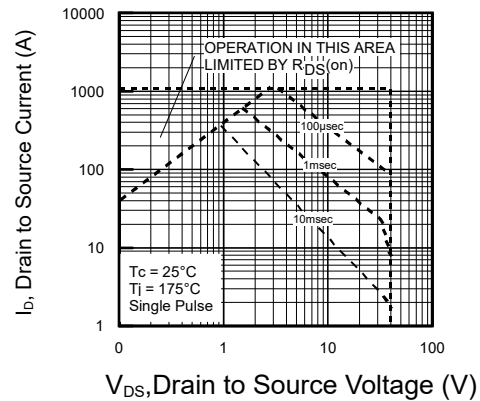


Figure 8: Maximum Safe Operating Area

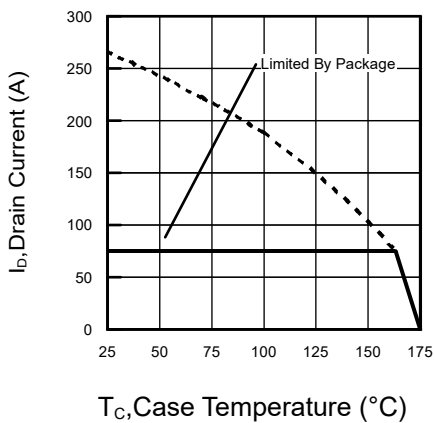


Figure 9: Maximum Drain Current vs. Case Temperature

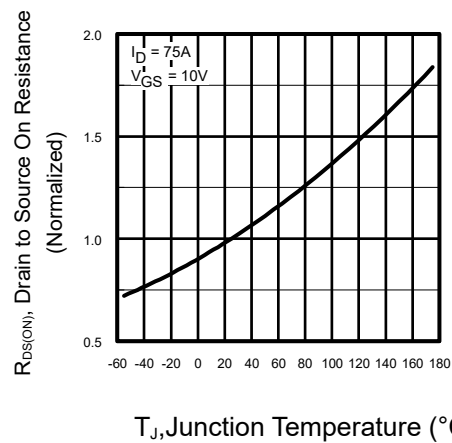


Figure 10: Drain-to-Source Breakdown Voltage

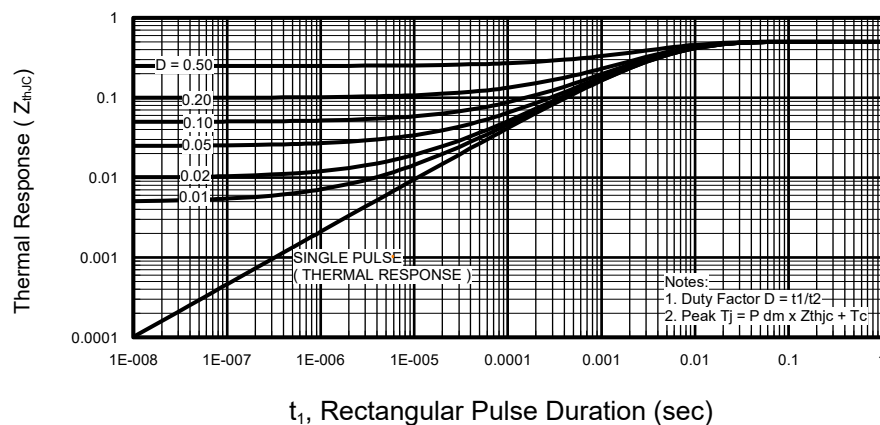


Figure 11: Maximum Effective Transient Thermal Impedance, Junction-to-Case



6.3 Typical Characteristics

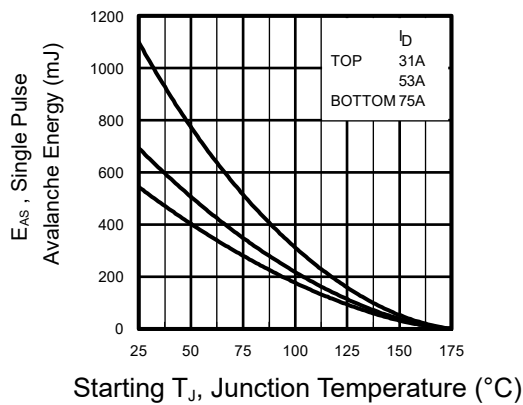


Figure 12: Maximum Avalanche Energy vs. Drain Current

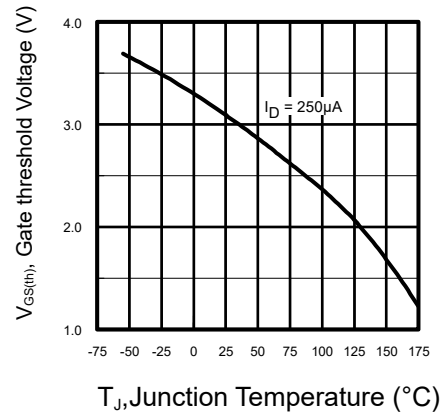


Figure 13: Threshold Voltage vs. Temperature

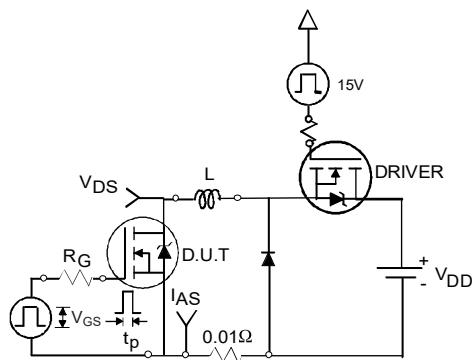


Figure 14a: Unclamped Inductive Test Circuit

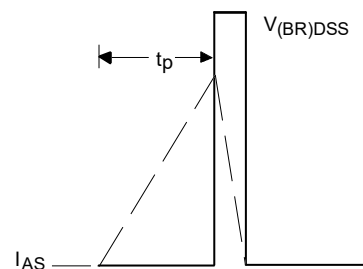


Figure 14b: Unclamped Inductive Waveforms

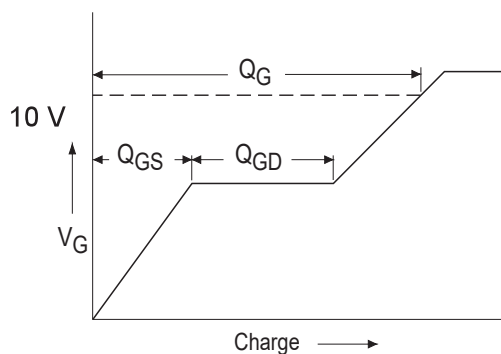


Figure 15a: Basic Gate Charge Waveform

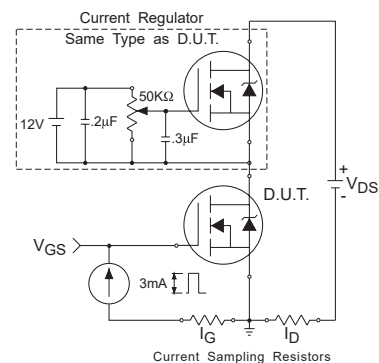
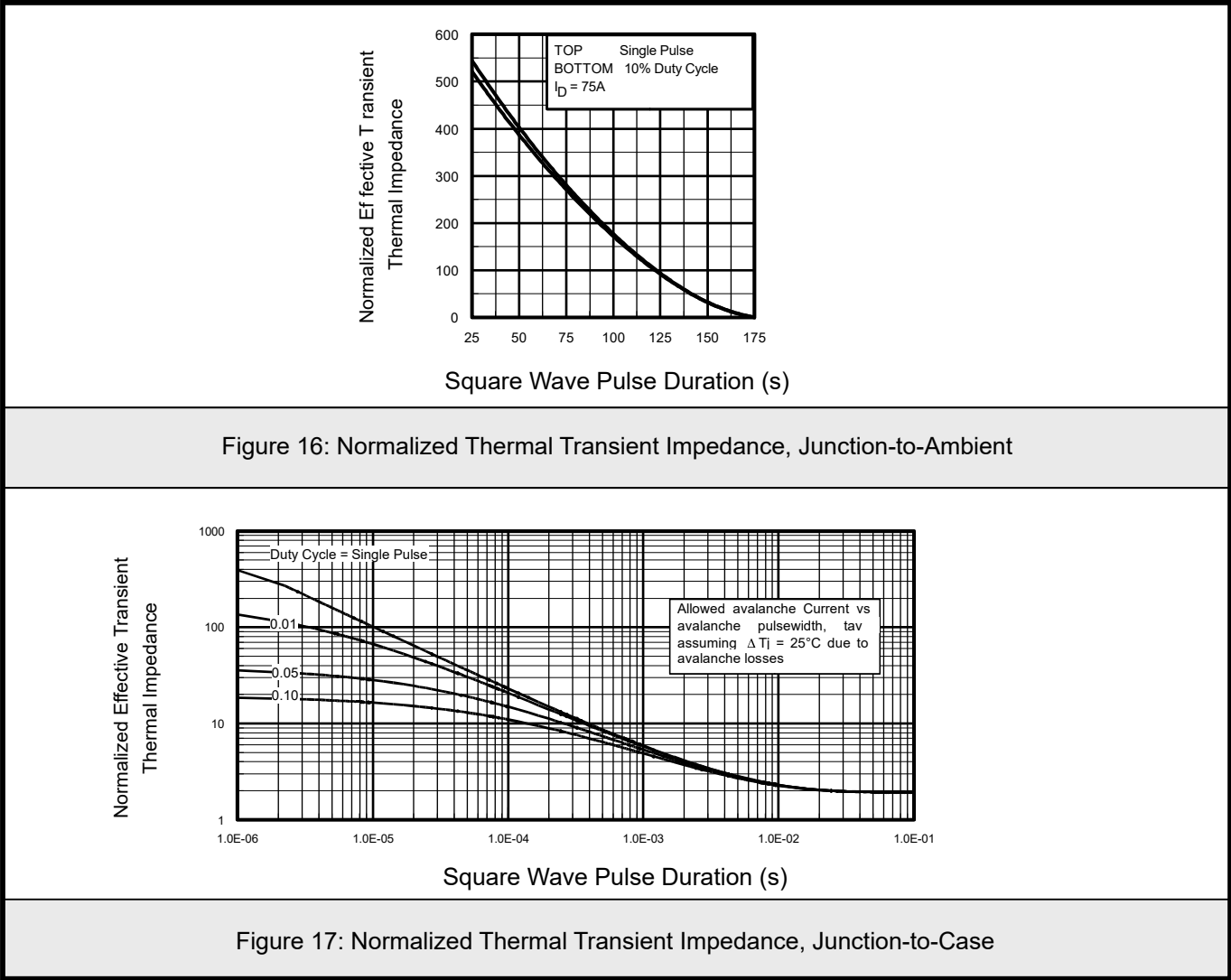


Figure 15b: Gate Charge Test Circuit



6.4Typical Characteristics





Notes:

1. Avalanche failures assumption: Purely a thermal phenomenon and failure occurs at a temperature far in excess of T_{jmax} .

This is validated for every part type.

2. Safe operation in Avalanche is allowed as long as T_{jmax} is not exceeded.

3. Equation below based on circuit and waveforms shown in Figures 14a, 14b.

4. $P_{D(ave)}$ = Average power dissipation per single avalanche pulse.

5. BV = Rated breakdown voltage (1.3 factor accounts for voltage increase during avalanche).

6. I_{av} = Allowable avalanche current.

7. ΔT = Allowable rise in junction temperature, not to exceed

T_{jmax} (assumed as 25°C in Figure 16,17).

t_{av} = Average time in avalanche.

D = Duty cycle in avalanche = $t_{av} \cdot f$

$Z_{thJC}(D, t_{av})$ = Transient thermal resistance, see figure 11).

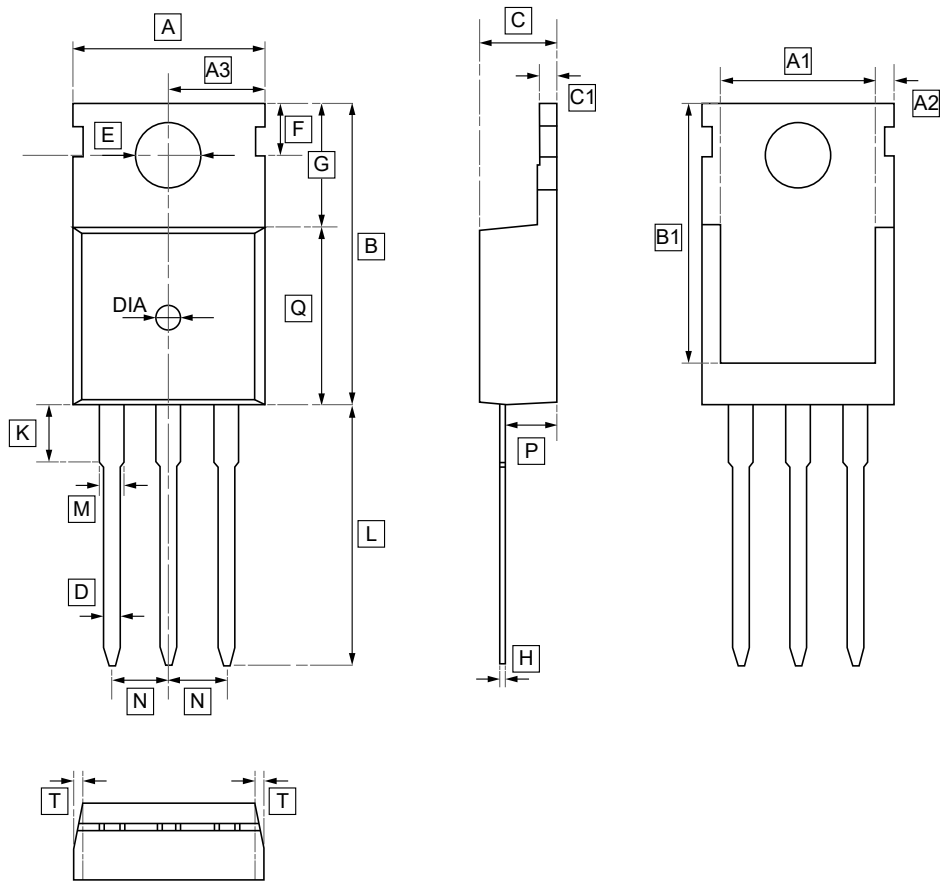
$$P_{D(ave)} = 1/2 (1.3 \cdot BV \cdot I_{av}) = \Delta T / Z_{thJC}$$

$$I_{av} = 2\Delta T / [1.3 \cdot BV \cdot Z_{th}]$$

$$E_{AS(AR)} = P_{D(ave)} \cdot t_{av}$$



7.1 TO-220 Package Outline Dimensions



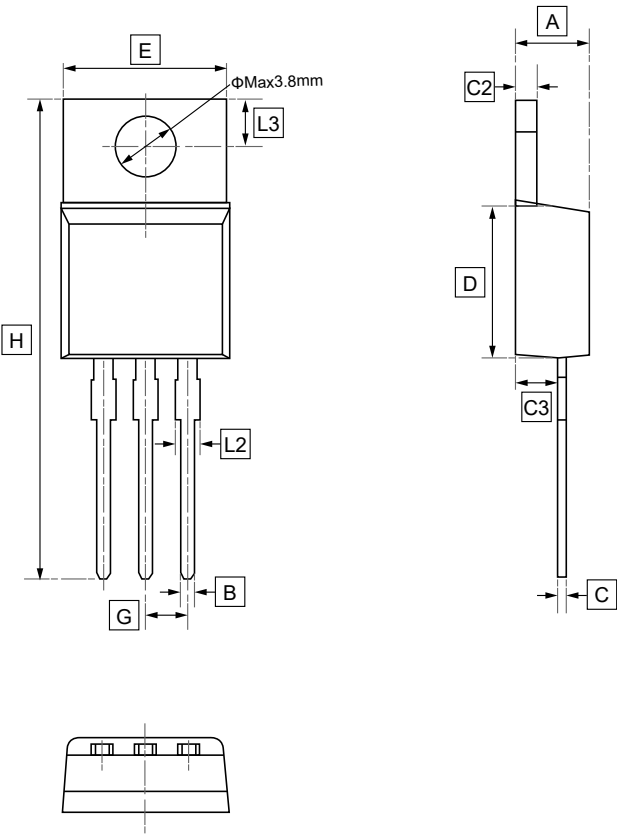
DIMENSIONS (mm are the original dimensions)

Symbol	A	A1	A2	A3	B	B1	C	C1	D	E	F	G
Min	9.7	8.44	1.05	4.8	15.4	12.9	4.28	1.1	0.6	3.4	2.65	5.2
Max	10.3	8.84	1.25	5.2	16.2	13.5	4.68	1.5	1.0	3.8	3.25	5.8

Symbol	H	K	L	L1	M	N	P	Q	T	DIA
Min	0.4	2.9	12.8	2.7	1.15	2.49	2.1	8.7	W:0.35	⌀1.5
Max	0.6	3.3	13.6	3.3	1.35	2.59	2.7	9.3		(deep 0.2)



7.2 TO-220 Package Outline Dimensions

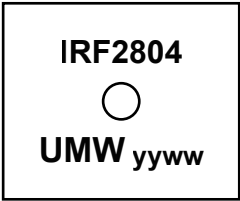


DIMENSIONS (mm are the original dimensions)

Symbol	A	B	C	C2	C3	D	E	G	H	L2	L3
Min	4.30	0.60	0.28	1.17	2.30	8.80	9.80	2.44	28.55	1.10	2.59
Max	4.70	1.00	0.48	1.37	2.70	9.20	10.20	2.64	29.15	1.50	2.89



8.Ordering Information



yy: Year Code
ww: Week Code

Order Code	Package	Base QTY	Delivery Mode
UMW IRF2804PBF	TO-220	1000	Tube and box



9.Disclaimer

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