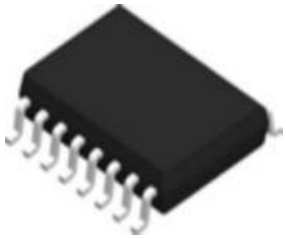
SN74HC595DR-HX Bit Shift Registers With 3-State Output Registers

Description

The SN74HC595DR-HX devices feature an 8-bit serial-in, parallel-out shift register that feeds into an 8-bit D-type storage register. This storage register is equipped with parallel three-state outputs. Distinct clock signals are provided for both the shift and storage registers. The shift register includes a direct overriding clear ($\overline{SRCLR}$) input, a serial (SER) input, and serial outputs for cascading purposes. When the output-enable ($\overline{OE}$) input is set to high, the outputs enter a high-impedance state.

Features



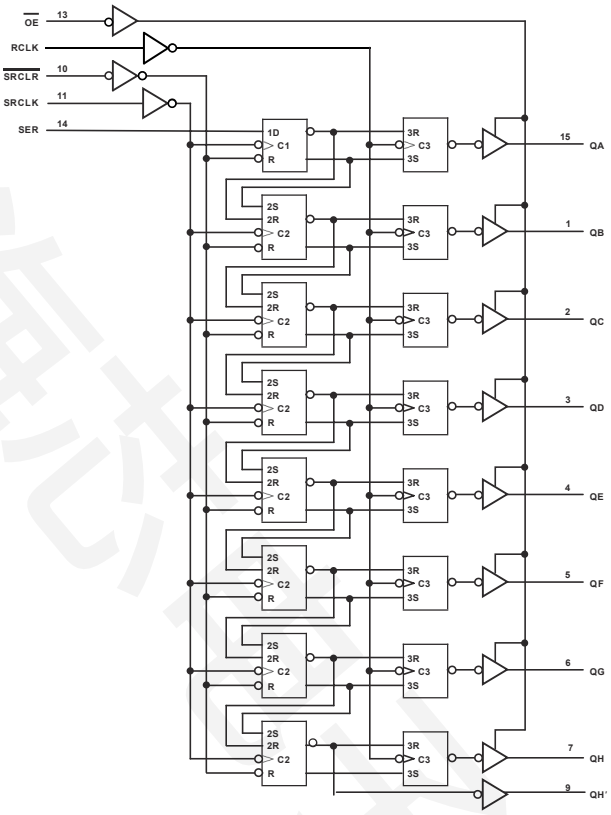
SOIC-16

- 8-bit serial-in, parallel-out shift
- Wide operating voltage range of 2 V to 6 V
- High-current 3-state outputs can drive up to 15 LSTTL loads
- Low power consumption: 80-μA (maximum) I_{CC}
- t_{pd} = 13 ns (typical)
- ±6-mA output drive at 5 V
- Low input current: 1 μA (maximum)
- Shift register has direct clear
- On products compliant to MIL-PRF-38535,all parameters are tested unless otherwise noted. On all other products, production processing does not necessarily include testing of all parameters.

Applications

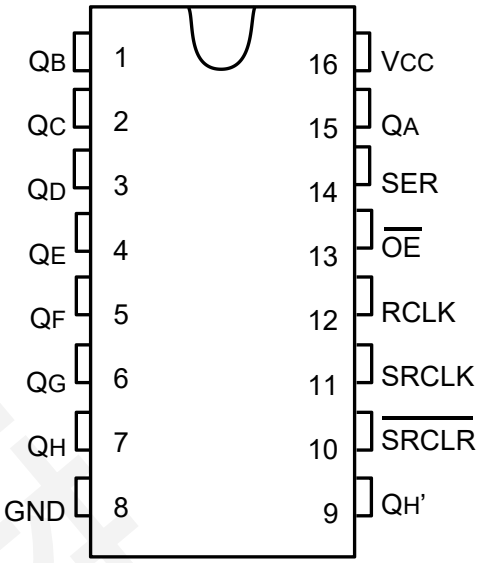
- Network switches
- Power infrastructure
- LED displays
- Servers

(1) For all available packages, see the orderable addendum at the end of the data sheet.



Functional Block Diagram

Pin Configuration and Functions



16-Pin SOIC Packsge Top View

Pin Functions

PIN			I/O(1)	DESCRIPTION
NAME	SOIC	LCCC		
GND	8	10	—	Ground Pin
$\overline{OE}$	13	17	I	Output Enable
Q_A	15	19	O	Q_A Output
Q_B	1	2	O	Q_B Output
Q_C	2	3	O	Q_C Output
Q_D	3	4	O	Q_D Output
Q_E	4	5	O	Q_E Output
Q_F	5	7	O	Q_F Output
Q_G	6	8	O	Q_G Output
Q_H	7	9	O	Q_H Output
$Q_{H'}$	9	12	O	$Q_{H'}$ Output
RCLK	12	14	I	RCLK Input
SER	14	18	I	SER Input
SRCLK	11	14	I	SRCLK Input
$\overline{SRCLR}$	10	13	I	$\overline{SRCLR}$ Input
NC	—	1	—	No Connection
		16		
		11		
		16		
V_{CC}	—	20	—	Power Pin

(1) Signal Types: I = Input, O = Output, I/O = Input or Output.

Specifications

1. Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

			MIN	MAX	UNIT
V_{CC}	Supply voltage		–0.5	7	V
I_{IK}	Input clamp current(2)	$V_I < 0$ or $V_I > V_{CC}$		±20	mA
I_{OK}	Output clamp current (2)	$V_O < 0$ or $V_O > V_{CC}$		±20	mA
I_O	Continuous output current	$V_O = 0$ to V_{CC}		±35	mA
	Continuous current through V_{CC} or GND			±70	mA
T_J	Junction temperature			150	°C
T_{stg}	Storage temperature		–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

(2) The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

2. ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	2000	V
		Charged device model (CDM), per ANSI/ESDA/JEDEC JS-002(2)	1000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

3. Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)(1)

			SN74HC595DR-HX			UNIT
			MIN	NOM	MAX	
V_{CC}	Supply voltage		2	5	6	V
V_{IH}	High-level input voltage	V_{CC} = 2 V	1.5			V
		V_{CC} = 4.5 V	3.15			
		V_{CC} = 6 V	4.2			
V_{IL}	Low-level input voltage	V_{CC} = 2 V			0.5	V
		V_{CC} = 4.5 V			1.35	
		V_{CC} = 6 V			1.8	
V_I	Input voltage		0		V_{CC}	V
V_O	Output voltage		0		V_{CC}	V
$\Delta t/\Delta v$	Input transition rise or fall time(2)	V_{CC} = 2 V			1000	ns
		V_{CC} = 4.5 V			500	
		V_{CC} = 6 V			400	
T_A	Operating free-air temperature		–40		85	°C

(1) All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation.

(2) If this device is used in the threshold region (from V_{IL}max = 0.5 V to V_{IH} min = 1.5 V), there is a potential to go into the wrong state from induced grounding, causing double clocking. Operating with the inputs at t_t = 1000 ns and V_{CC} = 2 V does not damage the device; however, functionally, the CLK inputs are not ensured while in the shift, count, or toggle operating modes.

4. Thermal Information

THERMAL METRIC(1)		SN74HC595DR-HX SOIC 16 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	57	°C/W

(1) For more information about traditional and new thermal metrics.

5. Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

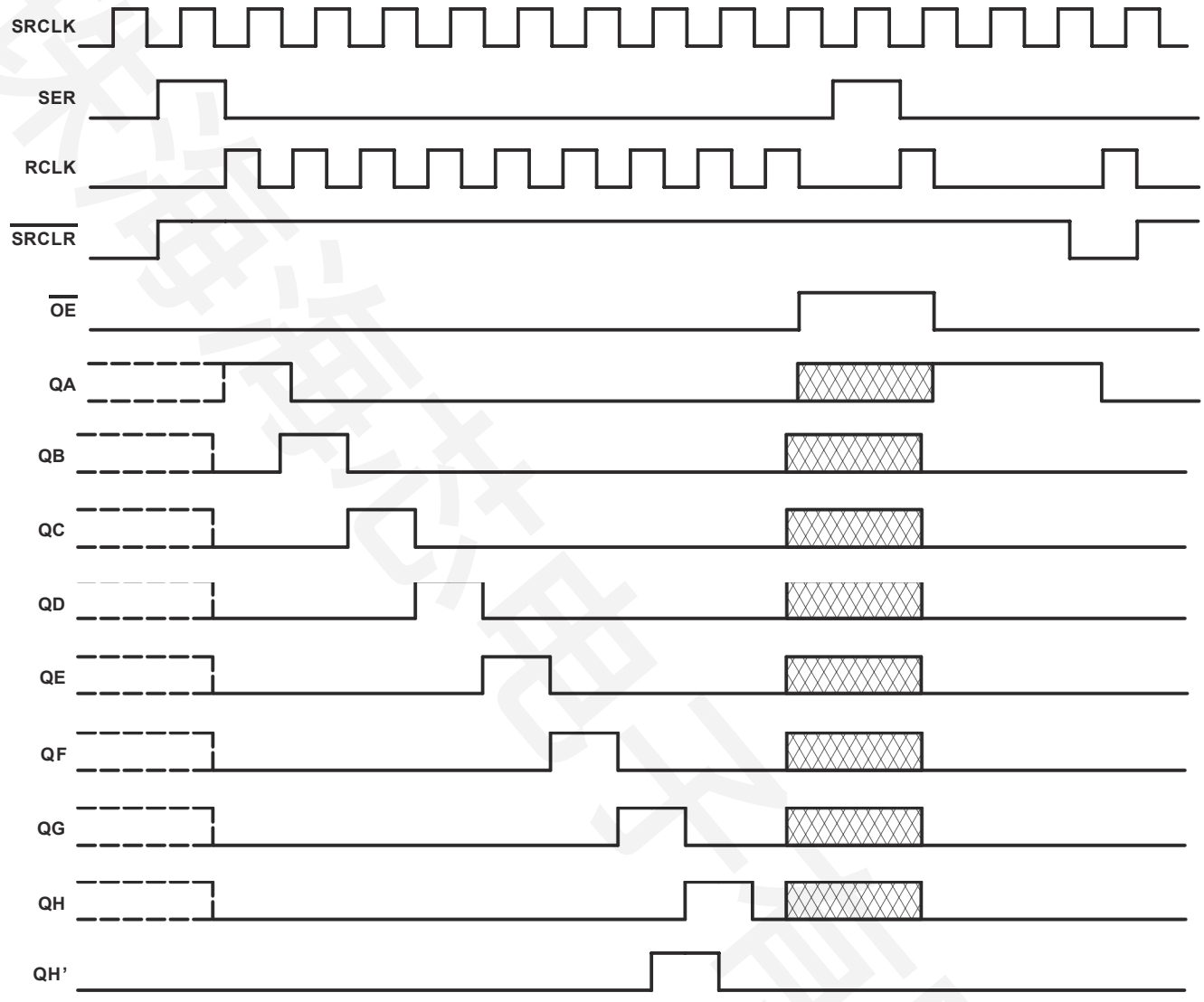
PARAMETER	TEST CONDITIONS		V_{CC}	T_A = 25°C			SN74HC595DR-HX		UNIT
				MIN	TYP	MAX	MIN	MAX	
V_{OH}	V_I = V_{IH} or V_{IL}	I_{OH} = –20 μA	2 V	1.9	1.998		1.9		V
			4.5 V	4.4	4.499		4.4		
			6 V	5.9	5.999		5.9		
		$Q_{H'}$, I_{OH} = –4 mA	4.5 V	3.98	4.3		3.84		
		Q_A – Q_H, I_{OH} = –6 mA		3.98	4.3		3.84		
		$Q_{H'}$, I_{OH} = –5.2 mA	6 V	5.48	5.8		5.34		
		Q_A – Q_H, I_{OH} = –7.8 mA		5.48	5.8		5.34		
V_{OL}	V_I = V_{IH} or V_{IL}	I_{OL} = 20 μA	2 V		0.002	0.1		0.1	V
			4.5 V		0.001	0.1		0.1	
			6 V		0.001	0.1		0.1	
		$Q_{H'}$, I_{OL} = 4 mA	4.5 V		0.17	0.26		0.33	
		Q_A – Q_H, I_{OL} = 6 mA			0.17	0.26		0.33	
		$Q_{H'}$, I_{OL} = 5.2 mA	6 V		0.15	0.26		0.33	
		Q_A – Q_H, I_{OL} = 7.8 mA			0.15	0.26		0.33	
I_I	V_I = V_{CC} or 0		6 V		±0.1	±100		±1000	nA
I_{OZ}	V_O = V_{CC} or 0, Q_A – Q_H		6 V		±0.01	±0.5		±5	μA
I_{CC}	V_I = V_{CC} or 0, I_O = 0		6 V			8		80	μA
C_i			2 V to 6 V		3	10		10	pF

6. Timing Requirements

over operating free-air temperature range (unless otherwise noted)

			Vcc	T_A = 25°C		SN74HC595DR-HX		UNIT
				MIN	MAX	MIN	MAX	
f_{clock}	Clock frequency		2 V		6		5	MHz
			4.5 V		31		25	
			6 V		36		29	
t_w	Pulse duration	SRCLK or RCLK high or low	2 V	80		100		ns
			4.5 V	16		20		
			6 V	14		17		
		$\overline{SRCLR}$ low	2 V	80		100		
			4.5 V	16		20		
			6 V	14		17		
t_{su}	Set-up time	SER before SRCLK↑	2 V	100		125		ns
			4.5 V	20		25		
			6 V	17		21		
		SRCLK↑ before RCLK↑(1)	2 V	75		94		
			4.5 V	15		19		
			6 V	13		16		
		$\overline{SRCLR}$ low before RCLK↑	2 V	50		65		
			4.5 V	10		13		
			6 V	9		11		
		$\overline{SRCLR}$ high (inactive) before SRCLK↑	2 V	50		60		
			4.5 V	10		12		
			6 V	9		11		
t_h	Hold time, SER after SRCLK↑		2 V	0		0		ns
			4.5 V	0		0		
			6 V	0		0		

(1) This set-up time allows the storage register to receive stable data from the shift register. The clocks can be tied together, in which case the shift register is one clock pulse ahead of the storage register.



NOTE: ▨ implies that the output is in 3-State mode.

Figure. Timing Diagram

7. Switching Characteristics

Over recommended operating free-air temperature range.

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	Vcc	T_A = 25°C			SN74HC595DR-HX		UNIT
					MIN	TYP	MAX	MIN	MAX	
f_{max}			50 pF	2 V	6	26		5		MHz
				4.5 V	31	38		25		
				6 V	36	42		29		
t_{pd}	SRCLK	$Q_{H'}$	50 pF	2 V		50	160		200	ns
				4.5 V		17	32		40	
				6 V		14	27		34	
	RCLK	Q_A – Q_H	50 pF	2 V		50	150		187	
				4.5 V		17	30		37	
				6 V		14	26		32	
t_{PHL}	$\overline{SRCLR}$	$Q_{H'}$	50 pF	2 V		51	175		219	ns
				4.5 V		18	35		44	
				6 V		15	30		37	
t_{en}	$\overline{OE}$	Q_A – Q_H	50 pF	2 V		40	150		187	ns
				4.5 V		15	30		37	
				6 V		13	26		32	
t_{dis}	$\overline{OE}$	Q_A – Q_H	50 pF	2 V		42	200		250	ns
				4.5 V		23	40		50	
				6 V		20	34		43	
t_t		Q_A – Q_H	50 pF	2 V		28	60		75	ns
				4.5 V		8	12		15	
				6 V		6	10		13	
		$Q_{H'}$	50 pF	2 V		28	75		95	
				4.5 V		8	15		19	
				6 V		6	13		16	
t_{pd}	RCLK	Q_A – Q_H	150 pf	2 V		60	200		250	ns
				4.5 V		22	40		50	
				6 V		19	34		43	
t_{en}	$\overline{OE}$	Q_A – Q_H	150 pf	2 V		70	200		250	ns
				4.5 V		23	40		50	
				6 V		19	34		43	
t_t		Q_A – Q_H	150 pf	2 V		45	210		265	ns
				4.5 V		17	42		53	
				6 V		13	36		45	

8. Operating Characteristics

T_A = 25°C

PARAMETER		TEST CONDITIONS	TYP	UNIT
C_{pd}	Power dissipation capacitance	No load	400	pF

9. Typical Characteristics

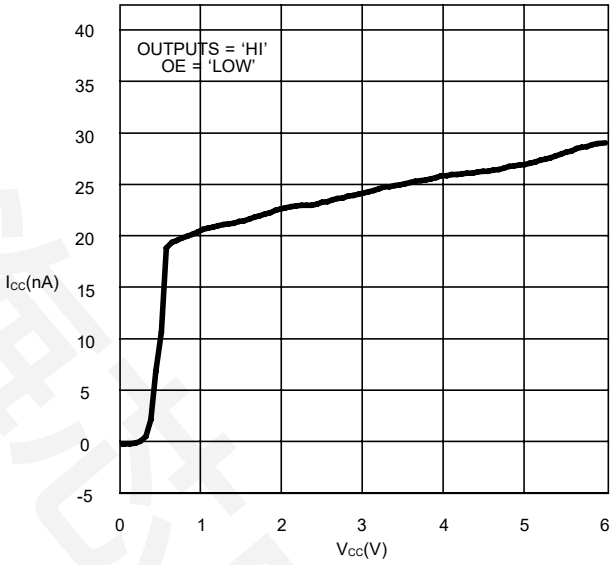
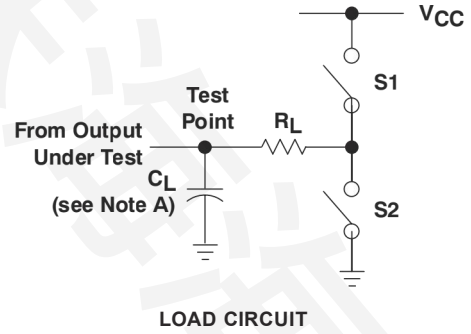


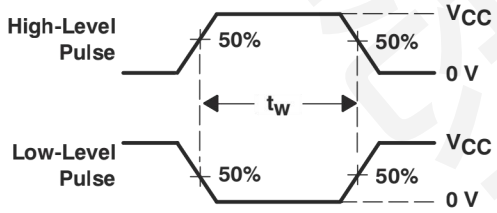
Figure. SN74HC595DR-HX Icc vs. Vcc

Parameter Measurement Information

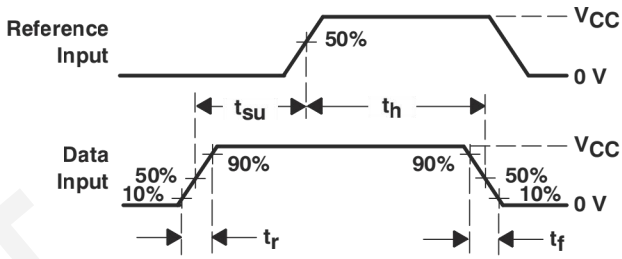


LOAD CIRCUIT

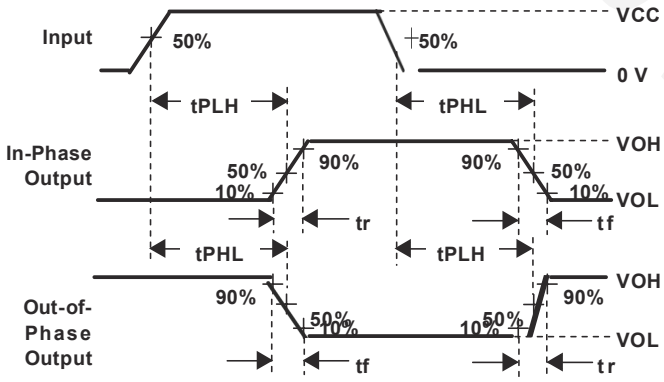
PARAMETER		RL	CL	S1	S2
ten	tPZH	1 kΩ	50 pF or 150 pF	Open	Closed
	tPZL			Closed	Open
tdis	tPHZ	1 kΩ	50 pF	Open	Closed
	tPLZ			Closed	Open
tpd or tt			50 pF or 150 pF	Open	Open



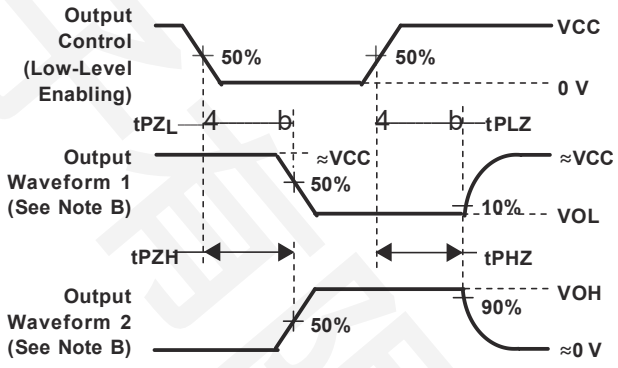
VOLTAGE WAVEFORMS
PULSE DURATIONS



VOLTAGE WAVEFORMS
SETUP AND HOLD AND INPUT RISE AND FALL TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY AND OUTPUT TRANSITION TIMES



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES FOR 3-STATE OUTPUTS

NOTES: A. CL includes probe and test-fixture capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
C. Phase relationships between waveforms were chosen arbitrarily. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, ZO = 50 Ω, tr = 6 ns, tf = 6 ns.
D. For clock inputs, fmax is measured when the input duty cycle is 50%.
E. The outputs are measured one at a time, with one input transition per measurement.
F. tPLZand tPHZ are the same as tdis.
G. tPZLand tPZH are the same as ten.
H. tPLHand tPHL are the same as tpd.

Figure. Load Circuit and Voltage Waveforms

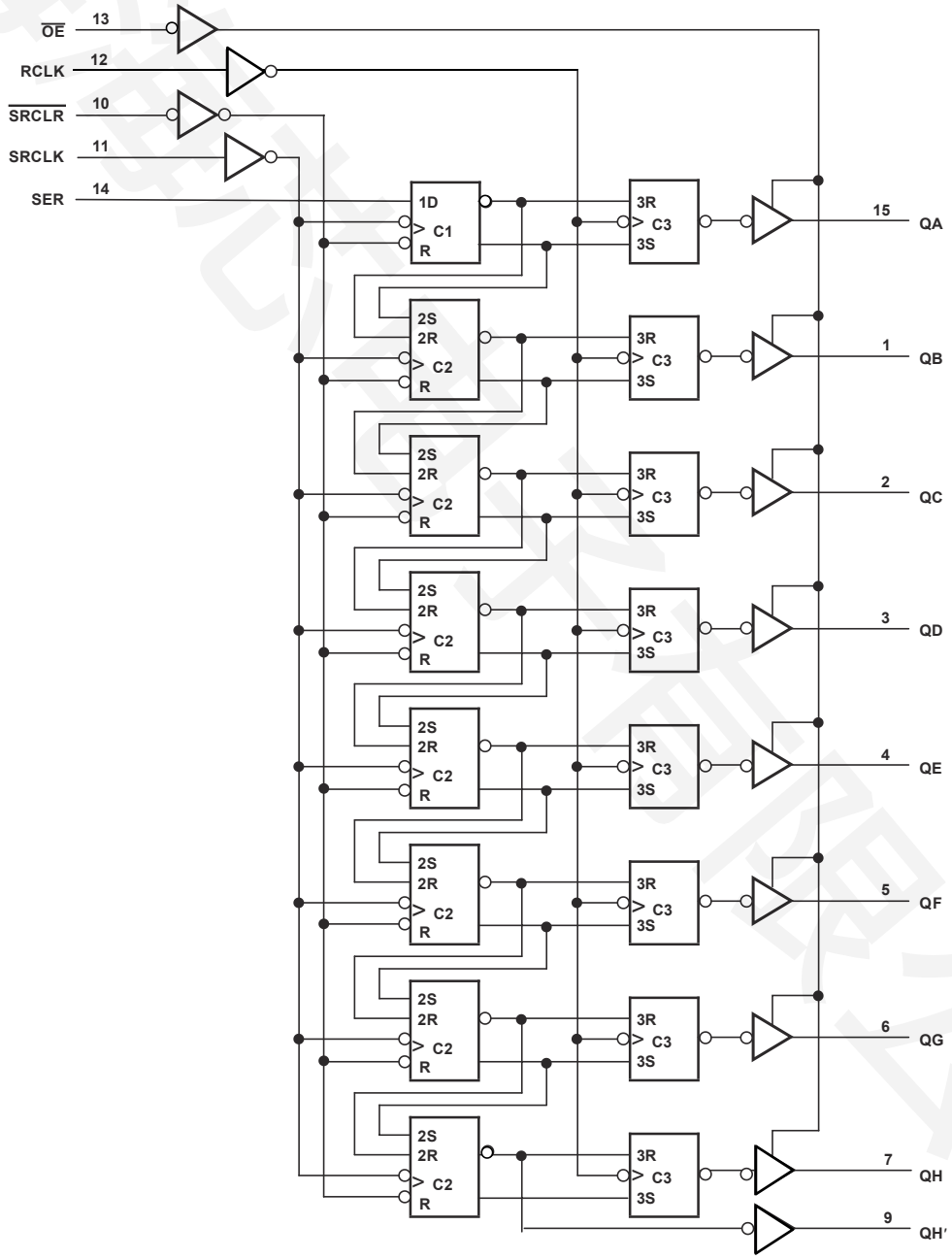
Detailed Description

1. Overview

The SN74HC595DR-HX is part of the HC family of logic devices intended for CMOS applications. The SN74HC595DR-HX is an 8-bit shift register that feeds an 8-bit D-type storage register.

Both the shift register clock (SRCLK) and storage register clock (RCLK) are positive-edge triggered. If both clocks are connected together, the shift register always is one clock pulse ahead of the storage register.

2. Functional Block Diagram



3. Feature Description

The SN74HC595DR-HX devices are 8-bit Serial-In, Parallel-Out Shift Registers. They have a wide operating current of 2 V to 6 V, and the high-current 3-state outputs can drive up to 15 LSTTL Loads. The devices have a low power consumption of 80-μA (Maximum) I_{CC}. Additionally, the devices have a low input current of 1 μA (Maximum) and a ±6-mA Output Drive at 5 V.

4. Device Functional Modes

Table. Function Table lists the functional modes of the SN74HC595DR-HX devices.

Table. Function Table

INPUTS					FUNCTION
SER	SRCLK	$\overline{SRCLR}$	RCLK	$\overline{OE}$	
X	X	X	X	H	Outputs Q_A – Q_H are disabled.
X	X	X	X	L	Outputs Q_A – Q_H are enabled.
X	X	L	X	X	Shift register is cleared.
L	↑	H	X	X	First stage of the shift register goes low. Other stages store the data of previous stage, respectively.
H	↑	H	X	X	First stage of the shift register goes high. Other stages store the data of previous stage, respectively.
X	X	X	↑	X	Shift-register data is stored in the storage register.

Application and Implementation

Note

"Information in the following applications sections is not part of the component specification and does not guarantee its accuracy or completeness. Users are responsible for determining the suitability of components for their intended purposes, as well as validating and testing their design implementation to ensure system functionality."

1. Application Information

The SN74HC595DR-HX is a low-drive CMOS device that can be used for a multitude of bus interface type applications where output ringing is a concern. The low drive and slow edge rates will minimize overshoot and undershoot on the outputs.

2. Typical Application

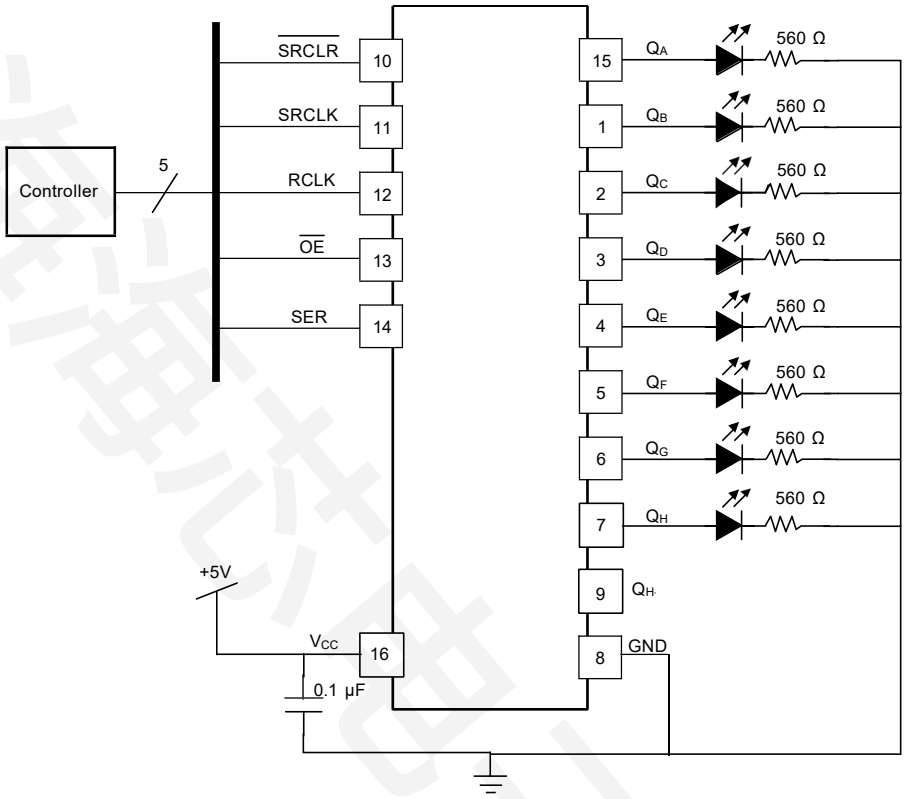


Figure. Typical Application Schematic

2.1. Design Requirements

This device uses CMOS technology and has balanced output drive. Take care to avoid bus contention because it can drive currents that would exceed maximum limits. The high drive will also create fast edges into light loads so routing and load conditions should be considered to prevent ringing.

2.2. Detailed Design Procedure

- Recommended input conditions
  - Specified high and low levels. See (V_{IH} and V_{IL}) in *Section Specifications 3* table.
  - Specified high and low levels. See (V_{IH} and V_{IL}) in *Section Specifications 3* table.
  - Inputs are overvoltage tolerant allowing them to go as high as 5.5 V at any valid V_{CC}
- Recommend output conditions
  - Load currents should not exceed 35 mA per output and 70 mA total for the part
  - Outputs should not be pulled above V_{CC}

Power Supply Recommendations

The power supply can be any voltage between the minimum and maximum supply voltage rating located in *Section Specifications 3* table.

Each V_{CC} pin should have a good bypass capacitor to prevent power disturbance. For devices with a single supply, 0.1 µf is recommended; if there are multiple V_{CC} pins, then 0.01 µf or 0.022 µf is recommended for each power pin. It is acceptable to parallel multiple bypass caps to reject different frequencies of noise. A 0.1 µf and a 1 µf are commonly used in parallel. The bypass capacitor should be installed as close to the power pin as possible for best results.

Layout

1. Layout Guidelines

When using multiple-bit logic devices, inputs should never float.

In many cases, functions or parts of functions of digital logic devices are unused, for example, when only two inputs of a triple-input AND gate are used or only 3 of the 4 buffer gates are used. Such input pins should not be left unconnected because the undefined voltages at the outside connections result in undefined operational states. Figure. Layout Diagram specifies the rules that must be observed under all circumstances. All unused inputs of digital logic devices must be connected to a high or low bias to prevent them from floating. The logic level that should be applied to any particular unused input depends on the function of the device. Generally they will be tied to GND or V_{CC}, whichever makes more sense or is more convenient. It is generally acceptable to float outputs, unless the part is a transceiver. If the transceiver has an output enable pin, it will disable the output section of the part when asserted. This will not disable the input section of the I/Os, so they cannot float when disabled.

2. Layout Example

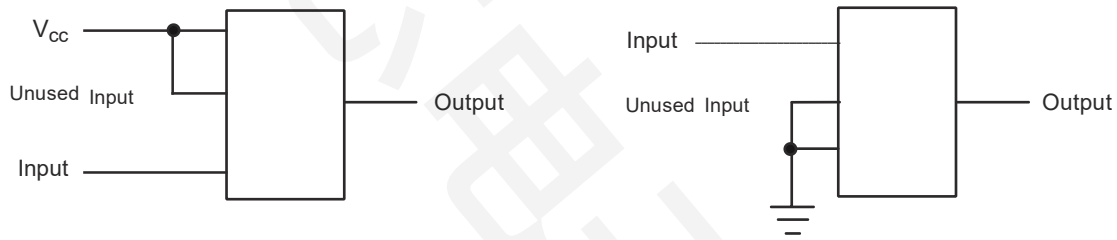


Figure. Layout Diagram

PACKAGING INFORMATION

Orderable Device	Package Type	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)
SN74HC595DR-HX	SOIC	16	2500	RoHS & Green	NIPDAU | SN	Level-1-260C-UNLIM	-40 to 85

(1) **RoHS:** Defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. May reference these types of products as "Pb-Free".
Green: Defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(2) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

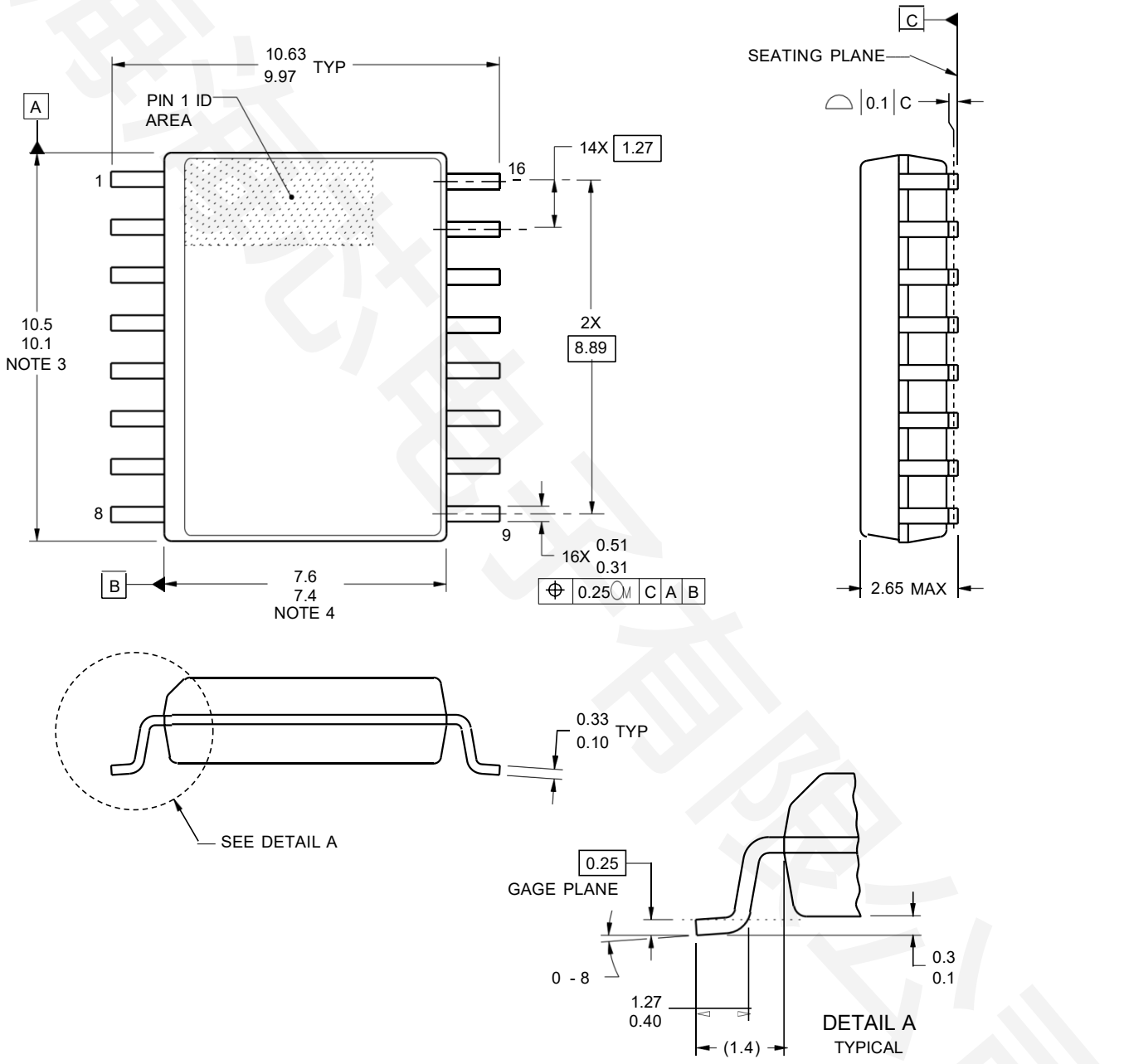
(3) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(4) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(5) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

Package Outline

SOIC-16



NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm, per side.
5. Reference JEDEC registration MS-013.