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SN74HC32PWR-TP

QUADRUPLE 2-INPUT POSITIVE-OR GATES

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Features

- Wide supply voltage range from 2.0 V to 6.0 V
- CMOS low power dissipation
- High noise immunity
- Input CMOS level
- Packaging: TSSOP-14

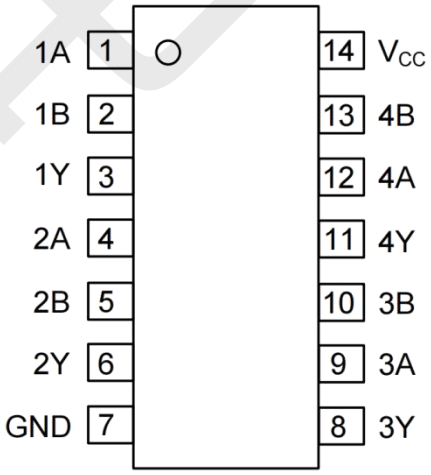
General Description

The 74HC32 are quadruple 2-input positive-or gates which provides the function Y=A+B in positive logic.

Applications

- S-R latch
- Alarm detection circuit
- Tampering detection circuit

PIN CONFIGURATIONS (Top view)



PIN DESCRIPTION

PIN NO.	PIN NAME	DESCRIPTION	PIN NO.	PIN NAME	DESCRIPTION
1	1A	Data input	8	3Y	Data output
2	1B	Data input	9	3A	Data input
3	1Y	Data output	10	3B	Data input
4	2A	Data input	11	4Y	Data output
5	2B	Data input	12	4A	Data input
6	2Y	Data output	13	4B	Data input
7	GND	ground (0 V)	14	V_{CC}	supply voltage

Functional diagram

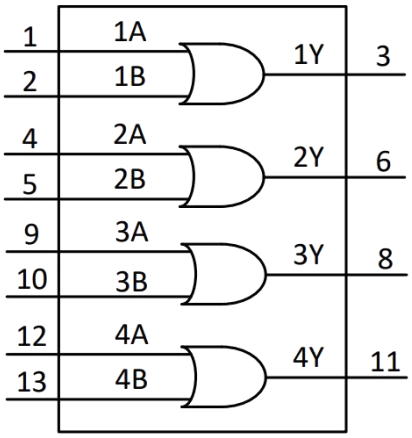


Fig. 1. Logic symbol

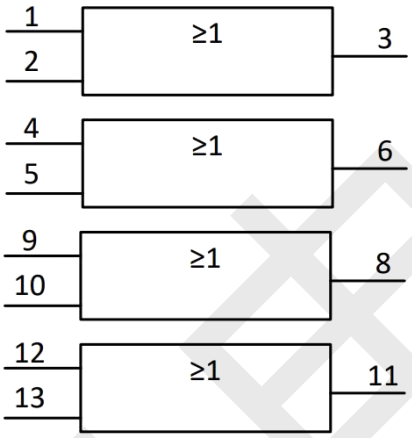


Fig. 2. IEC logic symbol

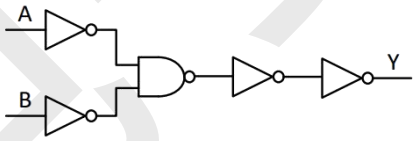


Fig. 3. Logic diagram(one gate)

Function table

Control		Output
nA	**nB**	**nY**
L	L	L
L	H	H
H	L	H
H	H	H

Note: H=HIGH voltage level; L=LOW voltage level.

ABSOLUTE MAXIMUM RATINGS

(Voltages are referenced to GND(ground=0V), unless otherwise specified.)

Parameter	Symbol	Conditions	Min	Max	Unit
Supply voltage	V_{CC}		-0.5	+7	V
Input clamping current	I_{IK}	V_I<-0.5V or V_I>V_{CC}+0.5V	--	±20	mA
Output clamping current	I_{OK}	V_O<-0.5V or V_O>V_{CC}+0.5V	--	±20	mA
Output current	I_O	-0.5V<V_O<V_{CC}+0.5V	--	±25	mA
Supply current	I_{CC}		--	50	mA
Ground current	I_{GND}		-50	--	mA
Total power dissipation	P_{tot}		--	500	mW
Storage temperature	T_{stg}		-65	+150	°C
Soldering temperature	T_L		260		°C

Recommended operating conditions

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Supply voltage	V_{CC}		2.0	5.0	6.0	V
Input voltage	V_I		0	--	V_{CC}	V
Output voltage	V_O		0	--	V_{CC}	V
Input transition rise and fall rate	Δt/ΔV	V_{CC}=2.0V	--	--	1000	ns
		V_{CC}=4.5V	--	--	500	ns
		V_{CC}=6.0V	--	--	400	ns
Ambient temperature	T_{amb}		-40	--	+125	℃

Electrical Characteristics (DC)

(T_{amb}=25℃, voltages are referenced to GND (ground=0V), unless otherwise specified.)

Parameter	Symbol	Conditions		Min	Typ	Max	Unit
HIGH-level input voltage	V_{IH}	V_{CC}=2.0V		1.5	1.2	--	V
		V_{CC}=4.5V		3.15	2.4	--	V
		V_{CC}=6.0V		4.2	3.2	--	V
LOW-level input voltage	V_{IL}	V_{CC}=2.0V		--	0.8	0.5	V
		V_{CC}=4.5V		--	2.1	1.35	V
		V_{CC}=6.0V		--	2.8	1.8	V
HIGH-level output voltage	V_{OH}	V_I=V_{IH} or V_{IL}	I_O=-20uA; V_{CC}=2.0V	1.9	2.0	--	V
			I_O=-20uA; V_{CC}=4.5V	4.4	4.5	--	V
			I_O=-20uA; V_{CC}=6.0V	5.9	6.0	--	V
			I_O=-4.0mA; V_{CC}=4.5V	3.98	4.32	--	V
			I_O=-5.2mA; V_{CC}=6.0V	5.48	5.81	--	V
LOW-level output voltage	V_{OL}	V_I=V_{IH} or V_{IL}	I_O=20uA; V_{CC}=2.0V	--	0	0.1	V
			I_O=20uA; V_{CC}=4.5V	--	0	0.1	V
			I_O=20uA; V_{CC}=6.0V	--	0	0.1	V
			I_O=4.0mA; V_{CC}=4.5V	--	0.15	0.26	V
			I_O=5.2mA; V_{CC}=6.0V	--	0.16	0.26	V
Input leakage current	I_I	V_I= V_{CC} or GND;V_{CC}=6.0V		--	--	±1	uA
Supply current	I_{CC}	V_I= V_{CC} or GND; I_O=0A;V_{CC}=6.0V		--	--	2.0	uA
Input capacitance	C_I			--	3	10	pF

Electrical Characteristics (AC)

(T_{amb}=25℃, voltages are referenced to GND (ground=0V), unless otherwise specified.)

Parameter	Symbol	Conditions		Min	Typ	Max	Unit
nA, nB, to nY propagation delay	t_{pd}	see Figure 5[1]	V_{CC}=2.0V	--	--	100	ns
			V_{CC}=4.5V	--	--	30	ns
			V_{CC}=5.0V;C_L=15pF	--	20	--	ns
			V_{CC}=6.0V	--	--	17	ns
Transition time	t_t	see Figure 5[2]	V_{CC}=2.0V	--	--	75	ns
			V_{CC}=4.5V	--	--	15	ns
			V_{CC}=6.0V	--	--	13	ns
Power dissipation capacitance	C_{PD}	per package; V_I= GND to V_{CC}[3]		--	20	--	pF

Note:

[1] t_{pd} is the same as t_{PLH} and t_{PHL}.

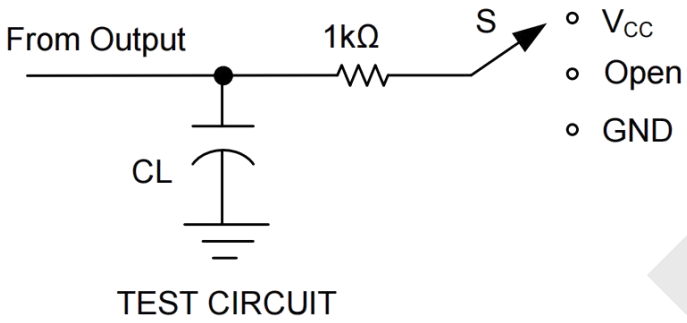
[2] t_t is the same as t_{THL} and t_{TLH}.

[3] C_{PD} is used to determine the dynamic power dissipation (P_D in uW). $P_D=(C_{PD}\times V_{CC}^2\times f_i\times N)+\sum(C_L\times V_{CC}^2\times f_o)$ where:

f_i=input frequency in MHz; f_o=output frequency in MHz; C_L=output load capacitance in pF; V_{CC}=supply voltage in V; N=number of inputs switching;

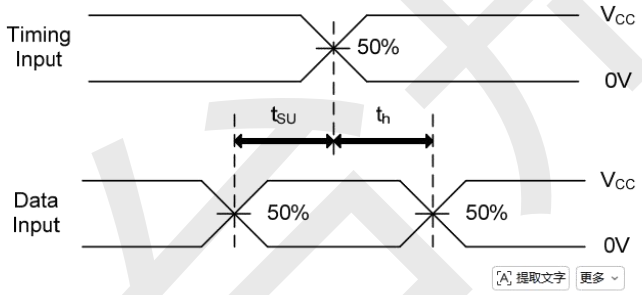
$\sum(C_L\times V_{CC}^2\times f_o)$=sum of outputs.

Testing Circuit

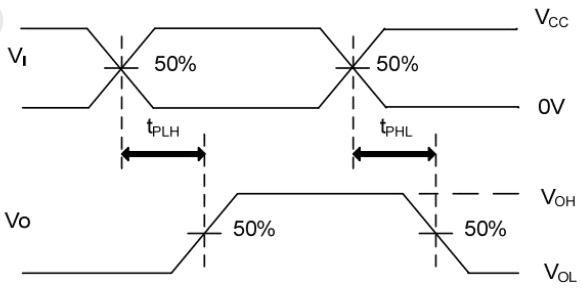


TEST CIRCUIT

TEST	S
t_{PLH}/t_{PHL}	Open
t_{PHZ}/t_{PZH}	GND
t_{PLZ}/t_{PZL}	V_{CC}



SETUP TIME AND HOLD TIME

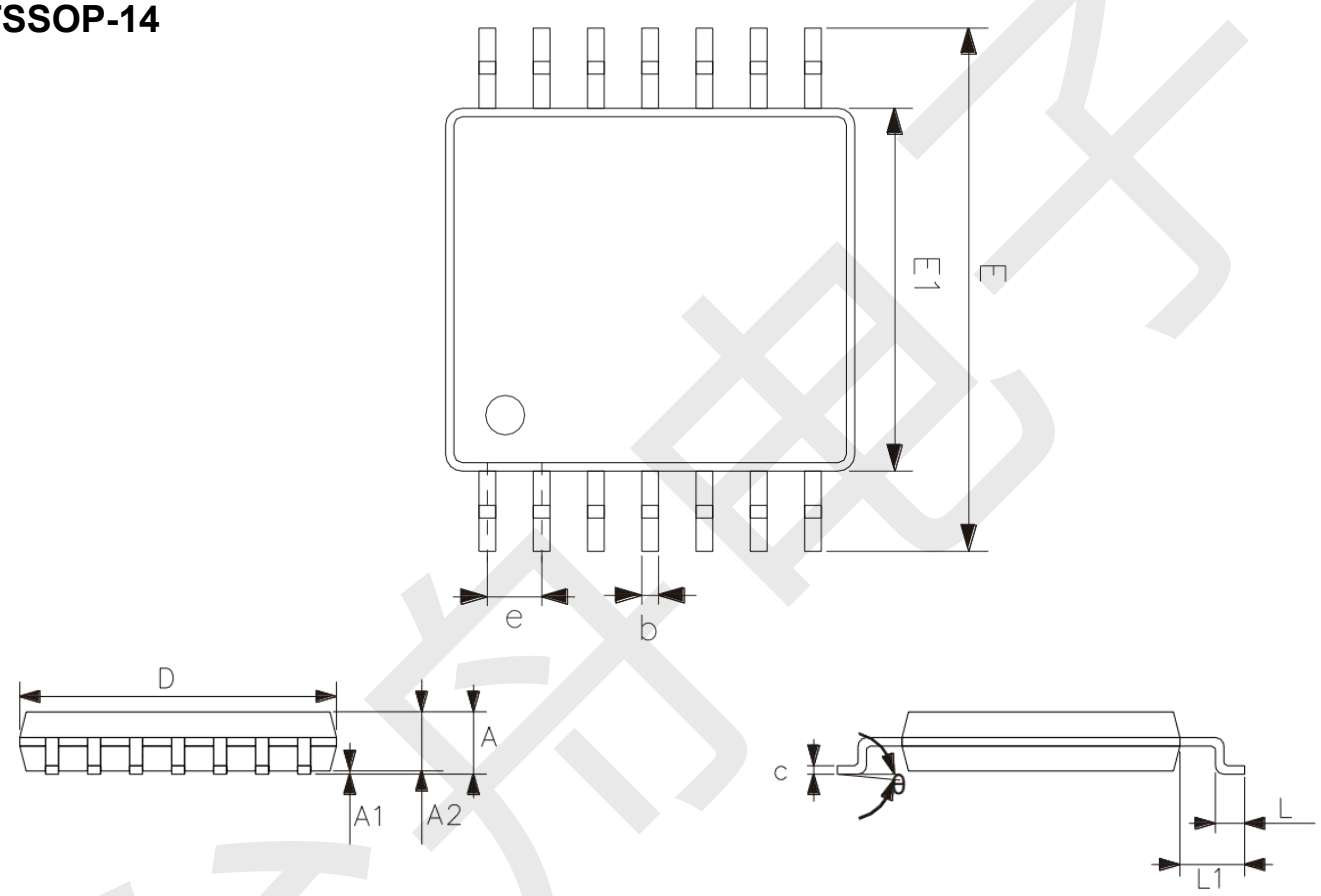


PROPAGATION DELAY TIMES

Note: C_L includes probe and jig capacitance.
PRR ≤1MHz, Z_O = 50Ω, t_R ≤3ns, t_F ≤3ns.

Package information

TSSOP-14



Symbol	Dimensions (mm)	
	Min.	Max.
A	-	1.20
A1	0.05	0.15
A2	0.80	1.05
b	0.19	0.30
c	0.09	0.20
D	4.90	5.10
E1	4.30	4.50
E	6.20	6.60
e	0.65	
L	0.45	0.75
L1	1.00	
θ	0°	8°