TECH PUBLIC
台舟电子

74HC3G04DP-TP

TRIPLE INVERTER GATE

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Features

- Wide supply voltage range from 2.0 V to 6.0 V
- Input CMOS level
- High noise immunity
- CMOS low power dissipation
- ESD Protection Exceeds JESD 22
  -2000-V Human-Body Model (A114-A)
  -200-V Machine Model (A115-A)
  -1000-V Charged-Device Model (C101)
- MSOP-8 Package Available

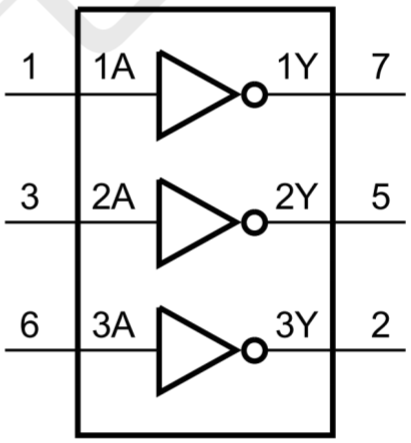
Applications

- AV Receiver
- Audio Dock:Portable
- Blu-ray Player and Home Theater
- Embedded PC
- Personal Digital Assistant(PDA)
- Power:Telecom/Server AC/DC Supply:Single Controller:Analog and Digital

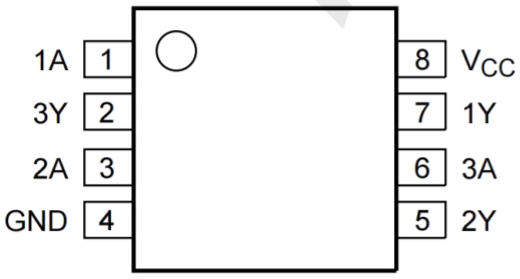
General Description

The 74HC3G04 is a triple inverter. Inputs include clamp diodes. This enables the use of current limiting resistors to interface inputs to voltages in excess of VCC.

Logic Diagram



Pin Configuratio



MSOP-8

Function Table

INPUT(A)	OUTPUT(Y)
H	L
L	H

Note:H: HIGH voltage level;L: LOW voltage level.

Absolute Maximum Ratings

(Unless otherwise specified)

PARAMETER	SYMBOL	CONDITIONS	RATINGS	UNIT
Supply Voltage	V_{CC}		-0.5 ~ +7.0	V
Input Voltage	V_{IN}		-0.5 ~ +7.0	V
Output Voltage	V_{OUT}	Output in the high or low state	-0.5 ~ +7.0	V
		Output in the power-off state	-0.5 ~ VCC+0.5	V
VCC or GND Current	I_{CC}		50	mA
Continuous Output Current	I_{OUT}		20	mA
Input Clamp Current	I_{IK}	V_{IN}<0	20	mA
Output Clamp Current	I_{OK}	V_{OUT}<0	20	mA
Storage Temperature Range	T_{STG}		-65 ~ +150	℃
Junction to Ambient	θ_{JA}		220	℃/W

Note: Absolute maximum ratings are those values beyond which the device could be permanently damaged. Absolute maximum ratings are stress ratings only and functional device operation is not implied.

Recommended Operating Conditions

(Unless otherwise specified)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Supply Voltage	V_{CC}		2.0	--	6.0	V
Input Voltage	V_{IN}		0	--	6.0	V
Output Voltage	V_{OUT}	High or low state	0	--	V_{CC}	V
Operating Temperature (Note)	T_A		-40	--	+125	°C

Electrical Characteristics (unless otherwise specified)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
High-Level input voltage	V_{IH}	V_{CC}=2.0V	1.5	--	--	V
		V_{CC}=4.5V	3.15	--	--	V
		V_{CC}=6.0V	4.2	--	--	V
Low-Level input voltage	V_{IL}	V_{CC}=2.0V	--	--	0.5	V
		V_{CC}=4.5V	--	--	1.35	V
		V_{CC}=6.0V	--	--	1.8	V
High-Level Output Voltage	V_{OH}	V_{CC}=2.0V, V_{IN}=V_{IH} or V_{IL}, I_{OH}=-50μA	1.9	2.0	--	V
		V_{CC}=4.5V, V_{IN}=V_{IH} or V_{IL}, I_{OH}=-50μA	4.4	4.5	--	V
		V_{CC}=6.0V, V_{IN}=V_{IH} or V_{IL}, I_{OH}=-50μA	5.9	6.0	--	V
		V_{CC}=4.5V, V_{IN}=V_{IH} or V_{IL}, I_{OH}=-8.0mA	4.18	--	--	V
		V_{CC}=6.0V, V_{IN}=V_{IH} or V_{IL}, I_{OH}=-8.0mA	5.68	--	--	V
Low-Level Output Voltage	V_{OL}	V_{CC}=2.0V, V_{IN}=V_{IH} or V_{IL}, I_{OL}=50μA	--	--	0.1	V
		V_{CC}=3.0V, V_{IN}=V_{IH} or V_{IL}, I_{OL}=50μA	--	--	0.1	V
		V_{CC}=4.5V, V_{IN}=V_{IH} or V_{IL}, I_{OL}=50μA	--	--	0.1	V
		V_{CC}=3.0V, V_{IN}=V_{IH} or V_{IL}, I_{OL}=4.0mA	--	--	0.33	V
		V_{CC}=6.0V, V_{IN}=V_{IH} or V_{IL}, I_{OL}=8.0mA	--	--	0.33	V
Input Leakage Current	$I_{I(LEAK)}$	V_{CC}=6.0V, V_{IN}=V_{CC} or GND	--	--	0.1	μA
Quiescent Supply Current	I_{CC}	V_{CC}=6.0V, V_{IN}=V_{CC} or GND, I_{OUT}=0	--	--	10	μA
Input Capacitance	C_{IN}	V_{IN}=V_{CC} or GND	--	--	10	pF

OPERATING CHARACTERISTICS

(f=10MHz, TA =25°C , unless otherwise specified)

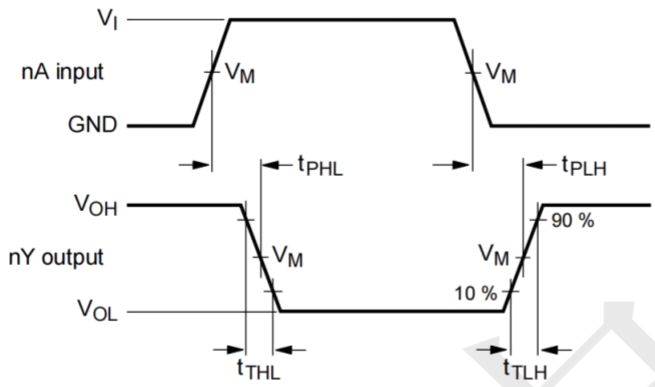
PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Power Dissipation Capacitance	C_{PD}	V_{CC}=2.0V	--	9	--	pF
		V_{CC}=3.3V	--	9	--	pF
		V_{CC}=4.5V	--	9	--	pF
		V_{CC}=6.0V	--	9	--	pF

DYNAMIC CHARACTERISTICS

(T_A=25°C, unless otherwise specified)

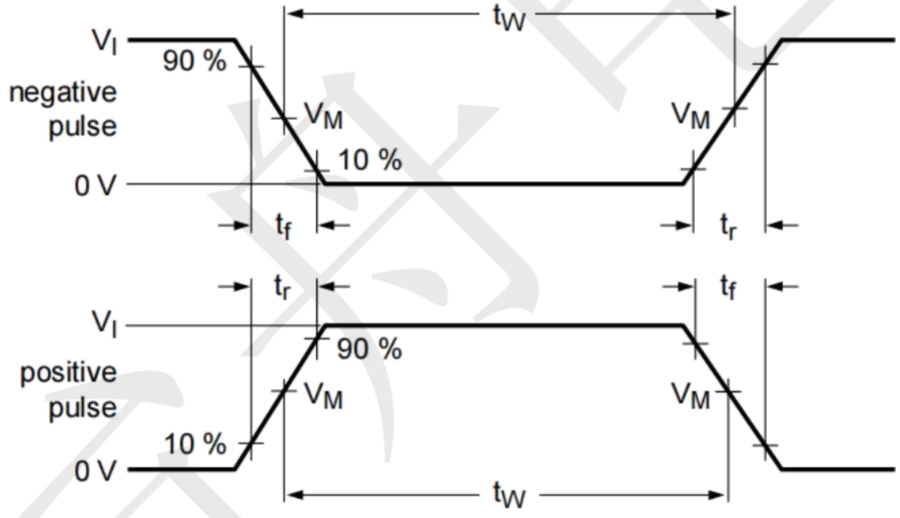
PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Propagation Delay From input (A) to output(Y)	t_{PD}	V_{CC}=3.3±0.15V,C_L=30pF, R_L=1kΩ	--	--	75	ns
		V_{CC}=5.5±0.2V,C_L=30pF, R_L=500Ω	--	--	15	ns
		V_{CC}=3.3±0.3V,C_L=50pF, R_L=500Ω	--	--	22	ns
		V_{CC}=5.5±0.5V,C_L=50pF, R_L=500Ω	--	--	19	ns

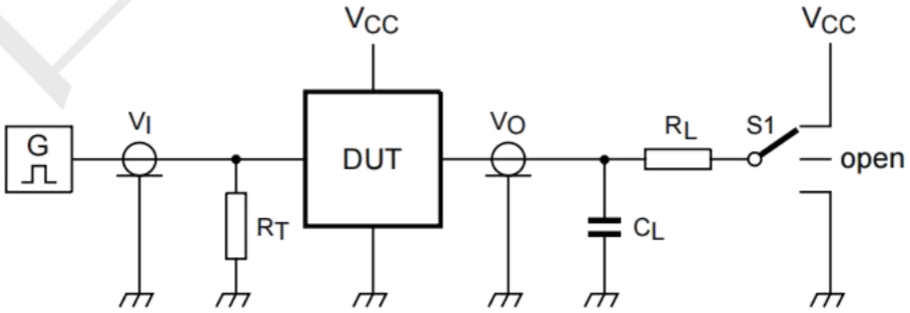
TEST CIRCUIT AND WAVEFORMS



Logic levels: V_{OL} and V_{OH} are typical output voltage levels that occur with the output load.

The data input (nA) to output (nY) propagation delays



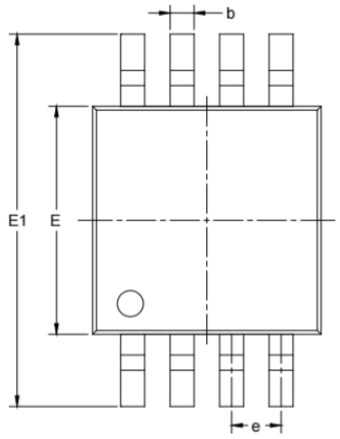


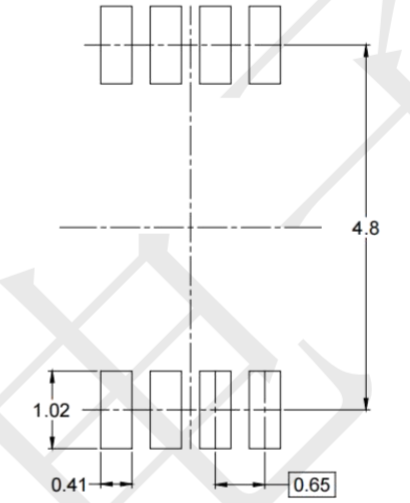
R_T = Termination resistance should be equal to output impedance Z_o of the pulse generator;
C_L = Load capacitance including jig and probe capacitance; R_L = Load resistance; S1 = Test selection switch.

Test circuit for measuring switching times

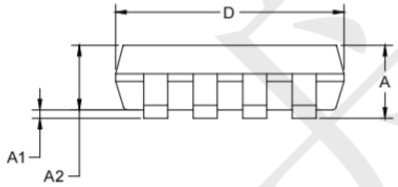
Package information

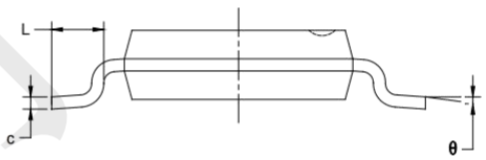
MSOP-8





RECOMMENDED LAND PATTERN (Unit: mm)





Symbol	Dimensions In Millimeters		Dimensions In Inches	
	MIN	MAX	MIN	MAX
A	0.820	1.100	0.032	0.043
A1	0.020	0.150	0.001	0.006
A2	0.750	0.950	0.030	0.037
b	0.250	0.380	0.010	0.015
c	0.090	0.230	0.004	0.009
D	2.900	3.100	0.114	0.122
E	2.900	3.100	0.114	0.122
E1	4.750	5.050	0.187	0.199
e	0.650 BSC		0.026 BSC	
L	0.400	0.800	0.016	0.031
θ	0°	6°	0°	6°