

EtronTech

EM6AB160

32M x 16 bit DDR Synchronous DRAM (SDRAM)

Advance (Rev. 1.3, Jun. /2015)

Features

- Fast clock rate: 250/200MHz
- Differential Clock CK & $\overline{CK}$
- Bi-directional DQS
- DLL enable/disable by EMRS
- Fully synchronous operation
- Internal pipeline architecture
- Four internal banks, 8M x 16-bit for each bank
- Programmable Mode and Extended Mode registers
 - CAS Latency: 2, 2.5, 3
 - Burst length: 2, 4, 8
 - Burst Type: Sequential & Interleaved
- Individual byte write mask control
- DM Write Latency = 0
- Auto Refresh and Self Refresh
- 8192 refresh cycles / 64ms
- Precharge & active power down
- Power supplies: VDD & VDDQ = 2.5V $\pm$ 0.2V
- Operating Temperature: T_A = 0~70°C
- Interface: SSTL_2 I/O Interface
- Package: 66 Pin TSOP II, 0.65mm pin pitch
 - Pb and Halogen free
- Package: 60-Ball, 8x13x1.2 mm (max) FBGA
 - Pb free and Halogen Free

Overview

The EM6AB160 SDRAM is a high-speed CMOS double data rate synchronous DRAM containing 512 Mbits. It is internally configured as a quad 8M x 16 DRAM with a synchronous interface (all signals are registered on the positive edge of the clock signal, CK). Data outputs occur at both rising edges of CK and $\overline{CK}$. Read and write accesses to the SDRAM are burst oriented; accesses start at a selected location and continue for a programmed number of locations in a programmed sequence. Accesses begin with the registration of a BankActivate command which is then followed by a Read or Write command. The EM6AB160 provides programmable Read or Write burst lengths of 2, 4, or 8. An auto precharge function may be enabled to provide a self-timed row precharge that is initiated at the end of the burst sequence. The refresh functions, either Auto or Self Refresh are easy to use. In addition, EM6AB160 features programmable DLL option. By having a programmable mode register and extended mode register, the system can choose the most suitable modes to maximize its performance. These devices are well suited for applications requiring high memory bandwidth, result in a device particularly well suited to high performance main memory and graphics applications.

Table 1. Ordering Information

Part Number	Clock Frequency	Data Rate	Package
EM6AB160TSE-4G	250MHz	500Mbps/pin	TSOPII
EM6AB160TSE-5G	200MHz	400Mbps/pin	TSOPII
EM6AB160WKE-4H	250MHz	500Mbps/pin	FBGA
EM6AB160WKE-5H	200MHz	400Mbps/pin	FBGA

TS : indicates TSOPII package
WK: indicates 8x13x1.2 mm FBGA package
E: indicates Generation Code
G: indicates Pb and Halogen free for TSOPII Package
H: indicates Pb and Halogen free for FBGA Package

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Figure 1. Pin Assignment (Top View)

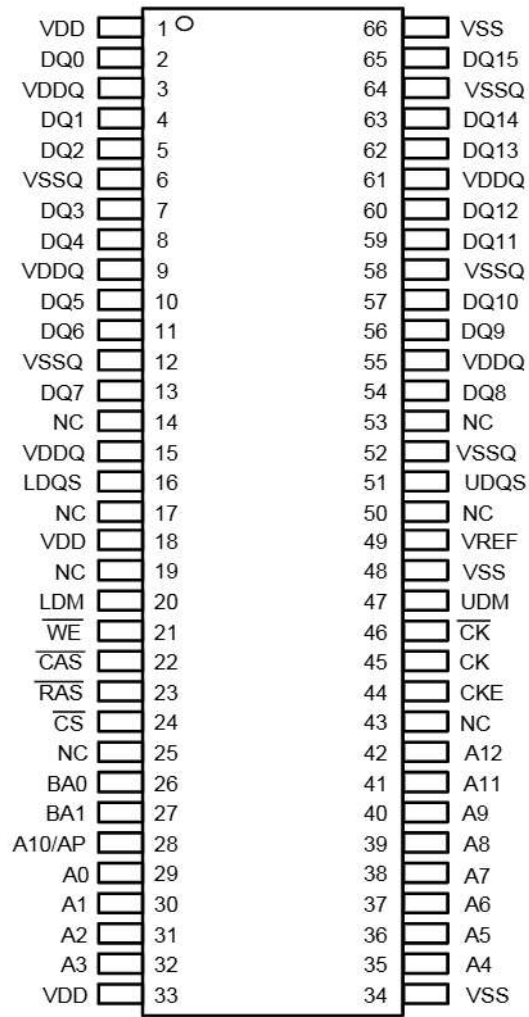


Figure 1.1 Ball Assignment (Top View)

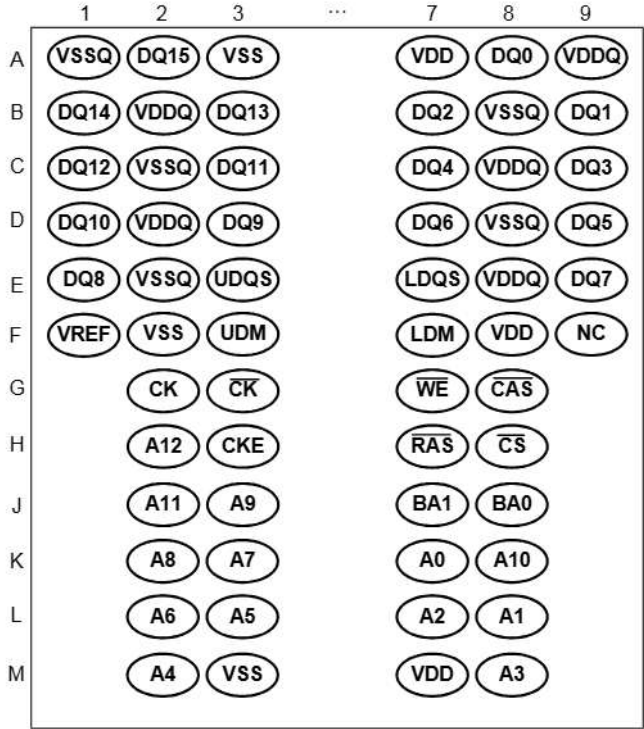
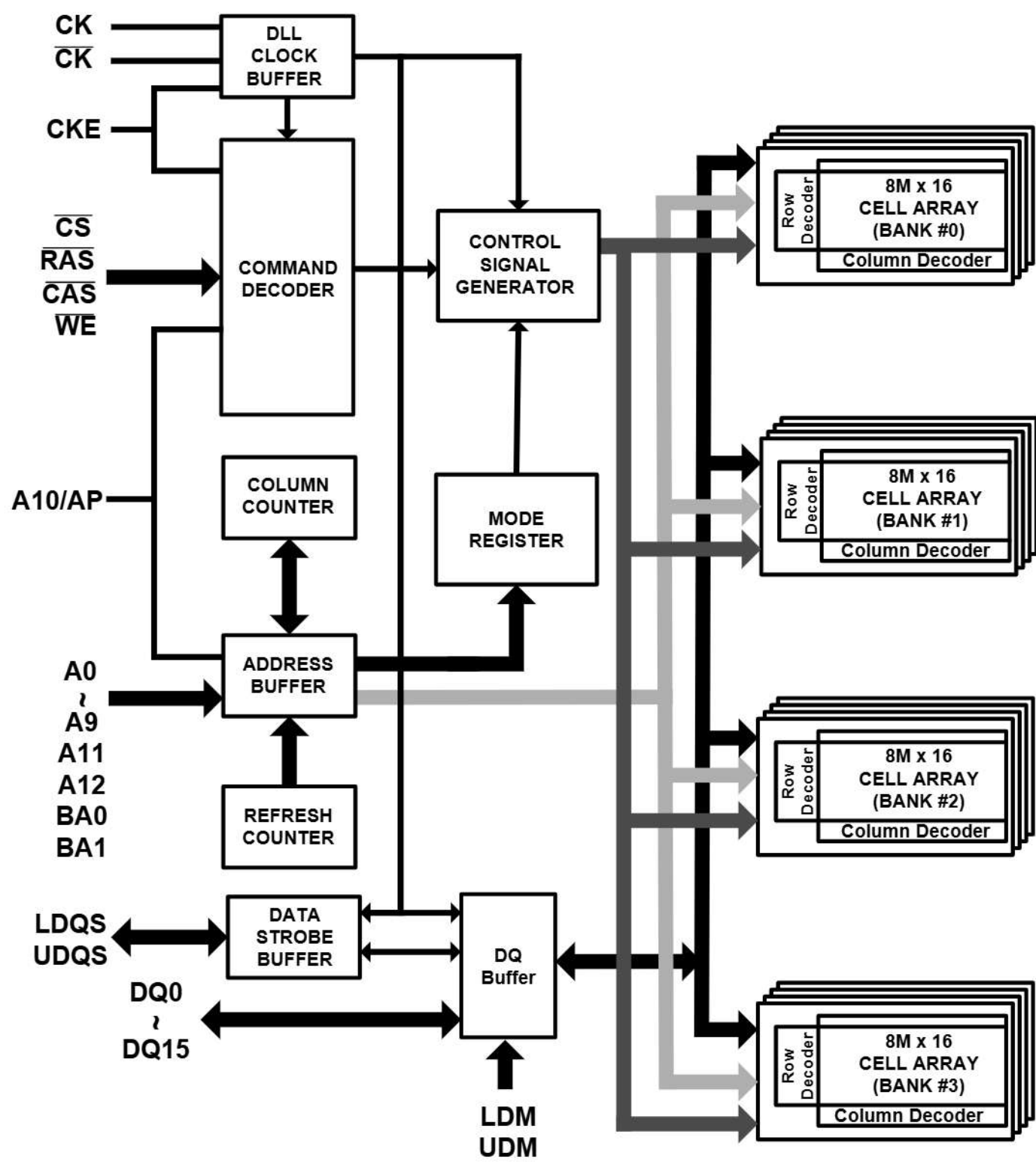


Figure 2. Block Diagram



Pin Descriptions

Table 2. Pin Details of EM6AB160

Symbol	Type	Description
CK, $\overline{CK}$	Input	Differential Clock: CK and $\overline{CK}$ are differential clock inputs. All address and control input signals are sampled on the crossing of the positive edge of CK and negative edge of $\overline{CK}$. Input and output data is referenced to the crossing of CK and $\overline{CK}$ (both directions of the crossing)
CKE	Input	Clock Enable: CKE activates (HIGH) and deactivates (LOW) the CK signal. If CKE goes low synchronously with clock, the internal clock is suspended from the next clock cycle and the state of output and burst address is frozen as long as the CKE remains low. When all banks are in the idle state, deactivating the clock controls the entry to the Power Down and Self Refresh modes.
BA0, BA1	Input	Bank Activate: BA0 and BA1 define to which bank the BankActivate, Read, Write, or BankPrecharge command is being applied.
A0-A12	Input	Address Inputs: A0-A12 are sampled during the BankActivate command (row address A0-A12) and Read/Write command (column address A0-A9 with A10 defining Auto Precharge).
$\overline{CS}$	Input	Chip Select: $\overline{CS}$ enables (sampled LOW) and disables (sampled HIGH) the command decoder. All commands are masked when $\overline{CS}$ is sampled HIGH. $\overline{CS}$ provides for external bank selection on systems with multiple banks. It is considered part of the command code.
$\overline{RAS}$	Input	Row Address Strobe: The $\overline{RAS}$ signal defines the operation commands in conjunction with the $\overline{CAS}$ and $\overline{WE}$ signals and is latched at the positive edges of CK. When $\overline{RAS}$ and $\overline{CS}$ are asserted "LOW" and $\overline{CAS}$ is asserted "HIGH," either the BankActivate command or the Precharge command is selected by the $\overline{WE}$ signal. When the $\overline{WE}$ is asserted "HIGH," the BankActivate command is selected and the bank designated by BA is turned on to the active state. When the $\overline{WE}$ is asserted "LOW," the Precharge command is selected and the bank designated by BA is switched to the idle state after the precharge operation.
$\overline{CAS}$	Input	Column Address Strobe: The $\overline{CAS}$ signal defines the operation commands in conjunction with the $\overline{RAS}$ and $\overline{WE}$ signals and is latched at the positive edges of CK. When $\overline{RAS}$ is held "HIGH" and $\overline{CS}$ is asserted "LOW," the column access is started by asserting $\overline{CAS}$ "LOW." Then, the Read or Write command is selected by asserting $\overline{WE}$ "HIGH" or "LOW".
$\overline{WE}$	Input	Write Enable: The $\overline{WE}$ signal defines the operation commands in conjunction with the $\overline{RAS}$ and $\overline{CAS}$ signals and is latched at the positive edges of CK. The $\overline{WE}$ input is used to select the BankActivate or Precharge command and Read or Write command.
LDQS, UDQS	Input / Output	Bidirectional Data Strobe: Specifies timing for Input and Output data. Read Data Strobe is edge triggered. Write Data Strobe provides a setup and hold time for data and DQM. LDQS is for DQ0~7, UDQS is for DQ8~15.
LDM, UDM	Input	Data Input Mask: Input data is masked when DM is sampled HIGH during a write cycle. LDM masks DQ0-DQ7, UDM masks DQ8-DQ15.
DQ0 - DQ15	Input / Output	Data I/O: The DQ0-DQ15 input and output data are synchronized with positive and negative edges of LDQS and UDQS. The I/Os are byte-maskable during Writes.
V _{DD}	Supply	Power Supply: 2.5V $\pm$ 0.2V .

V _{SS}	Supply	Ground
V _{DDQ}	Supply	DQ Power: 2.5V ± 0.2V . Provide isolated power to DQs for improved noise immunity.
V _{SSQ}	Supply	DQ Ground: Provide isolated ground to DQs for improved noise immunity.
V _{REF}	Supply	Reference Voltage for Inputs: +0.5*V _{DDQ}
NC	-	No Connect: These pins should be left unconnected.

Operation Mode

Table 3 shows the truth table for the operation commands.

Table 3. Truth Table (Note (1), (2))

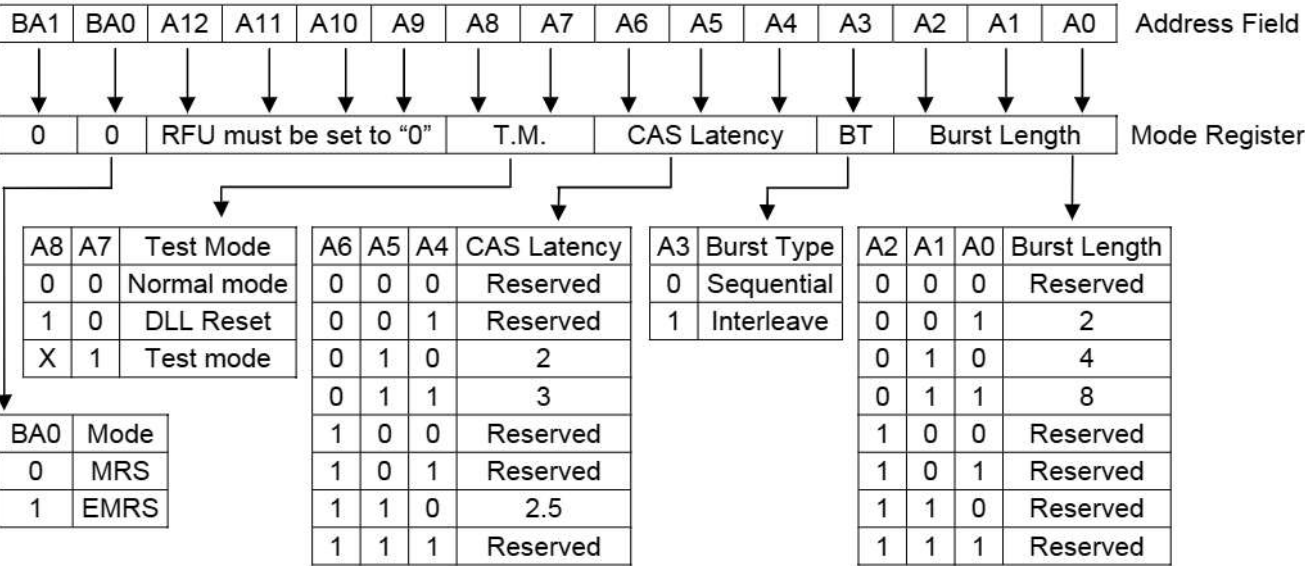
Command	State	CKE _{n-1}	CKE _n	DM	BA0,1	A10	A0-9, 11-12	$\overline{\text{CS}}$	RAS	$\overline{\text{CAS}}$	$\overline{\text{WE}}$
BankActivate	Idle ⁽³⁾	H	X	X	V	Row address		L	L	H	H
BankPrecharge	Any	H	X	X	V	L	X	L	L	H	L
PrechargeAll	Any	H	X	X	X	H	X	L	L	H	L
Write	Active ⁽³⁾	H	X	X	V	L	Column address (A0 ~ A9)	L	H	L	L
Write and AutoPrecharge	Active ⁽³⁾	H	X	X	V	H		L	H	L	L
Read	Active ⁽³⁾	H	X	X	V	L	Column address (A0 ~ A9)	L	H	L	H
Read and Autoprecharge	Active ⁽³⁾	H	X	X	V	H		L	H	L	H
Mode Register Set	Idle	H	X	X	OP code			L	L	L	L
Extended MRS	Idle	H	X	X	OP code			L	L	L	L
No-Operation	Any	H	X	X	X	X	X	L	H	H	H
Burst Stop	Active ⁽⁴⁾	H	X	X	X	X	X	L	H	H	L
Device Deselect	Any	H	X	X	X	X	X	H	X	X	X
AutoRefresh	Idle	H	H	X	X	X	X	L	L	L	H
SelfRefresh Entry	Idle	H	L	X	X	X	X	L	L	L	H
SelfRefresh Exit	Idle (SelfRefresh)	L	H	X	X	X	X	H	X	X	X
								L	H	H	H
Precharge Power Down Mode Entry	Idle	H	L	X	X	X	X	H	X	X	X
								L	H	H	H
Precharge Power Down Mode Exit	Any (PowerDown)	L	H	X	X	X	X	H	X	X	X
								L	H	H	H
Active Power Down Mode Entry	Active	H	L	X	X	X	X	H	X	X	X
								L	V	V	V
Active Power Down Mode Exit	Any (PowerDown)	L	H	X	X	X	X	H	X	X	X
								L	H	H	H
Data Input Mask Disable	Active	H	X	L	X	X	X	X	X	X	X
Data Input Mask Enable ⁽⁵⁾	Active	H	X	H	X	X	X	X	X	X	X

- Note:**
- 1. V=Valid data, X=Don't Care, L=Low level, H=High level
 - 2. CKE_n signal is input level when commands are provided.
CKE_{n-1} signal is input level one clock cycle before the commands are provided.
 - 3. These are states of bank designated by BA signal.
 - 4. Device state is 2, 4, and 8 burst operation.
 - 5. LDM and UDM can be enabled respectively.

Mode Register Set (MRS)

The Mode Register stores the data for controlling various operating modes of a DDR SDRAM. It programs CAS Latency, Burst Type, and Burst Length to make the DDR SDRAM useful for a variety of applications. The default value of the Mode Register is not defined; therefore the Mode Register must be written by the user. Values stored in the register will be retained until the register is reprogrammed. The Mode Register is written by asserting Low on $\overline{CS}$, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, BA1 and BA0 (the device should have all banks idle with no bursts in progress prior to writing into the mode register, and CKE should be High). The state of address pins A0~A12 and BA0, BA1 in the same cycle in which $\overline{CS}$, $\overline{RAS}$, $\overline{CAS}$ and $\overline{WE}$ are asserted Low is written into the Mode Register. A minimum of two clock cycles, tMRD, are required to complete the write operation in the Mode Register. The Mode Register is divided into various fields depending on functionality. The Burst Length uses A0~A2, Burst Type uses A3, and CAS Latency (read latency from column address) uses A4~A6. A logic 0 should be programmed to all the undefined addresses to ensure future compatibility. Reserved states should not be used to avoid unknown device operation or incompatibility with future versions. Refer to the table for specific codes for various burst lengths, burst types and CAS latencies.

Table 4. Mode Register Bitmap



- Burst Length Field (A2~A0)
This field specifies the data length of column access using the A2~A0 pins and selects the Burst Length to be 2, 4, 8.

Table 5. Burst Length

A2	A1	A0	Burst Length
0	0	0	Reserved
0	0	1	2
0	1	0	4
0	1	1	8
1	0	0	Reserved
1	0	1	Reserved
1	1	0	Reserved
1	1	1	Reserved

- Addressing Mode Select Field (A3)
The Addressing Mode can be one of two modes, either Interleave Mode or Sequential Mode. Both Sequential Mode and Interleave Mode support burst length of 2, 4 and 8.

Table 6. Addressing Mode

A3	Addressing Mode
0	Sequential
1	Interleave

- Burst Definition, Addressing Sequence of Sequential and Interleave Mode

Table 7. Burst Address ordering

Burst Length	Start Address			Sequential	Interleave
	A2	A1	A0		
2	X	X	0	0, 1	0, 1
	X	X	1	1, 0	1, 0
4	X	0	0	0, 1, 2, 3	0, 1, 2, 3
	X	0	1	1, 2, 3, 0	1, 0, 3, 2
	X	1	0	2, 3, 0, 1	2, 3, 0, 1
	X	1	1	3, 0, 1, 2	3, 2, 1, 0
8	0	0	0	0, 1, 2, 3, 4, 5, 6, 7	0, 1, 2, 3, 4, 5, 6, 7
	0	0	1	1, 2, 3, 4, 5, 6, 7, 0	1, 0, 3, 2, 5, 4, 7, 6
	0	1	0	2, 3, 4, 5, 6, 7, 0, 1	2, 3, 0, 1, 6, 7, 4, 5
	0	1	1	3, 4, 5, 6, 7, 0, 1, 2	3, 2, 1, 0, 7, 6, 5, 4
	1	0	0	4, 5, 6, 7, 0, 1, 2, 3	4, 5, 6, 7, 0, 1, 2, 3
	1	0	1	5, 6, 7, 0, 1, 2, 3, 4	5, 4, 7, 6, 1, 0, 3, 2
	1	1	0	6, 7, 0, 1, 2, 3, 4, 5	6, 7, 4, 5, 2, 3, 0, 1
	1	1	1	7, 0, 1, 2, 3, 4, 5, 6	7, 6, 5, 4, 3, 2, 1, 0

- CAS Latency Field (A6~A4)
This field specifies the number of clock cycles from the assertion of the Read command to the first read data. The minimum whole value of CAS Latency depends on the frequency of CK. The minimum whole value satisfying the following formula must be programmed into this field. $t_{CAC}(\text{min}) \leq \text{CAS Latency} \times t_{CK}$

Table 8. CAS Latency

A6	A5	A4	CAS Latency
0	0	0	Reserved
0	0	1	Reserved
0	1	0	2 clocks
0	1	1	3 clocks
1	0	0	Reserved
1	0	1	Reserved
1	1	0	2.5 clocks
1	1	1	Reserved

- Test Mode field (A8~A7)
These two bits are used to enter the test mode and must be programmed to "00" in normal operation.

Table 9. Test Mode

A8	A7	Test Mode
0	0	Normal mode
1	0	DLL Reset

- (BA0, BA1)

Table 10. MRS/EMRS

BA1	BA0	A12 ~ A0
RFU	0	MRS Cycle
RFU	1	Extended Functions (EMRS)

Extended Mode Register Set (EMRS)

The Extended Mode Register Set stores the data for enabling or disabling DLL and selecting output driver strength. The default value of the extended mode register is not defined, therefore must be written after power up for proper operation. The Extended Mode Register is written by asserting Low on $\overline{CS}$, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, BA1 and BA0 (the device should have all banks idle with no bursts in progress prior to writing into the mode register, and CKE should be High). The state of A0 ~ A12, BA0 and BA1 is written in the mode register in the same cycle as $\overline{CS}$, $\overline{RAS}$, $\overline{CAS}$, and $\overline{WE}$ going low. The DDR SDRAM should be in all bank precharge with CKE already high prior to writing into the extended mode register. A1 is used for setting driver strength to normal, or weak. Two clock cycles are required to complete the write operation in the extended mode register. The mode register contents can be changed using the same command and clock cycle requirements during operation as long as all banks are in the idle state. A0 is used for DLL enable or disable. "High" on BA0 is used for EMRS. Refer to the table for specific codes.

Table 11. Extended Mode Register Bitmap

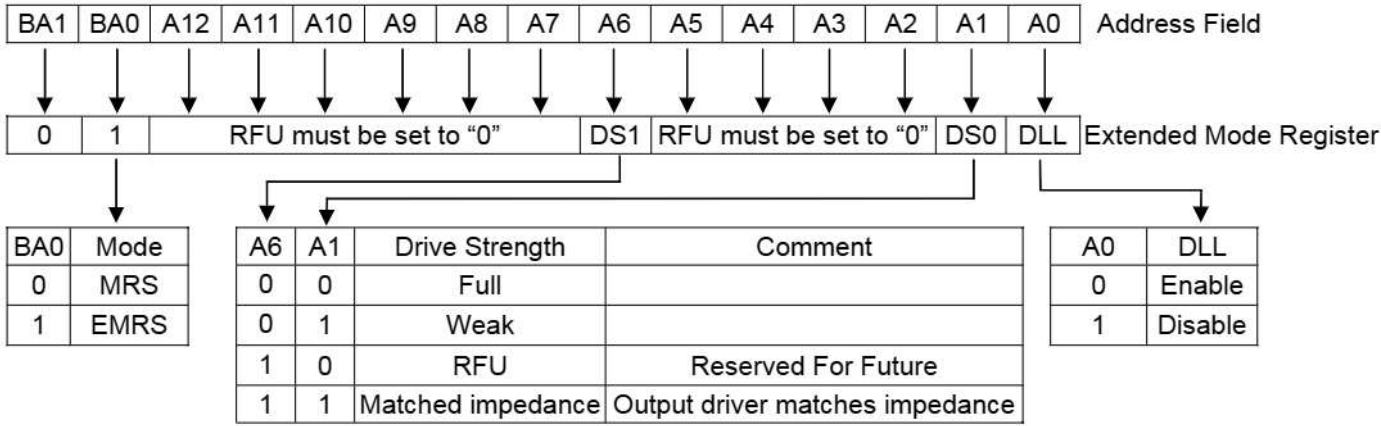


Table 12. Absolute Maximum Rating

Symbol	Item	Rating	Unit
VIN, VOUT	Input, Output Voltage	- 0.5~ VDDQ + 0.5	V
VDD, VDDQ	Power Supply Voltage	- 1~3.6	V
TA	Ambient Temperature	0~70	°C
TSTG	Storage Temperature	- 55~150	°C
TSOLDER	Soldering Temperature	260	°C
PD	Power Dissipation	1	W
IOS	Short Circuit Output Current	50	mA

Note1: Stress greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device.
Note2: These voltages are relative to Vss

Table 13. Recommended D.C. Operating Conditions (TA = 0 ~ 70 °C)

Symbol	Parameter	Min.	Max.	Unit	Note
VDD	Power Supply Voltage	2.3	2.7	V	
VDDQ	Power Supply Voltage (for I/O Buffer)	2.3	2.7	V	
VREF	Input Reference Voltage	0.49*VDDQ	0.51* VDDQ	V	
VIH (DC)	Input High Voltage (DC)	VREF + 0.15	VDDQ + 0.3	V	
VIL (DC)	Input Low Voltage (DC)	-0.3	VREF – 0.15	V	
VTT	Termination Voltage	VREF - 0.04	VREF + 0.04	V	
VIN (DC)	Input Voltage Level, CK and $\overline{\text{CK}}$ inputs	-0.3	VDDQ + 0.3	V	
VID (DC)	Input Different Voltage, CK and $\overline{\text{CK}}$ inputs	0.36	VDDQ + 0.6	V	
Ii	Input leakage current	-2	2	μA	
IOZ	Output leakage current	-5	5	μA	
IOH	Output High Current	-16.2	-	mA	VOH = 1.95V
IOL	Output Low Current	16.2	-	mA	VOL = 0.35V

Note : All voltages are referenced to Vss.

Table 14. Capacitance (VDD = 2.5V, f = 1MHz, TA = 25 °C)

Symbol	Parameter	Min.	Max.	Unit
CIN1	Input Capacitance (CK, $\overline{\text{CK}}$)	2	3	pF
CIN2	Input Capacitance (All other input-only pins)	2	3	pF
C _{I/O}	DQ, DQS, DM Input/Output Capacitance	4	5	pF

Note: These parameters are guaranteed by design, periodically sampled and are not 100% tested

Table 15. D.C. Characteristics (V_{DD} = 2.5V ± 0.2V, T_A = 0~70 °C)

Parameter & Test Condition	Symbol	-4	-5	Unit	Note
		Max.			
OPERATING CURRENT: One bank; Active-Precharge; t _{RC} =t _{RC} (min); t _{CK} =t _{CK} (min); DQ,DM and DQS inputs changing once per clock cycle; Address and control inputs changing once every two clock cycles.	IDD0	85	80	mA	
OPERATING CURRENT: One bank; BL=4; reads - Refer to the following page for detailed test conditions	IDD1	95	90	mA	
PRECHARGE POWER-DOWN STANDBY CURRENT: All banks idle; power-down mode; t _{CK} =t _{CK} (min); CKE = LOW	IDD2P	5	5	mA	
PRECHARGE FLOATING STANDBY CURRENT: CS = HIGH; all banks idle; CKE = HIGH; t _{CK} =t _{CK} (min); address and other control inputs changing once per clock cycle; V _{IN} = V _{REF} for DQ, DQS and DM	IDD2F	40	35	mA	
PRECHARGE QUIET STANDBY CURRENT: CS =HIGH; all banks idle; CKE =HIGH; t _{CK} =t _{CK} (min) address and other control inputs stable at ≥ V _{IH} (min) or ≤ V _{IL} (max); V _{IN} = V _{REF} for DQ, DQS and DM	IDD2Q	40	35	mA	
ACTIVE POWER-DOWN STANDBY CURRENT : one bank active; power-down mode; CKE=LOW; t _{CK} =t _{CK} (min)	IDD3P	20	20	mA	
ACTIVE STANDBY CURRENT : $\overline{CS}$ =HIGH;CKE=HIGH; one bank active ; t _{RC} =t _{RC} (max);t _{CK} =t _{CK} (min);Address and control inputs changing once per clock cycle; DQ,DQS,and DM inputs changing twice per clock cycle	IDD3N	65	65	mA	
OPERATING CURRENT BURST READ : BL=2; READS; Continuous burst; one bank active; Address and control inputs changing once per clock cycle; t _{CK} =t _{CK} (min); I _{out} =0mA;50% of data changing on every transfer	IDD4R	150	130	mA	
OPERATING CURRENT BURST Write : BL=2; WRITES; Continuous Burst ;one bank active; address and control inputs changing once per clock cycle; t _{CK} =t _{CK} (min); DQ,DQS,and DM changing twice per clock cycle; 50% of data changing on every transfer	IDD4W	150	130	mA	
AUTO REFRESH CURRENT : t _{RC} =t _{RFC} (min); t _{CK} =t _{CK} (min)	IDD5	160	140	mA	
SELF REFRESH CURRENT: Self Refresh Mode ; CKE ≤ 0.2V;t _{CK} =t _{CK} (min)	IDD6	6	6	mA	1
BURST OPERATING CURRENT 4 bank operation: Four bank interleaving READs; BL=4;with Auto Precharge; t _{RC} =t _{RC} (min); t _{CK} =t _{CK} (min); Address and control inputs change only during Active, READ , or WRITE command	IDD7	230	210	mA	

Table 16. Electrical Characteristics and Recommended A.C.Operating Condition
(VDD = 2.5V ± 0.2V, TA = 0~70 °C)

Symbol	Parameter		-4		-5		Unit	Note
			Min.	Max.	Min.	Max.		
tCK	Clock cycle time	CL = 2	-	-	7.5	12	ns	
		CL = 2.5	-	-	6	12	ns	
		CL = 3	4	12	5	12	ns	
tCH	Clock high level width		0.45	0.55	0.45	0.55	tCK	
tCL	Clock low level width		0.45	0.55	0.45	0.55	tCK	
tHP	Clock half period		tCLMIN or tCHMIN	-	tCLMIN or tCHMIN	-	ns	2
tHZ	Data-out-high impedance time from CK, $\overline{CK}$		-	0.7	-	0.7	ns	3
tlZ	Data-out-low impedance time from CK, $\overline{CK}$		-0.7	0.7	-0.7	0.7	ns	3
tDQSK	DQS-out access time from CK, $\overline{CK}$		-0.6	0.6	-0.6	0.6	ns	
tAC	Output access time from CK, $\overline{CK}$		-0.7	0.7	-0.7	0.7	ns	
tDQSQ	DQS-DQ Skew		-	0.4	-	0.4	ns	
trPRE	Read preamble		0.9	1.1	0.9	1.1	tCK	
trPST	Read postamble		0.4	0.6	0.4	0.6	tCK	
tDQSS	CK to valid DQS-in		0.8	1.2	0.72	1.25	tCK	
twPRES	DQS-in setup time		0	-	0	-	ns	4
twPRE	DQS Write preamble		0.25	-	0.25	-	tCK	
twPST	DQS write postamble		0.4	0.6	0.4	0.6	tCK	5
tDQSH	DQS in high level pulse width		0.35	-	0.35	-	tCK	
tDQSL	DQS in low level pulse width		0.35	-	0.35	-	tCK	
tIS	Address and Control input setup time		0.7	-	0.7	-	ns	6
tIH	Address and Control input hold time		0.7	-	0.7	-	ns	6
tDS	DQ & DM setup time to DQS		0.4	-	0.4	-	ns	
tDH	DQ & DM hold time to DQS		0.4	-	0.4	-	ns	
tQH	DQ/DQS output hold time from DQS		tHP - tQHS	-	tHP - tQHS	-	ns	
tRC	Row cycle time		55	-	55	-	ns	
trFC	Refresh row cycle time		70	-	70	-	ns	
trAS	Row active time		40	70K	40	70K	ns	
trCD	Active to Read or Write delay		15	-	15	-	ns	
trP	Row precharge time		15	-	15	-	ns	
trRD	Row active to Row active delay		8	-	10	-	ns	
tWR	Write recovery time		12	-	15	-	ns	
twTR	Internal Write to Read Command Delay		2	-	2	-	tCK	
tMRD	Mode register set cycle time		8	-	10	-	ns	
trEFI	Average Periodic Refresh interval		-	7.8	-	7.8	μs	7
txSRD	Self refresh exit to read command delay		200	-	200	-	tCK	
txSNR	Self refresh exit to non-read command delay		75	-	75	-	ns	
tDAL	Auto Precharge write recovery + precharge time		tWR+tRP	-	tWR+tRP	-	ns	
tDIPW	DQ and DM input pulse width		1.75	-	1.75	-	ns	
tIPW	Control and Address input pulse width		2.2	-	2.2	-	ns	
tQHS	Data Hold Skew Factor		-	0.5	-	0.5	ns	
tDSS	DQS falling edge to CK setup time		0.2	-	0.2	-	tCK	
tDSH	DQS falling edge hold time from CK		0.2	-	0.2	-	tCK	
tRAP	Active to Autoprecharge Delay		tRCD or tRASmin	-	tRCD or tRASmin	-	ns	

Table 17. Recommended A.C. Operating Conditions (V_{DD} = 2.5V ± 0.2V, T_A = 0~70 °C)

Symbol	Parameter	Min.	Max.	Unit
V _{IH} (AC)	Input High Voltage (AC)	V _{REF} + 0.31	-	V
V _{IL} (AC)	Input Low Voltage (AC)	-	V _{REF} – 0.31	V
V _{ID} (AC)	Input Different Voltage, CK and $\overline{CK}$ inputs	0.7	V _{DDQ} + 0.6	V
V _{IX} (AC)	Input Crossing Point Voltage, CK and $\overline{CK}$ inputs	0.5*V _{DDQ} -0.2	0.5*V _{DDQ} +0.2	V

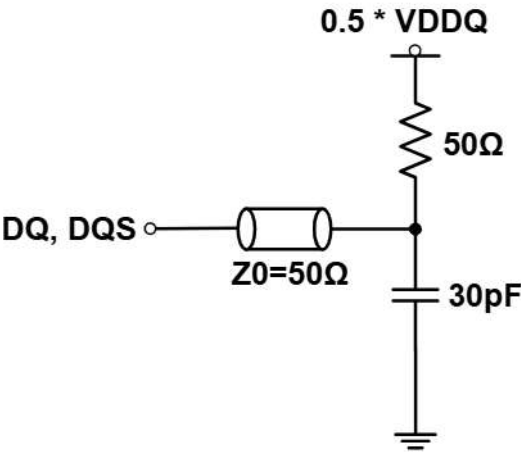
Note:

- 1) Enables on-chip refresh and address counters.
- 2) Min(t_{CL}, t_{CH}) refers to the smaller of the actual clock low time and actual clock high time as provided to the device.
- 3) t_{HZ} and t_{LZ} transitions occur in the same access time windows as valid data transitions. These parameters are not referenced to a specific voltage level, but specify when the device output is no longer driving(HZ), or begins driving(LZ).
- 4) The specific requirement is that DQS be valid (High, Low, or at some point on a valid transition) on or before this CLK edge. A valid transition is defined as monotonic, and meeting the input slew rate specifications of the device. When no writes were previously in progress on the bus, DQS will be transitioning from High-Z to logic LOW. If a previous write was in progress, DQS could be HIGH, LOW, or transitioning from HIGH to LOW at this time, depending on t_{DQSS}.
- 5) The maximum limit for this parameter is not a device limit. The device will operate with a greater value for this parameter, but system performance (bus turnaround) will degrade accordingly.
- 6) For command/address and CK & $\overline{CK}$ slew rate ≥ 1.0V/ns.
- 7) A maximum of eight AUTO REFRESH commands can be posted to any given DDR SDRAM device.
- 8) Power-up sequence is described in Note 10
- 9) A.C. Test Conditions

Table 17. SSTL_2 Interface

Reference Level of Output Signals (V _{REF})	0.5 * V _{DDQ}
Output Load	Reference to the Test Load
Input Signal Levels	V _{REF} +0.31 V / V _{REF} -0.31 V
Input Signals Slew Rate	1 V/ns
Reference Level of Input Signals	0.5 * V _{DDQ}

Figure 3. SSTL_2 A.C. Test Load



10) Power up Sequence

Power up must be performed in the following sequence.

- 1) Apply power to V_{DD} before or at the same time as V_{DDQ} , V_{TT} and V_{REF} when all input signals are held "NOP" state and maintain CKE "LOW".
- 2) Start clock and maintain stable condition for minimum 200 μ s.
- 3) Issue a "NOP" command and keep CKE "HIGH"
- 4) Issue a "Precharge All" command.
- 5) Issue EMRS – enable DLL.
- 6) Issue MRS – reset DLL. (An additional 200 clock cycles are required to lock the DLL).
- 7) Precharge all banks of the device.
- 8) Issue two or more Auto Refresh commands.
- 9) Issue MRS – with A8 to low to initialize the mode register.

Timing Waveforms

Figure 4. Activating a Specific Row in a Specific Bank

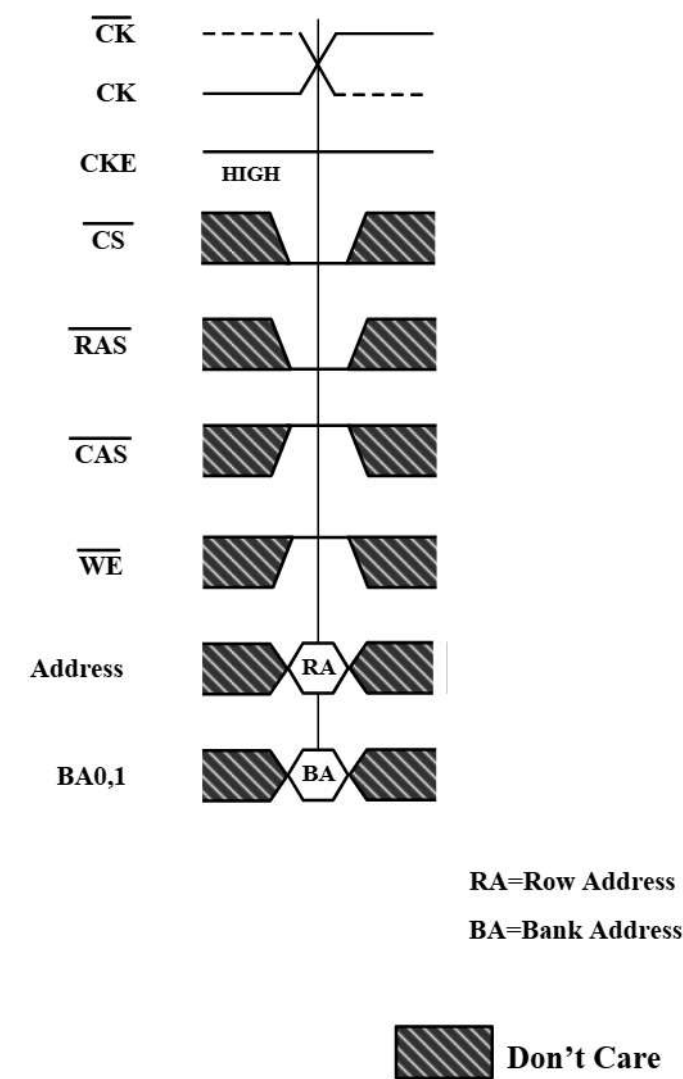


Figure 5. tRCD and tRRD Definition

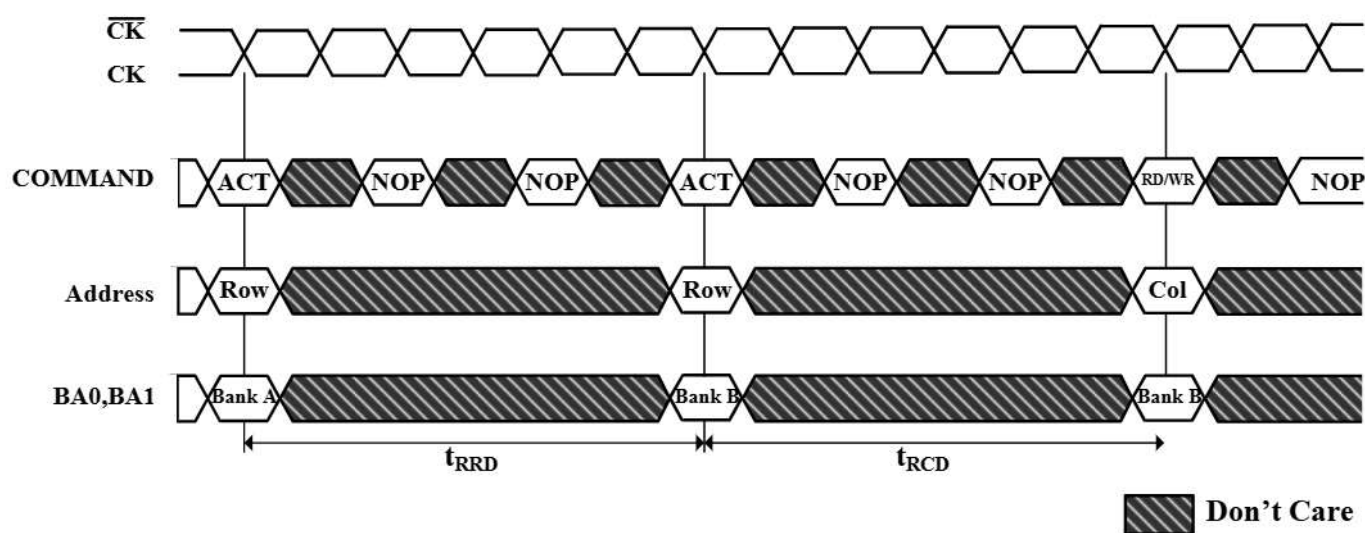


Figure 6. READ Command

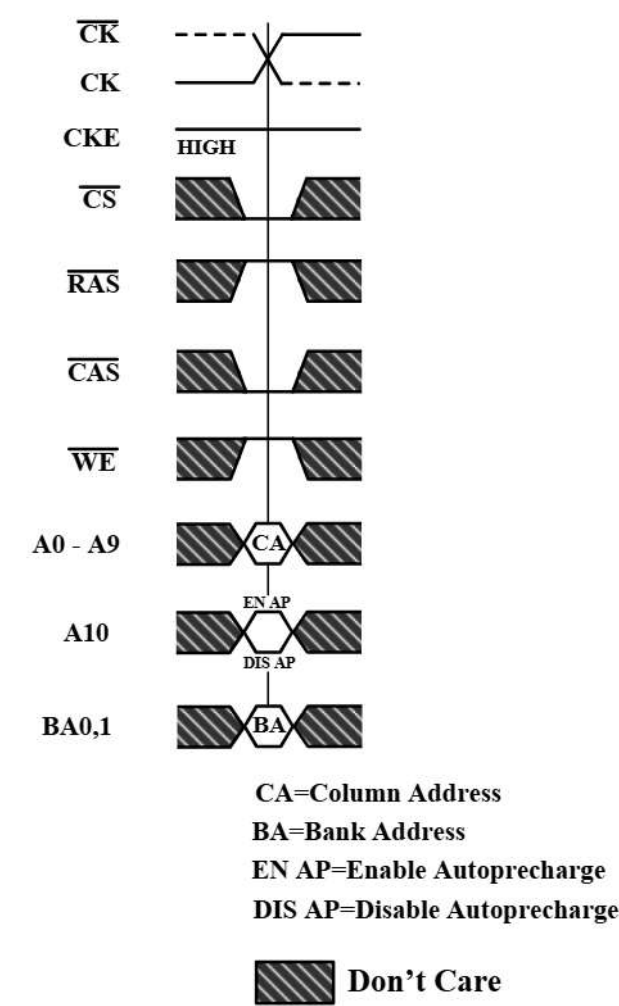
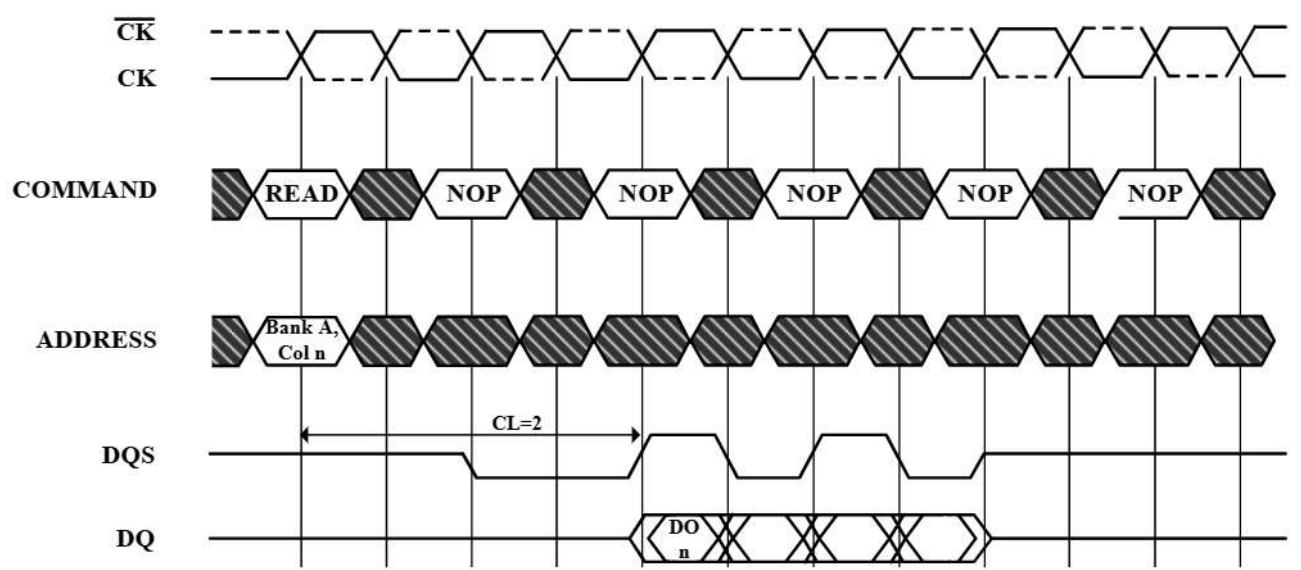


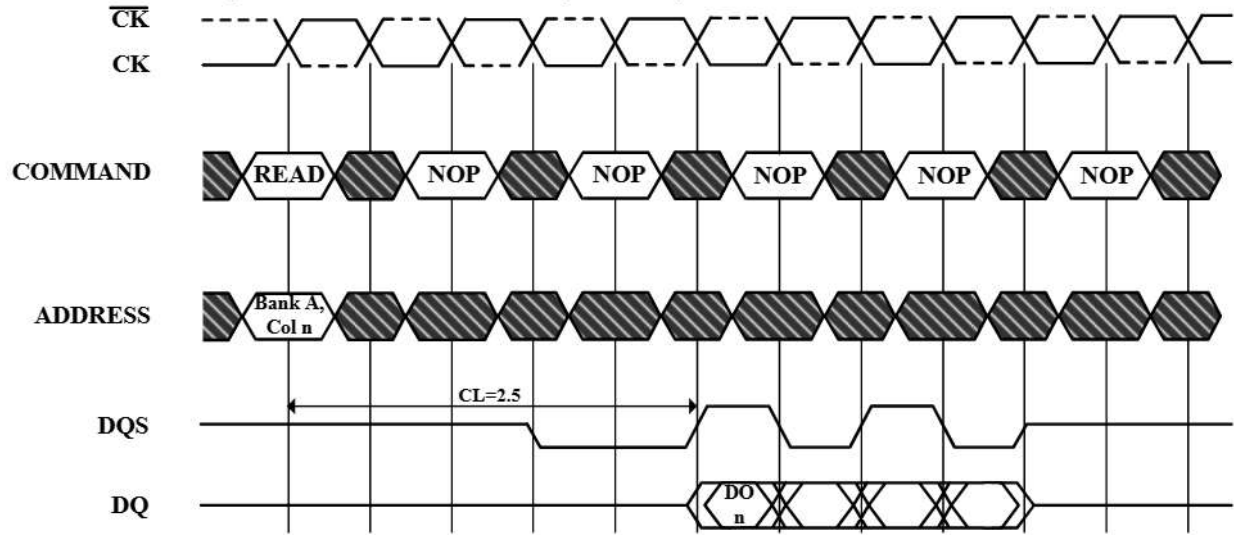
Figure 7. Read Burst Required CAS Latencies (CL=2)



DO n=Data Out from column n
Burst Length=4
3 subsequent elements of Data Out appear in the programmed order following DO n

Don't Care

Read Burst Required CAS Latencies (CL=2.5)



DO n=Data Out from column n
Burst Length=4
3 subsequent elements of Data Out appear in the programmed order following DO n

Don't Care

Read Burst Required CAS Latencies (CL=3)

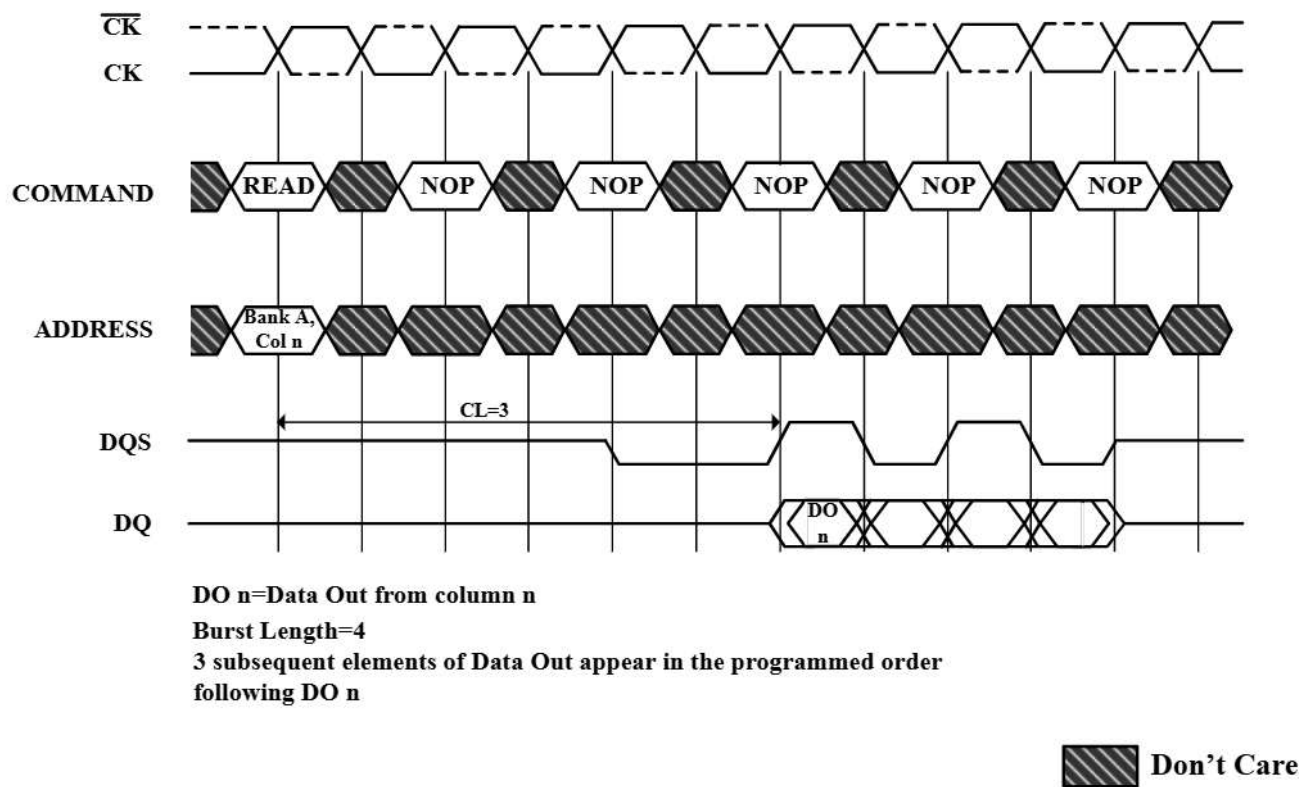
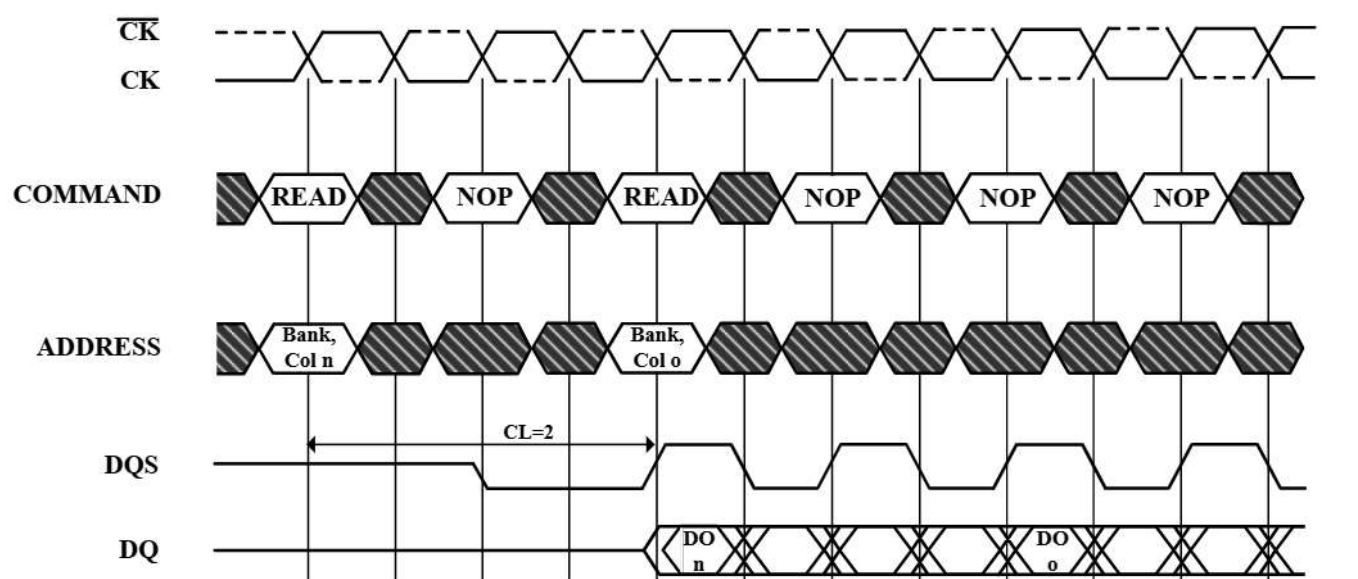


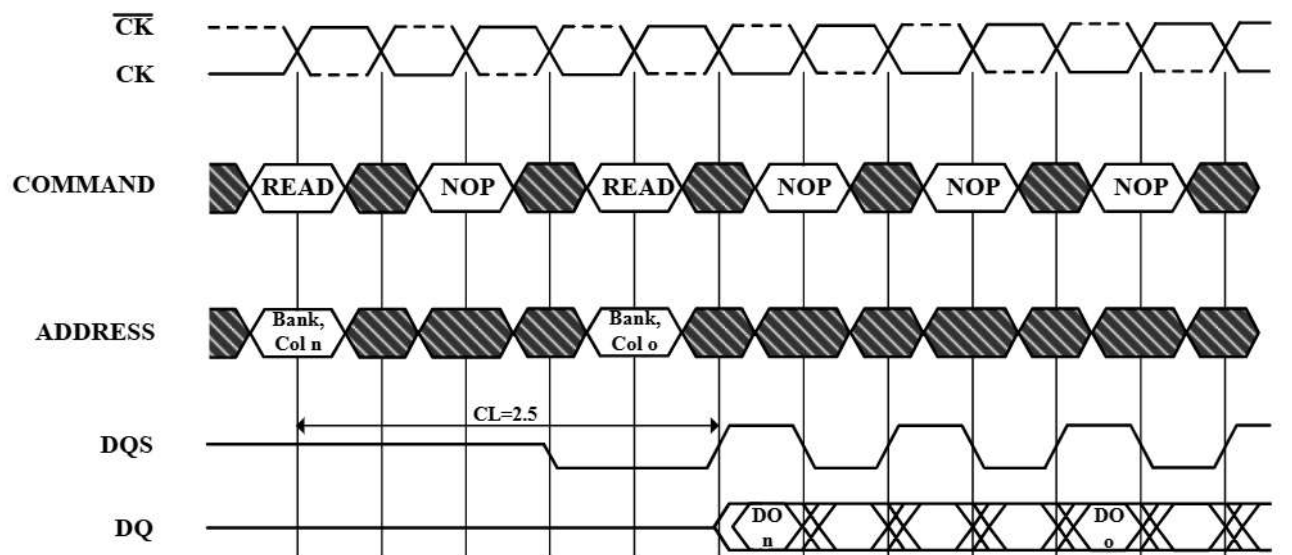
Figure 8. Consecutive Read Bursts Required CAS Latencies (CL=2)



DO n (or o)=Data Out from column n (or column o)
Burst Length=4 or 8 (if 4, the bursts are concatenated; if 8, the second burst interrupts the first)
3 subsequent elements of Data Out appear in the programmed order following DO n
3 (or 7) subsequent elements of Data Out appear in the programmed order following DO o
Read commands shown must be to the same device

Don't Care

Consecutive Read Bursts Required CAS Latencies (CL=2.5)



DO n (or o)=Data Out from column n (or column o)
Burst Length=4 or 8 (if 4, the bursts are concatenated; if 8, the second burst interrupts the first)
3 subsequent elements of Data Out appear in the programmed order following DO n
3 (or 7) subsequent elements of Data Out appear in the programmed order following DO o
Read commands shown must be to the same device

 Don't Care

Consecutive Read Bursts Required CAS Latencies (CL=3)

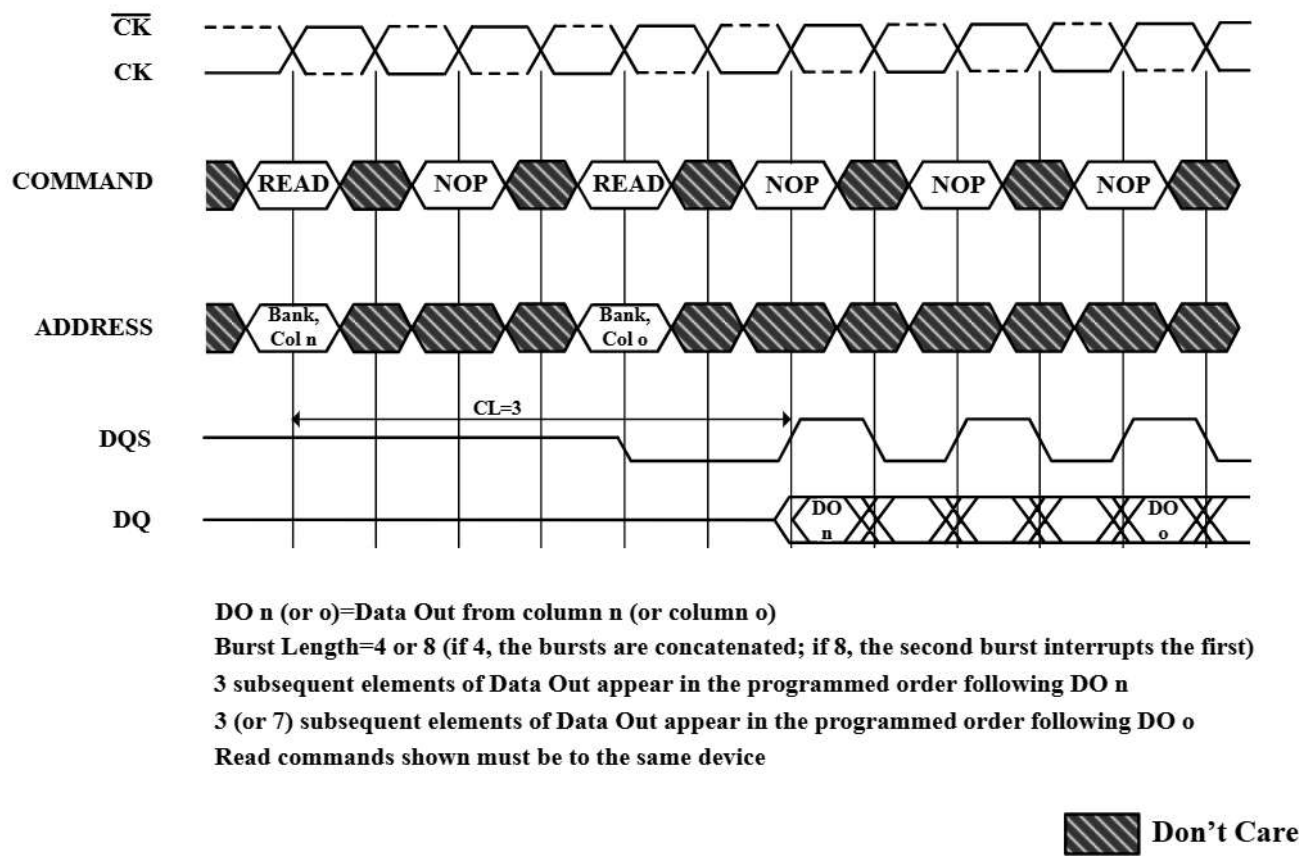
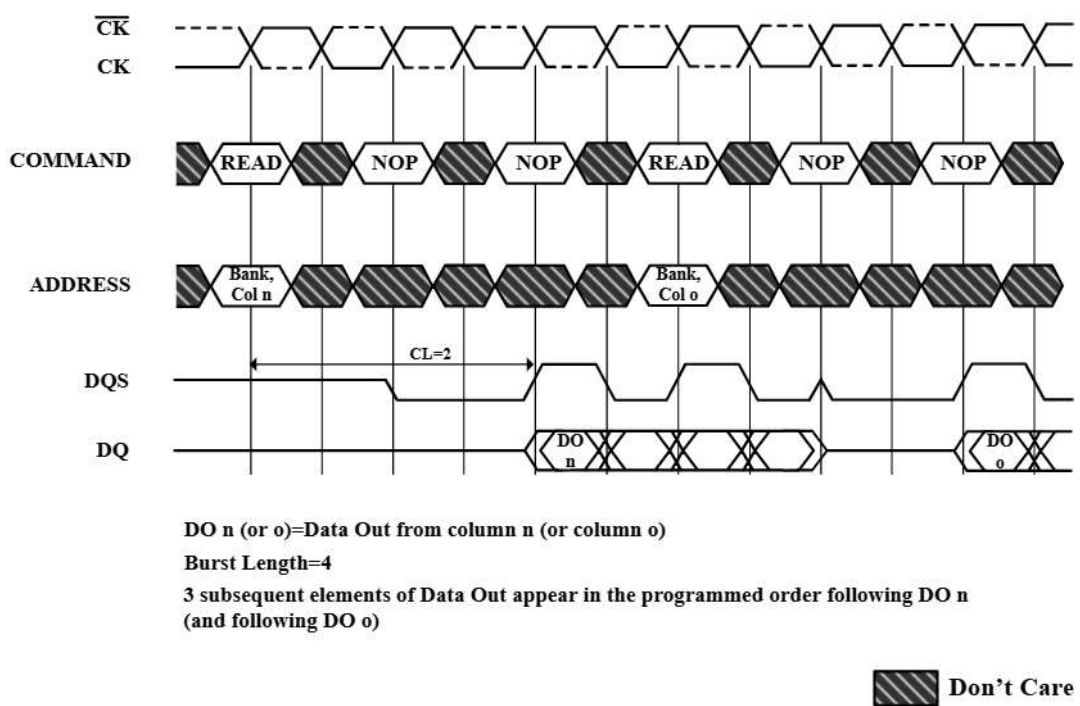
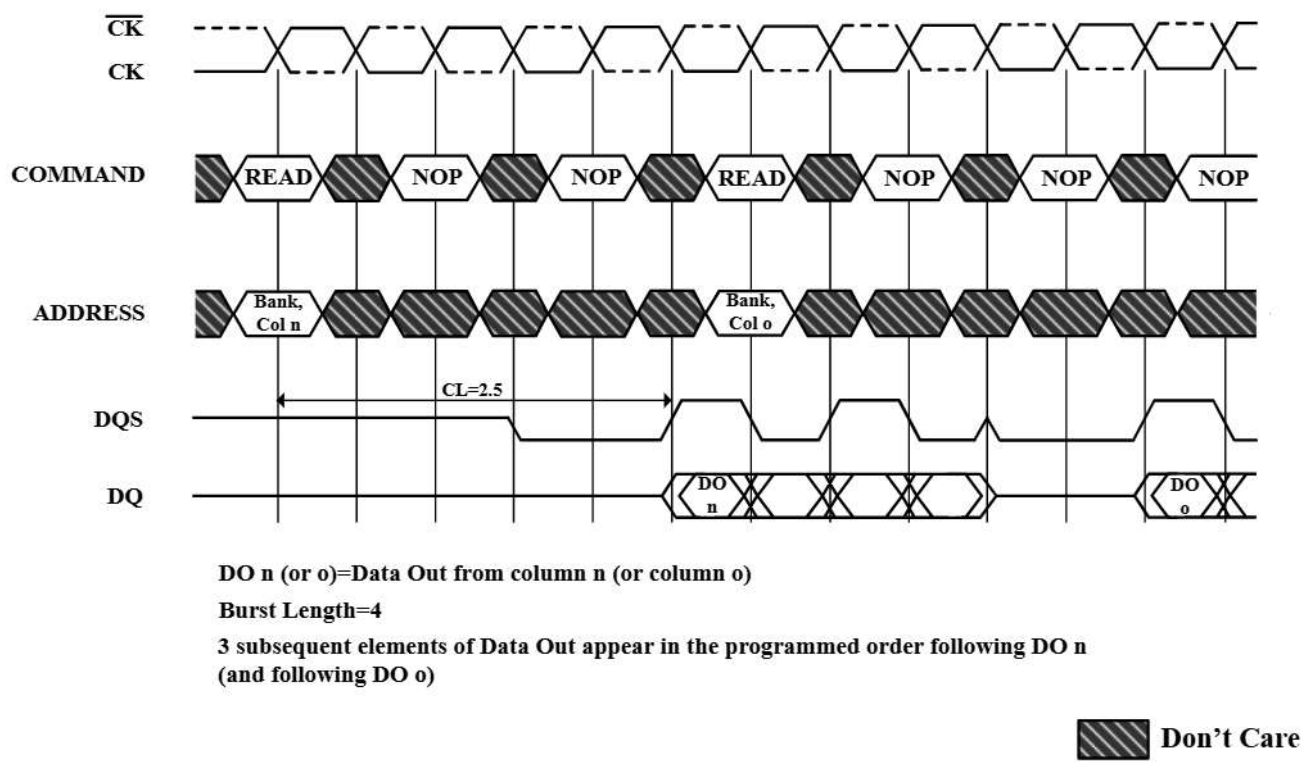


Figure 9. Non-Consecutive Read Bursts Required CAS Latencies (CL=2)



Non-Consecutive Read Bursts Required CAS Latencies (CL=2.5)



Non-Consecutive Read Bursts Required CAS Latencies (CL=3)

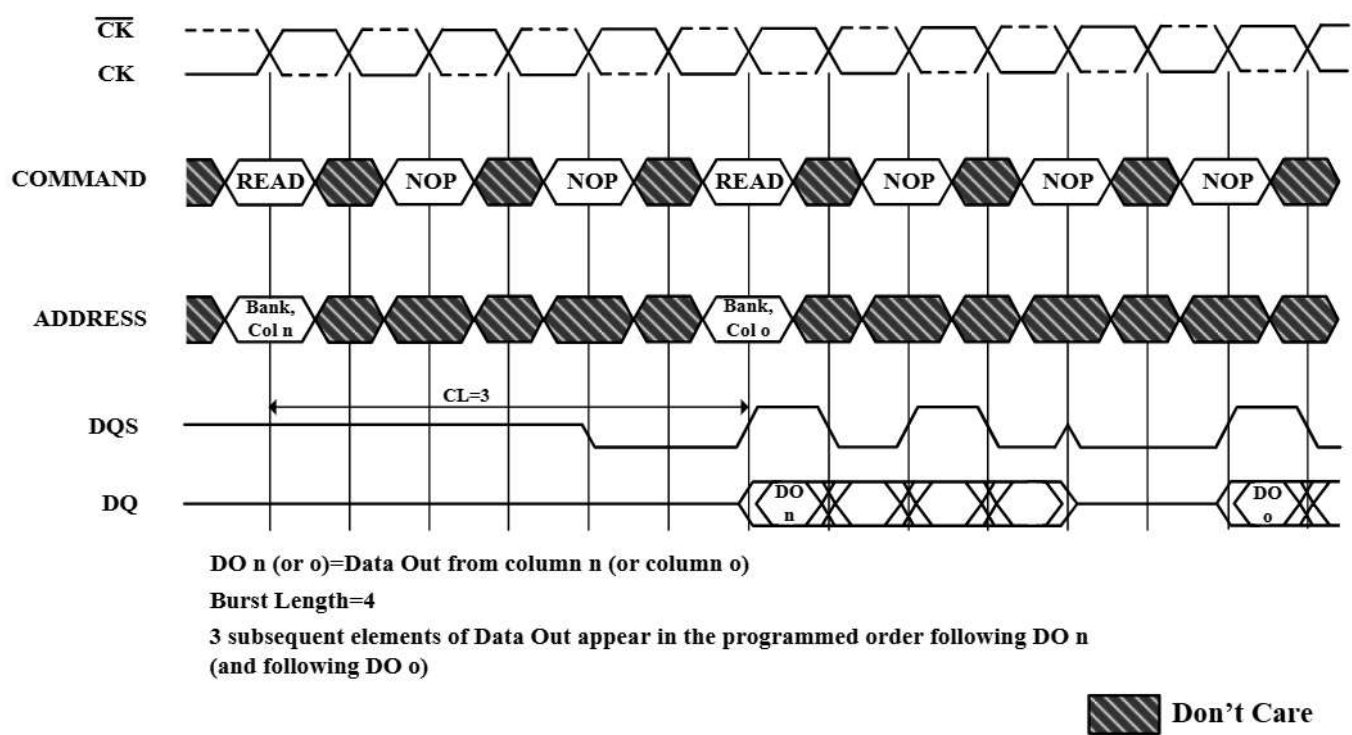
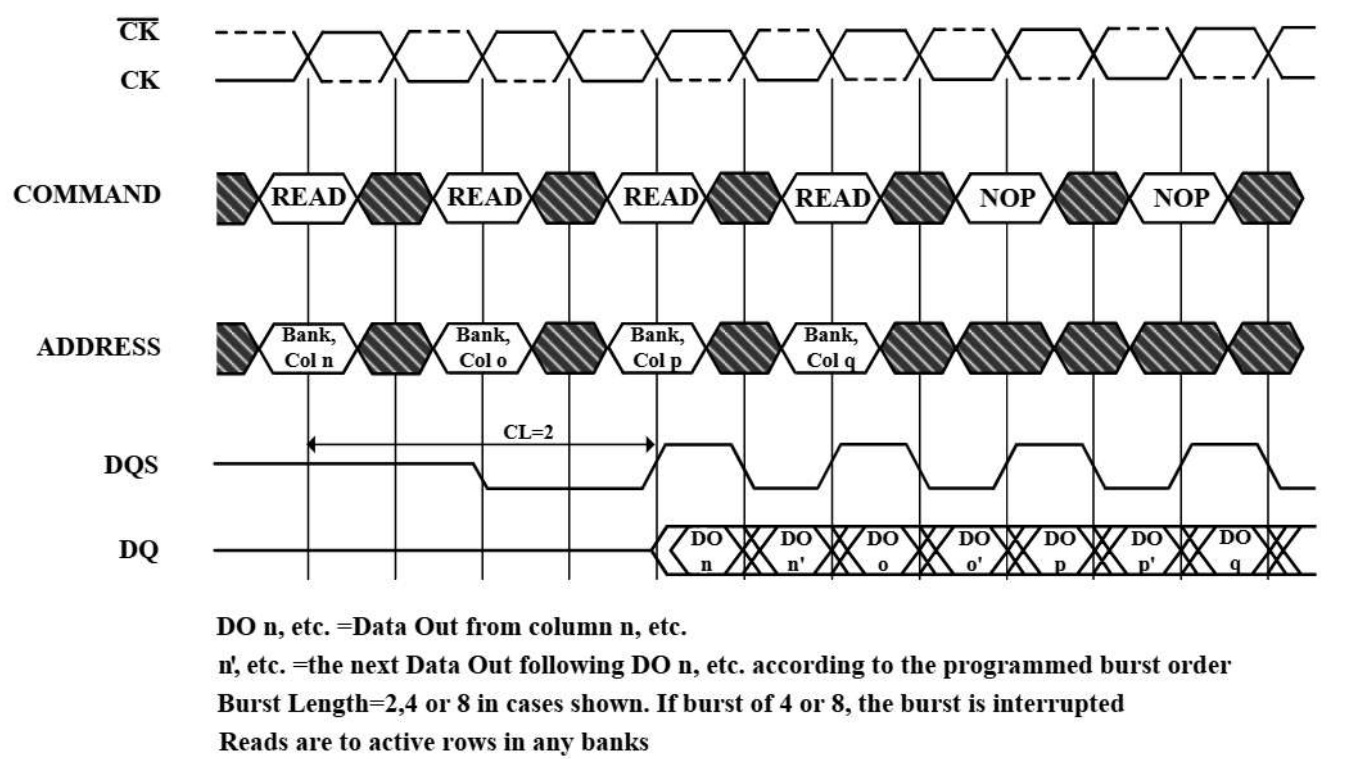
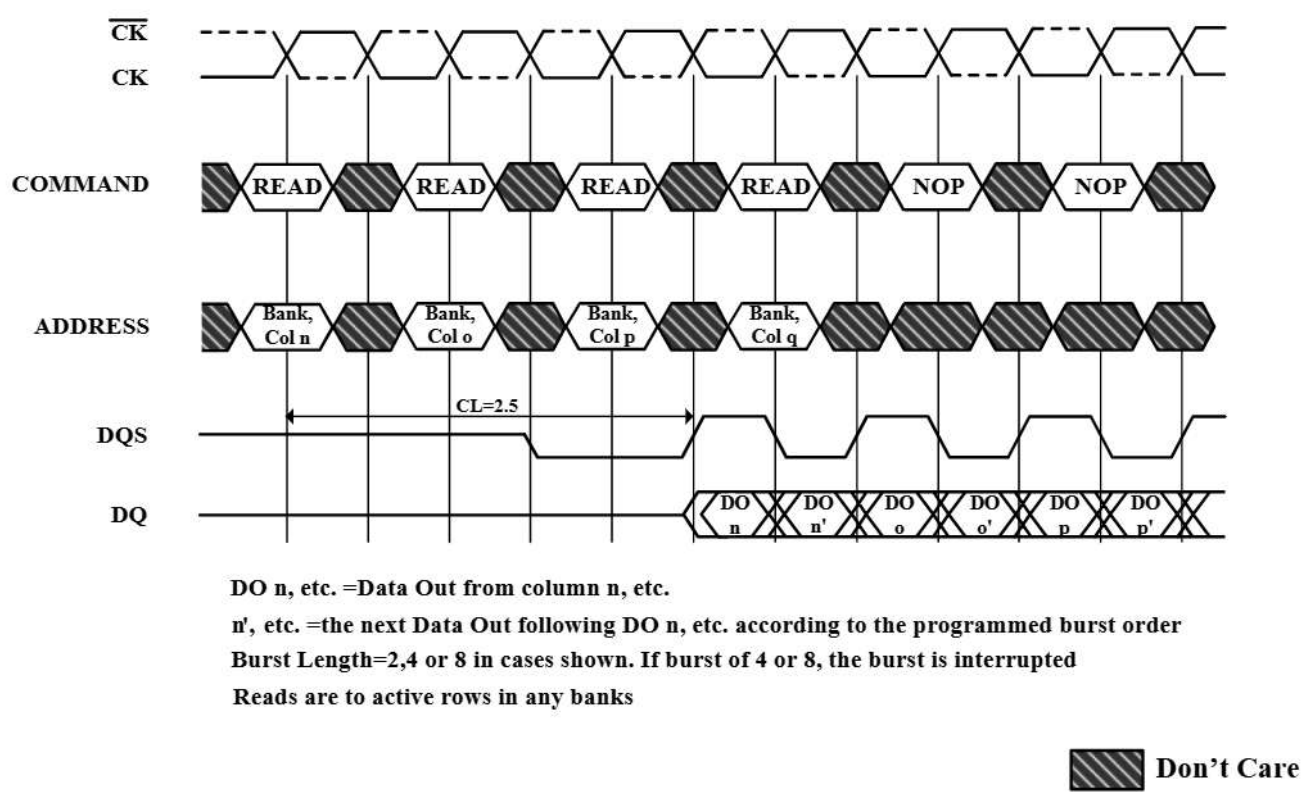


Figure 10. Random Read Accesses Required CAS Latencies (CL=2)



Random Read Accesses Required CAS Latencies (CL=2.5)



Random Read Accesses Required CAS Latencies (CL=3)

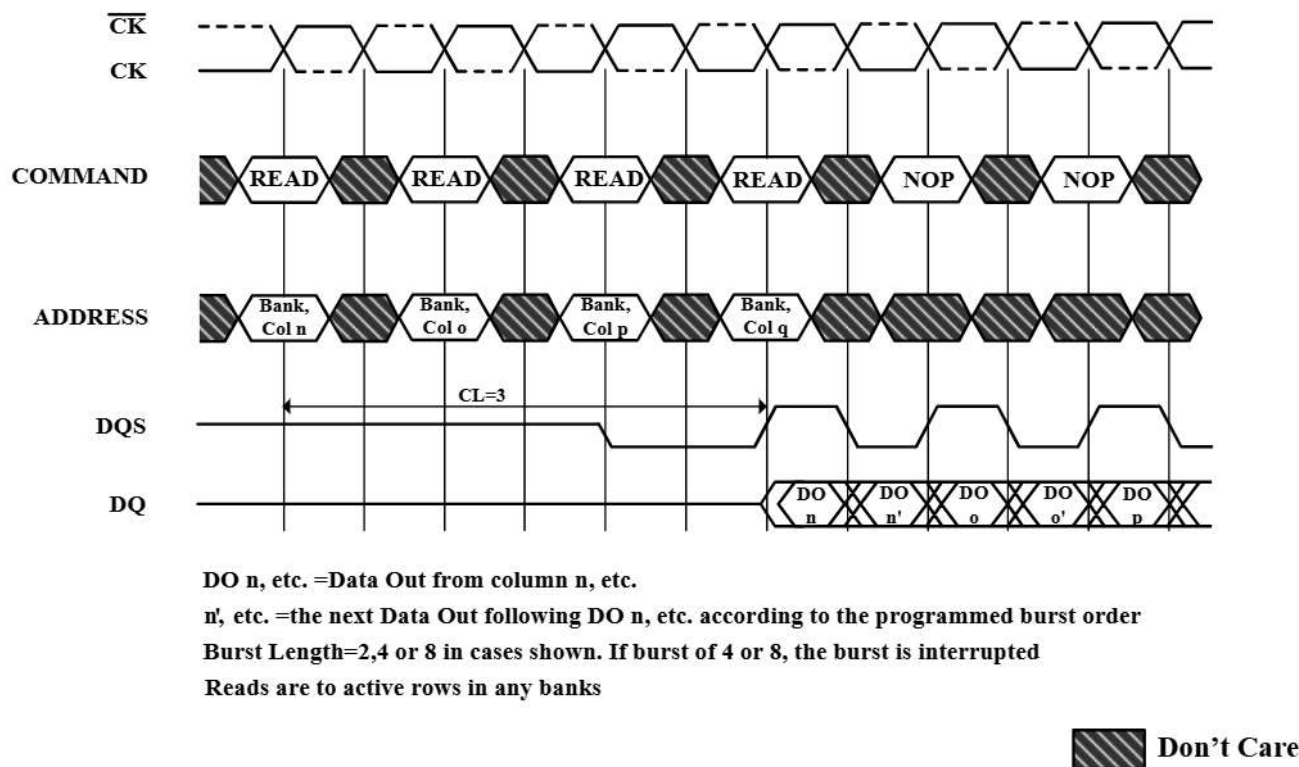
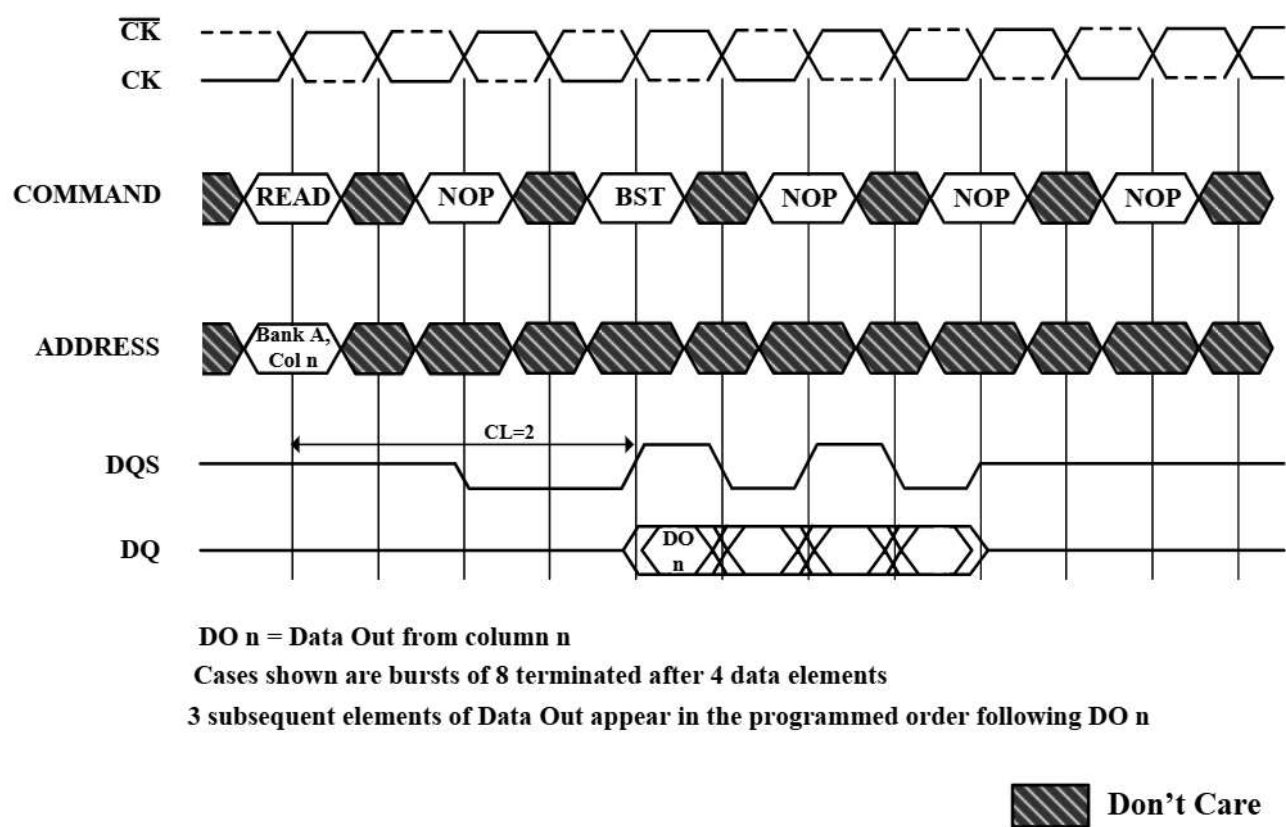
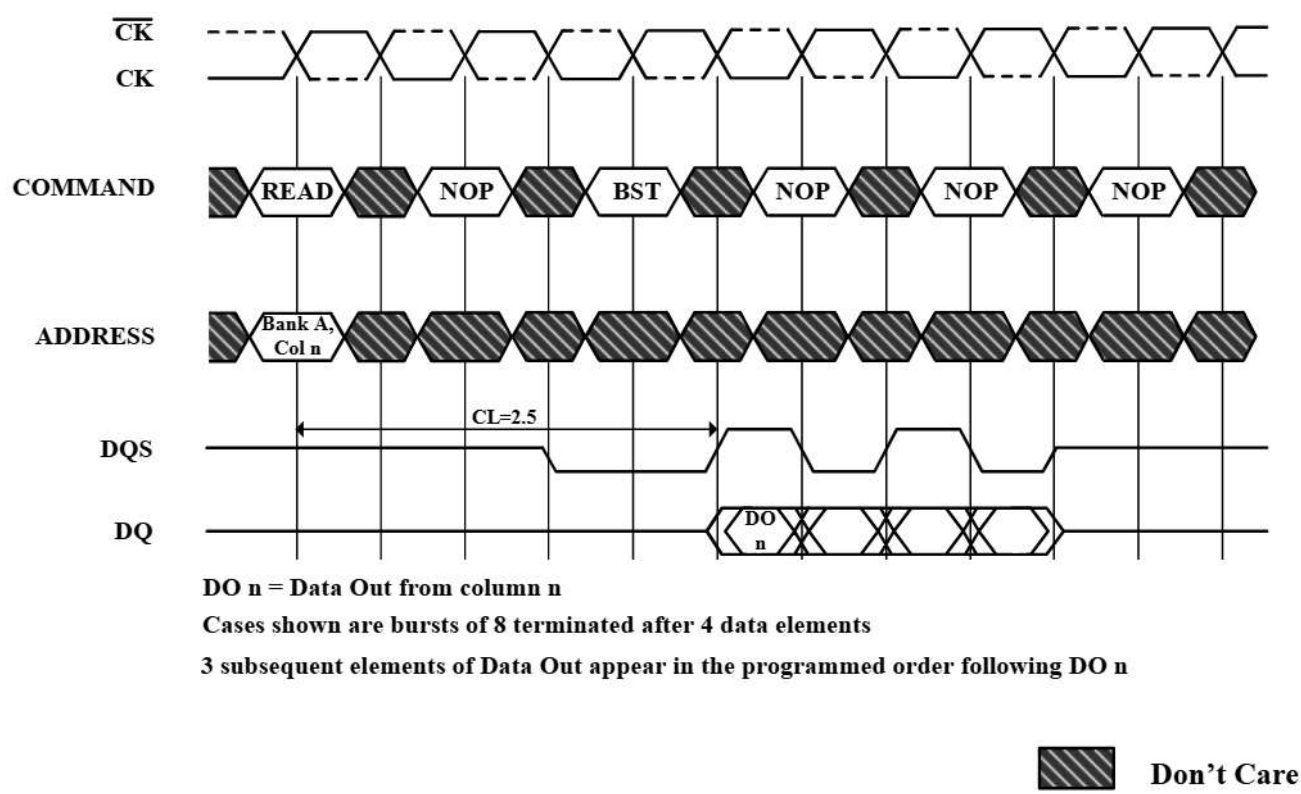


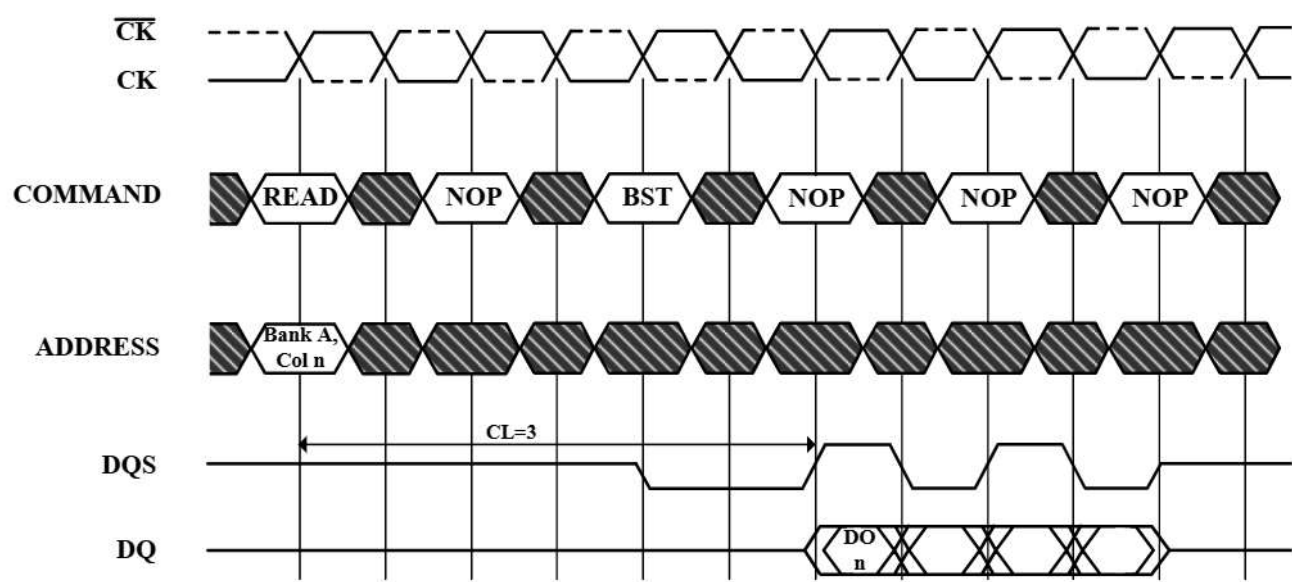
Figure 11. Terminating a Read Burst Required CAS Latencies (CL=2)



Terminating a Read Burst Required CAS Latencies (CL=2.5)



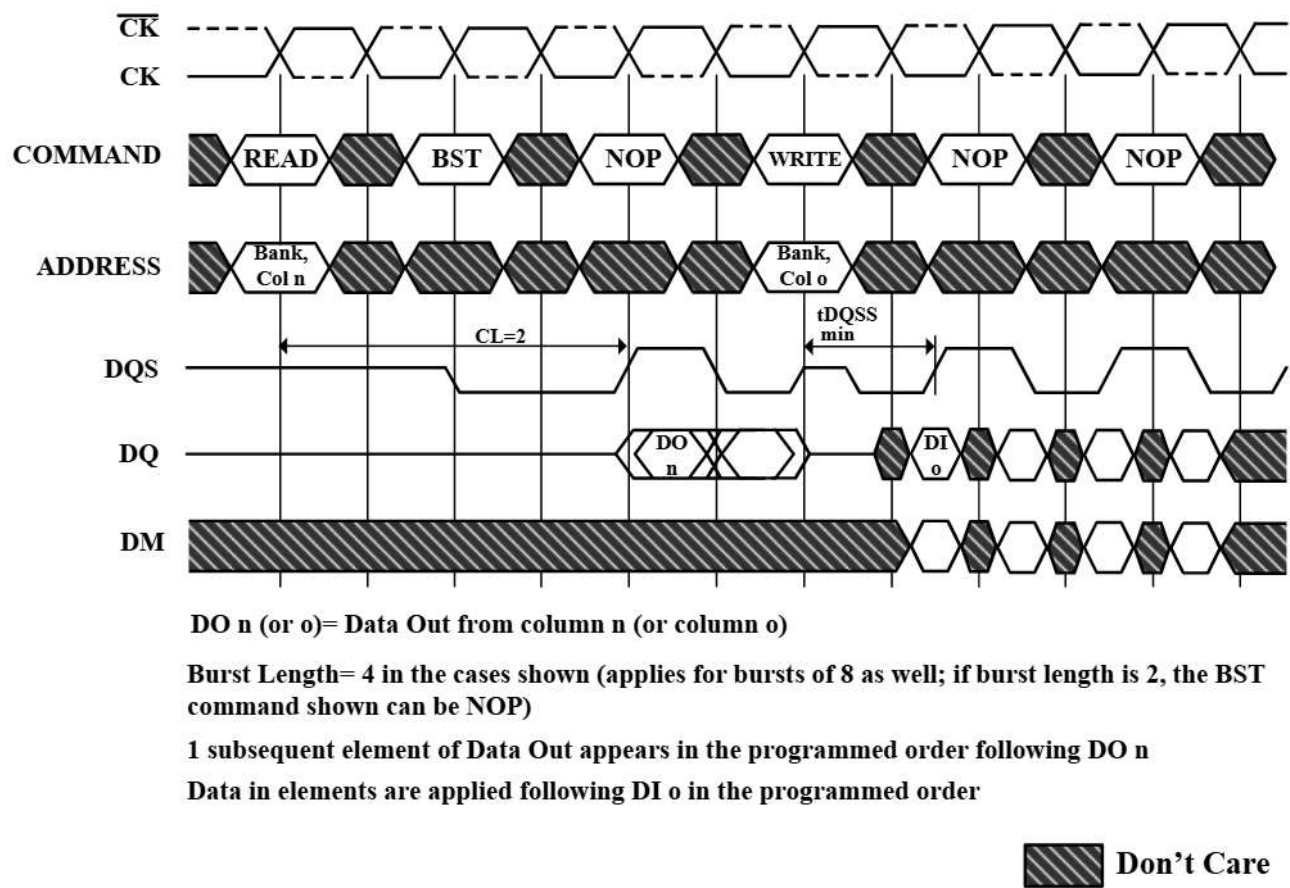
Terminating a Read Burst Required CAS Latencies (CL=3)



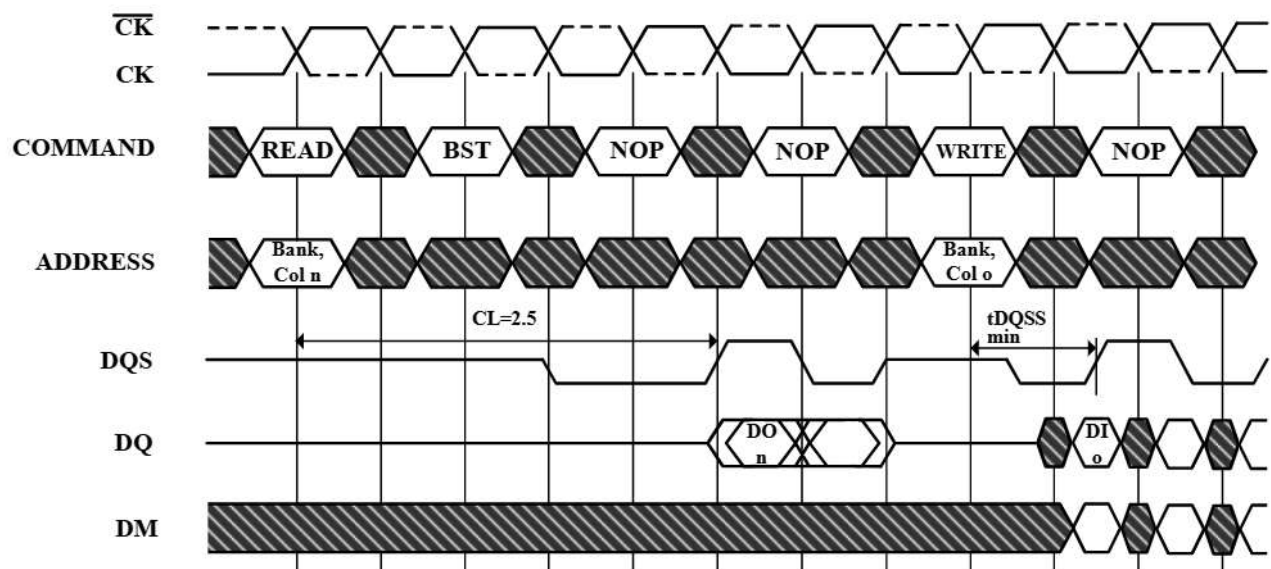
DO n = Data Out from column n
Cases shown are bursts of 8 terminated after 4 data elements
3 subsequent elements of Data Out appear in the programmed order following DO n

 Don't Care

Figure 12. Read to Write Required CAS Latencies (CL=2)



Read to Write Required CAS Latencies (CL=2.5)



DO n (or o)= Data Out from column n (or column o)

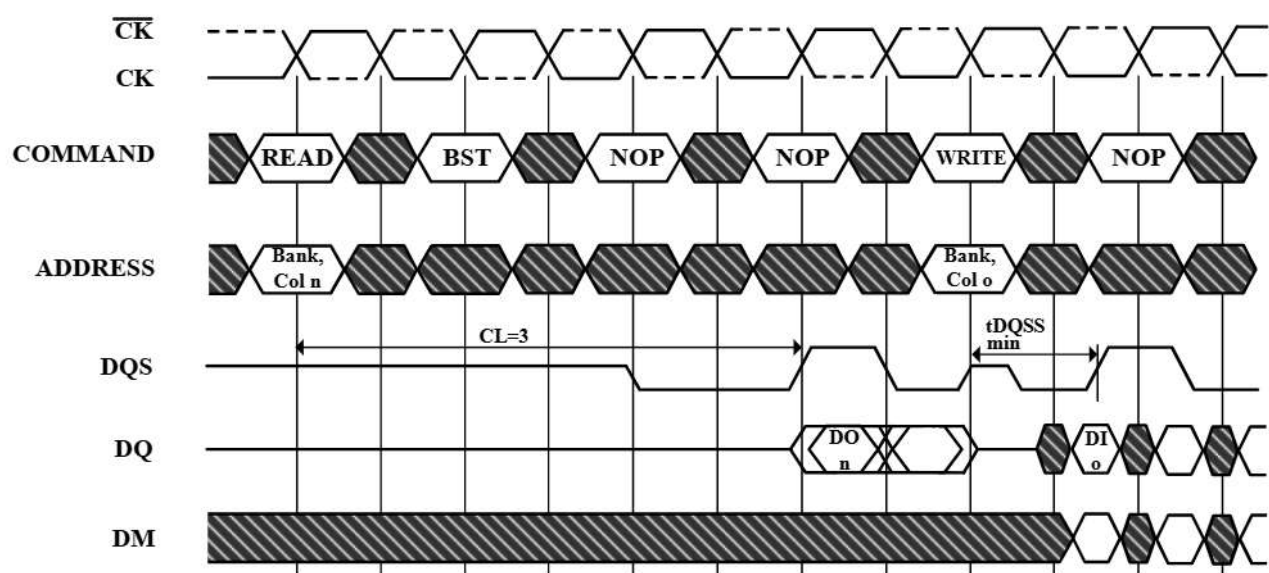
Burst Length= 4 in the cases shown (applies for bursts of 8 as well; if burst length is 2, the BST command shown can be NOP)

1 subsequent element of Data Out appears in the programmed order following DO n

Data in elements are applied following DI o in the programmed order

 Don't Care

Read to Write Required CAS Latencies (CL=3)



DO n (or o)= Data Out from column n (or column o)

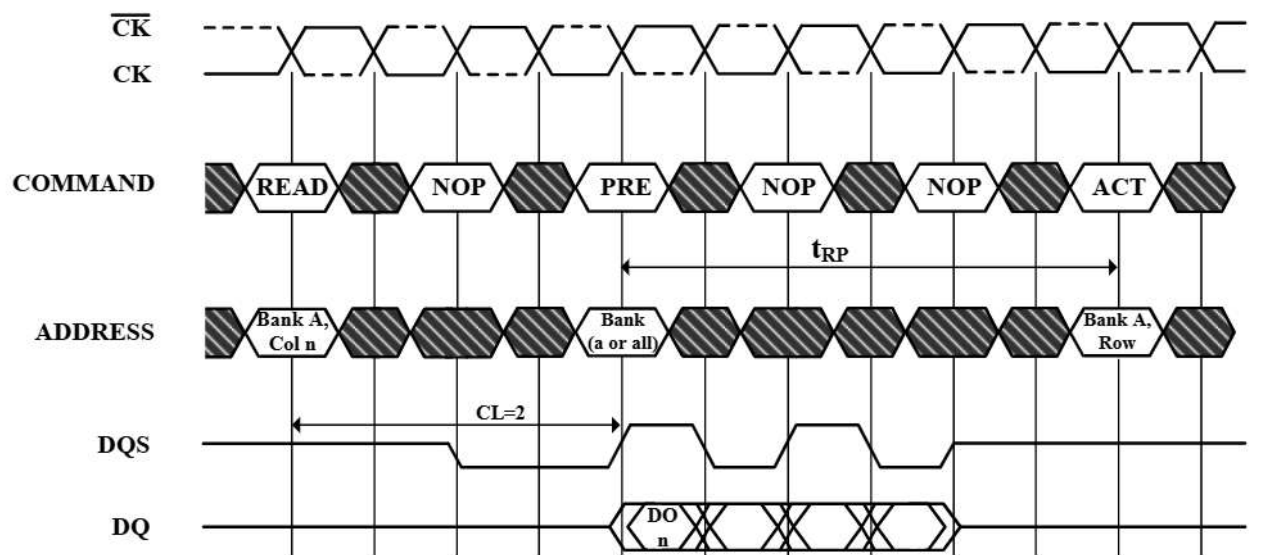
Burst Length= 4 in the cases shown (applies for bursts of 8 as well; if burst length is 2, the BST command shown can be NOP)

1 subsequent element of Data Out appears in the programmed order following DO n

Data in elements are applied following DI o in the programmed order

 Don't Care

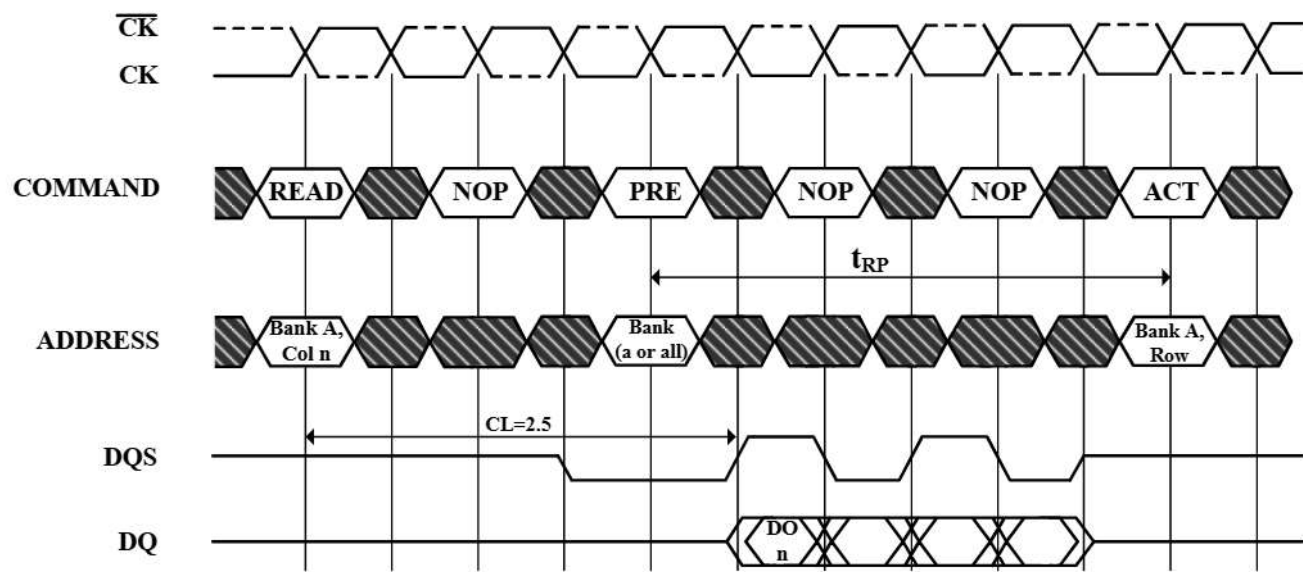
Figure 13. Read to Precharge Required CAS Latencies (CL=2)



DO n = Data Out from column n
Cases shown are either uninterrupted bursts of 4, or interrupted bursts of 8
3 subsequent elements of Data Out appear in the programmed order
following DO n
Precharge may be applied at (BL/2) tCK after the READ command
Note that Precharge may not be issued before tRAS ns after the ACTIVE
command for applicable banks
The Active command may be applied if tRC has been met

Don't Care

Read to Precharge Required CAS Latencies (CL=2.5)



DO n = Data Out from column n
Cases shown are either uninterrupted bursts of 4, or interrupted bursts of 8
3 subsequent elements of Data Out appear in the programmed order following DO n
Precharge may be applied at (BL/2) tCK after the READ command
Note that Precharge may not be issued before tRAS ns after the ACTIVE command for applicable banks
The Active command may be applied if tRC has been met

 Don't Care

Read to Precharge Required CAS Latencies (CL=3)

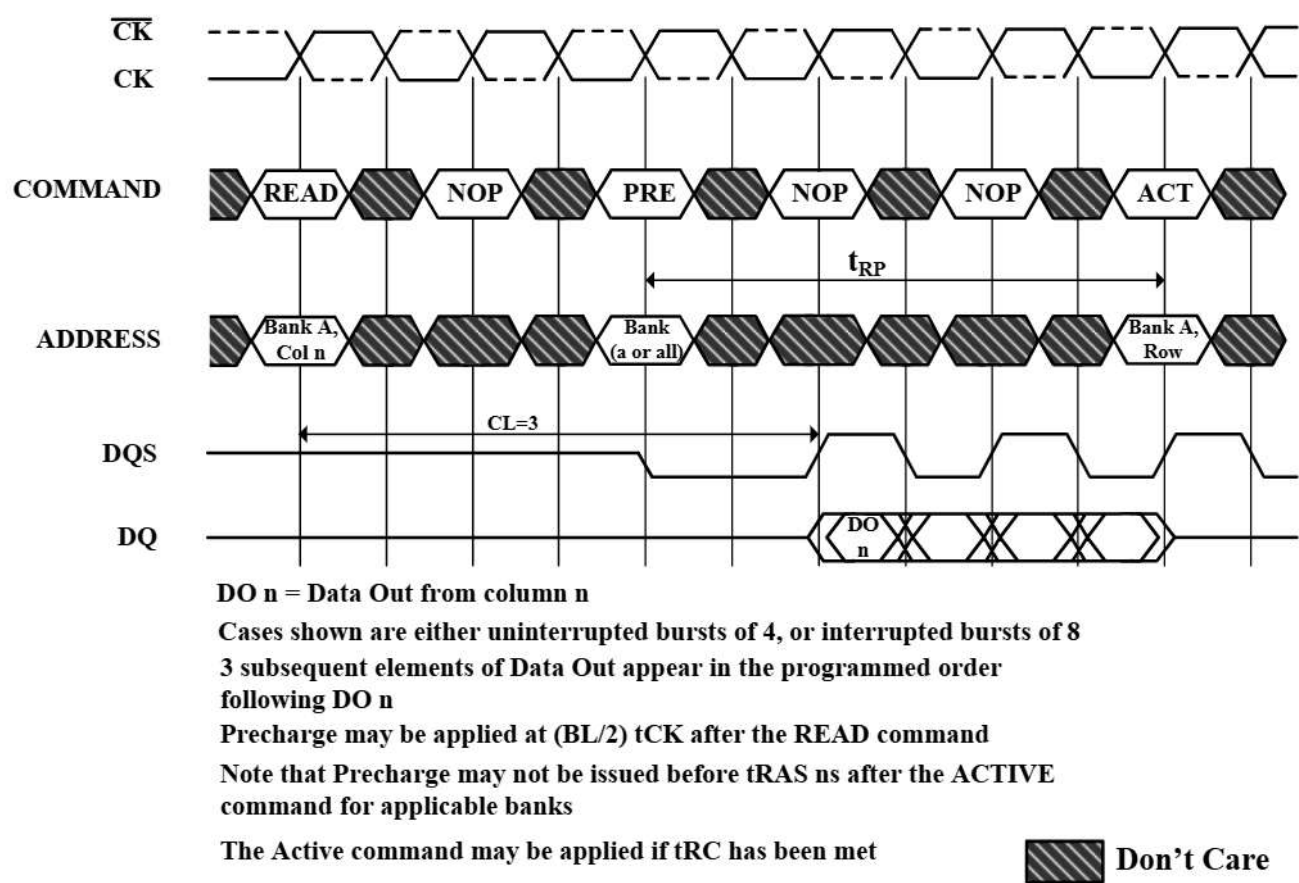


Figure 14. Write Command

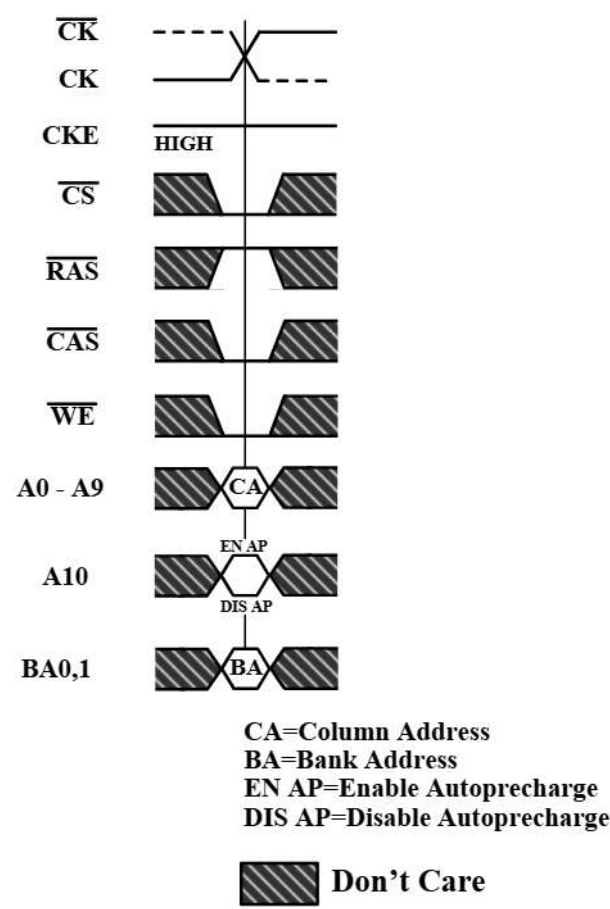


Figure 15. Write Max DQSS

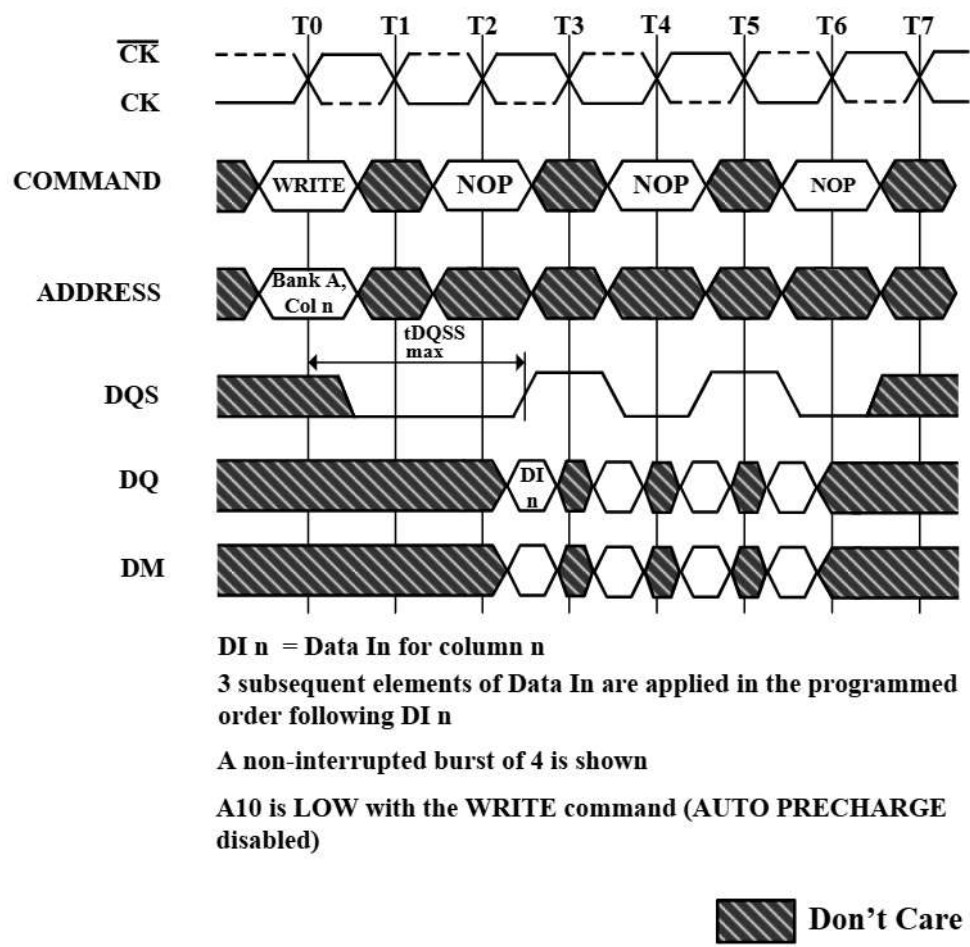


Figure 16. Write Min DQSS

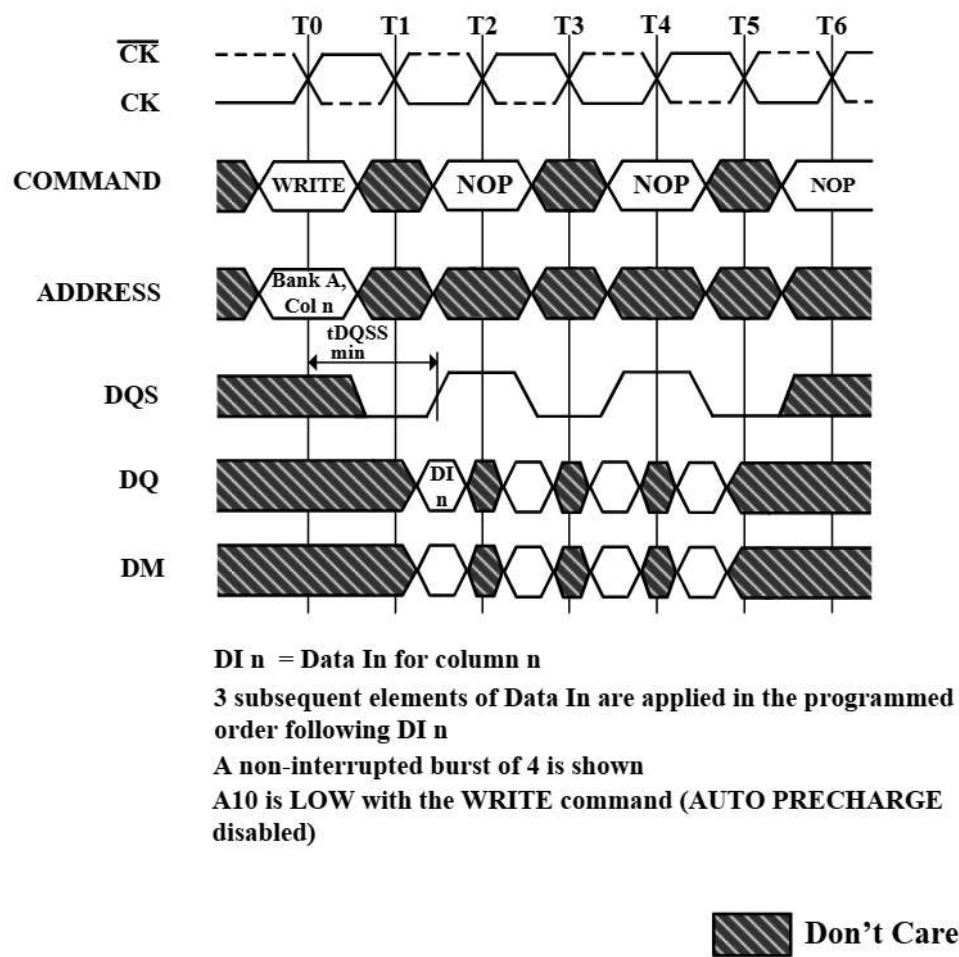


Figure 17. Write Burst Nom, Min, and Max tDQSS

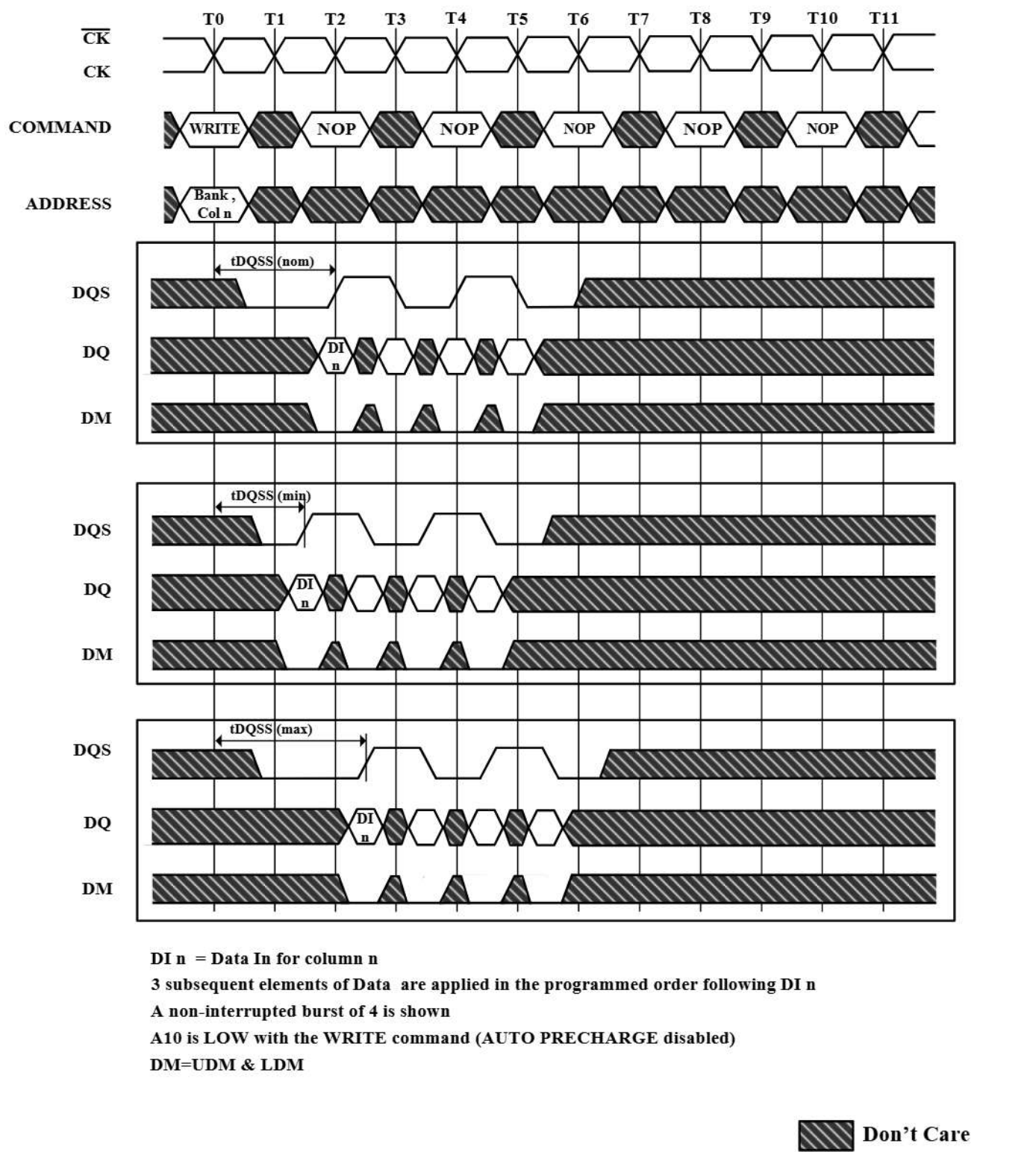


Figure 18. Write to Write Max tDQSS

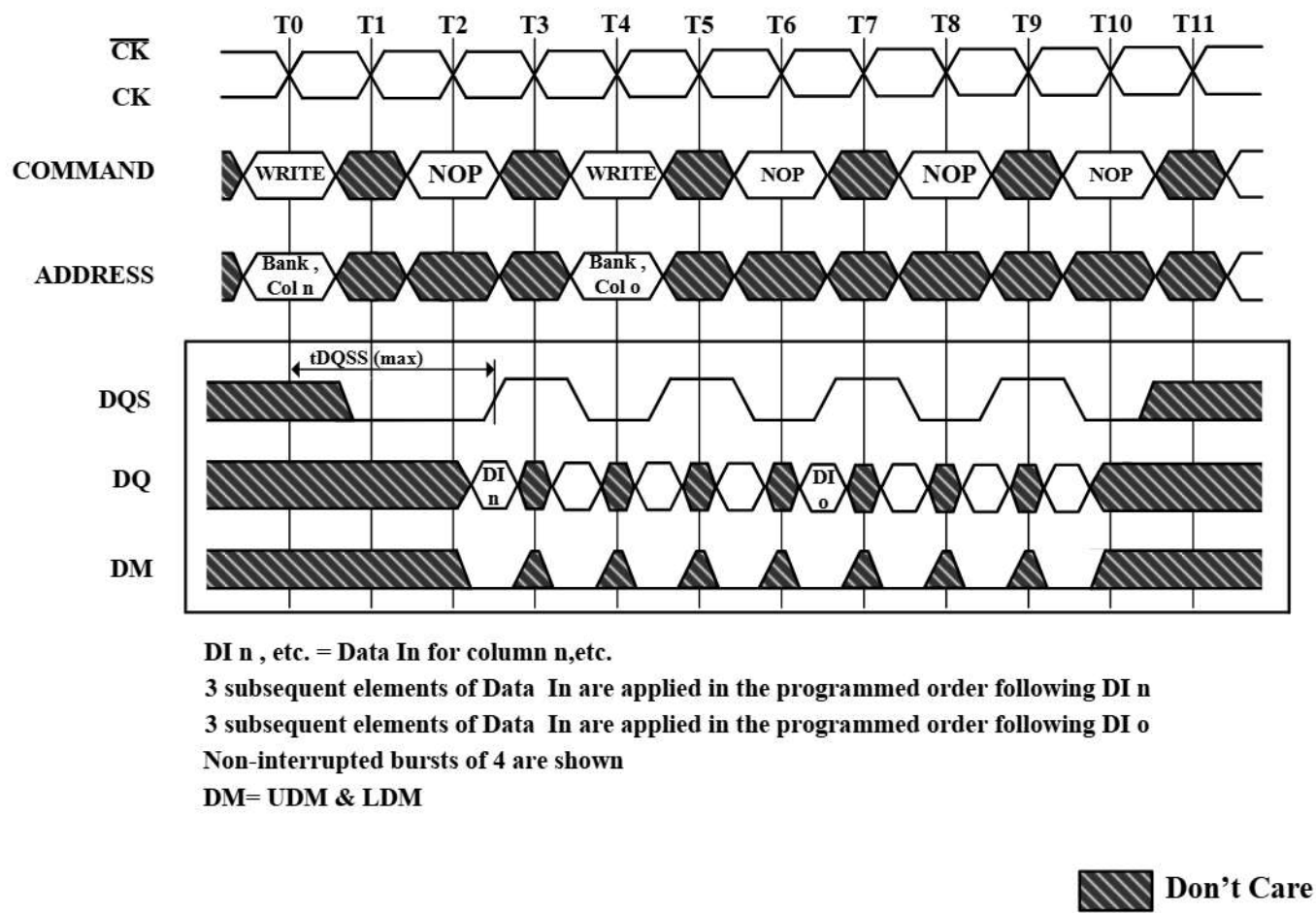
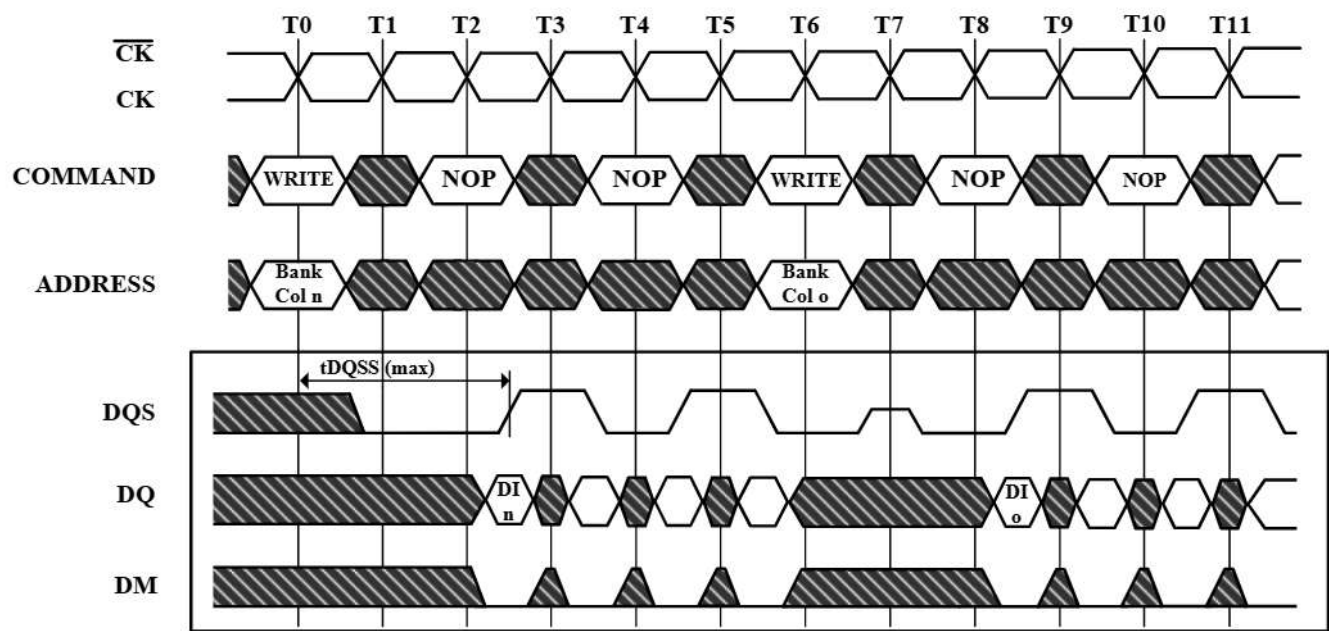


Figure 19. Write to Write Max tDQSS, Non Consecutive



DI n, etc. = Data In for column n, etc.
3 subsequent elements of Data In are applied in the programmed order following DI n
3 subsequent elements of Data In are applied in the programmed order following DI o
Non-interrupted bursts of 4 are shown
DM= UDM & LDM

 Don't Care

Figure 20. Random Write Cycles Max tDQSS

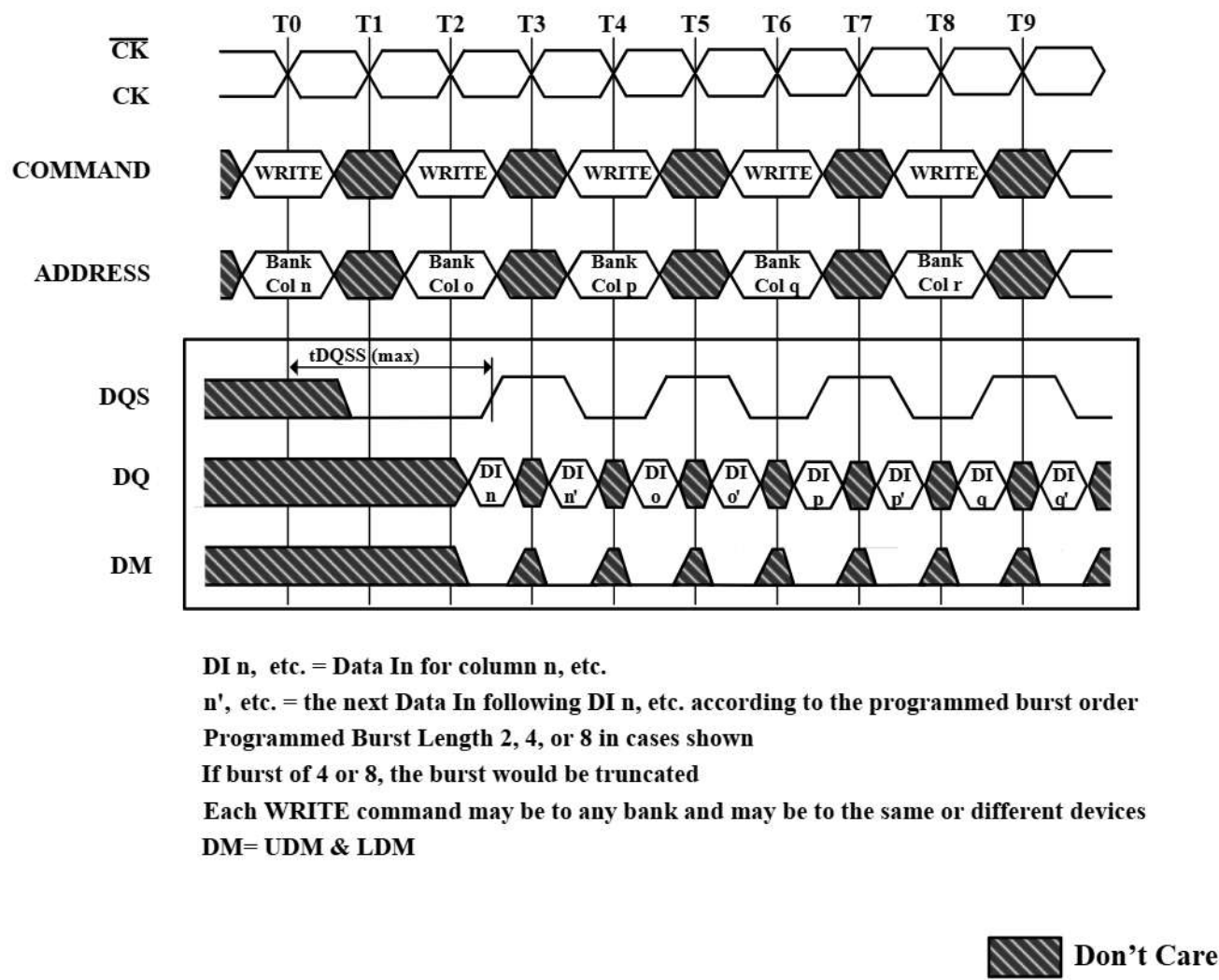


Figure 21. Write to Read Max tDQSS Non Interrupting

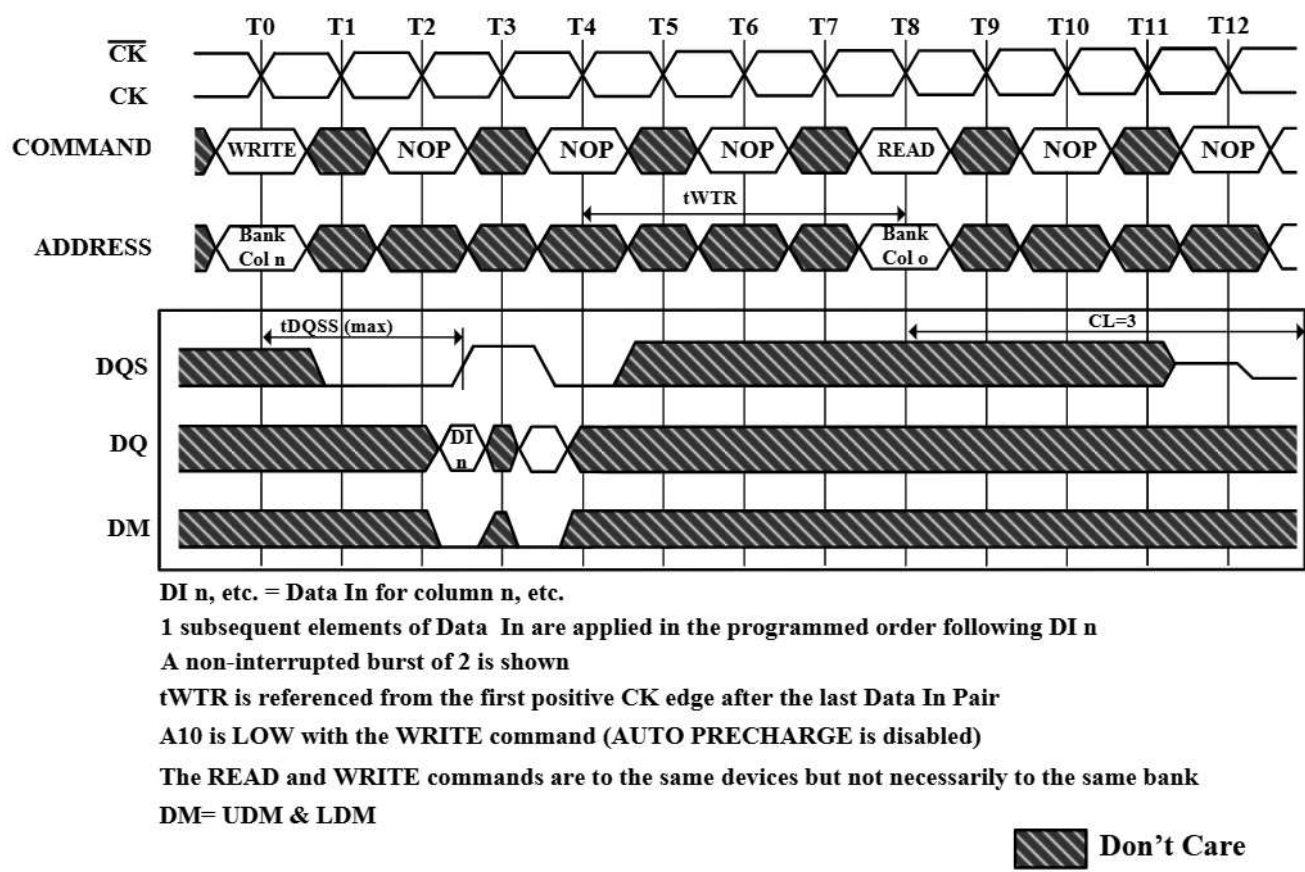
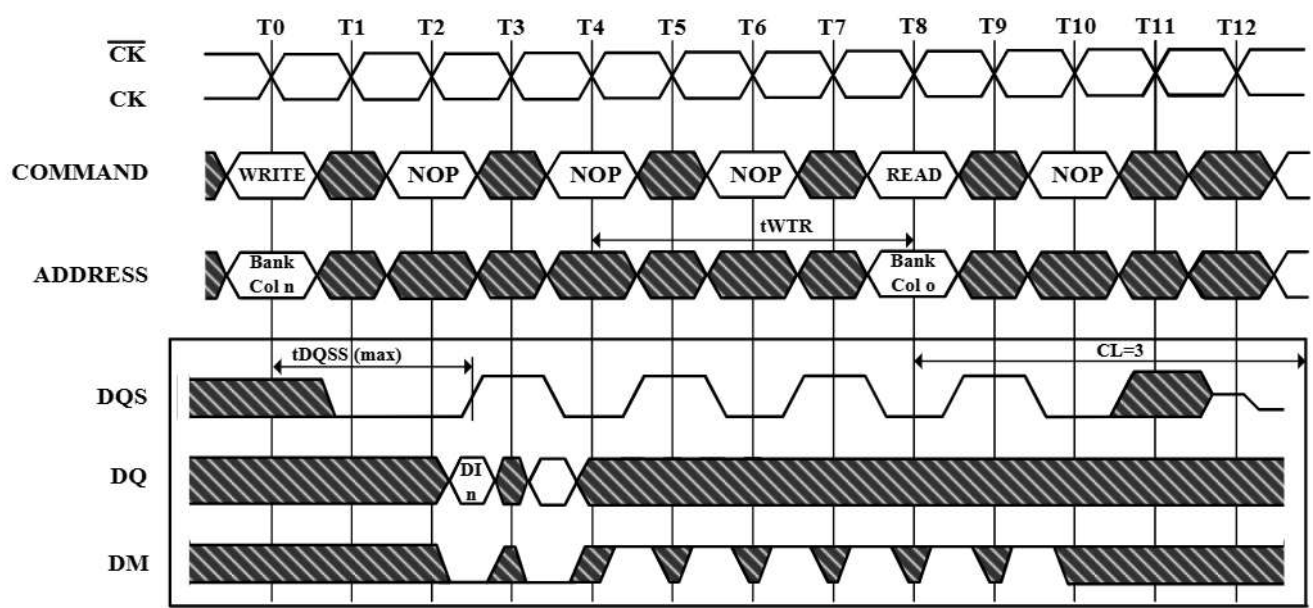


Figure 22. Write to Read Max tDQSS Interrupting



DI n, etc. = Data In for column n, etc.
1 subsequent elements of Data In are applied in the programmed order following DI n
An interrupted burst of 8 is shown, 2 data elements are written
tWTR is referenced from the first positive CK edge after the last Data In Pair
A10 is LOW with the WRITE command (AUTO PRECHARGE is disabled)
The READ and WRITE commands are to the same devices but not necessarily to the same bank
DM= UDM & LDM

Don't Care

Figure 23. Write to Read Max tDQSS, ODD Number of Data, Interrupting

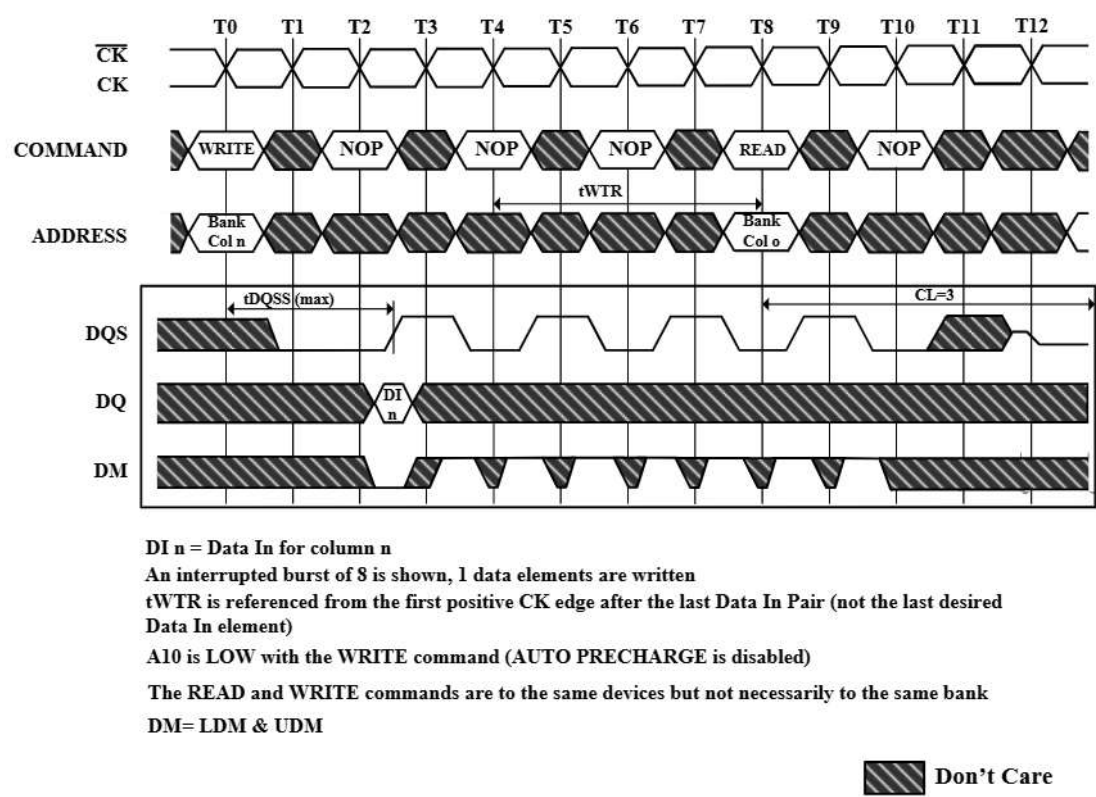
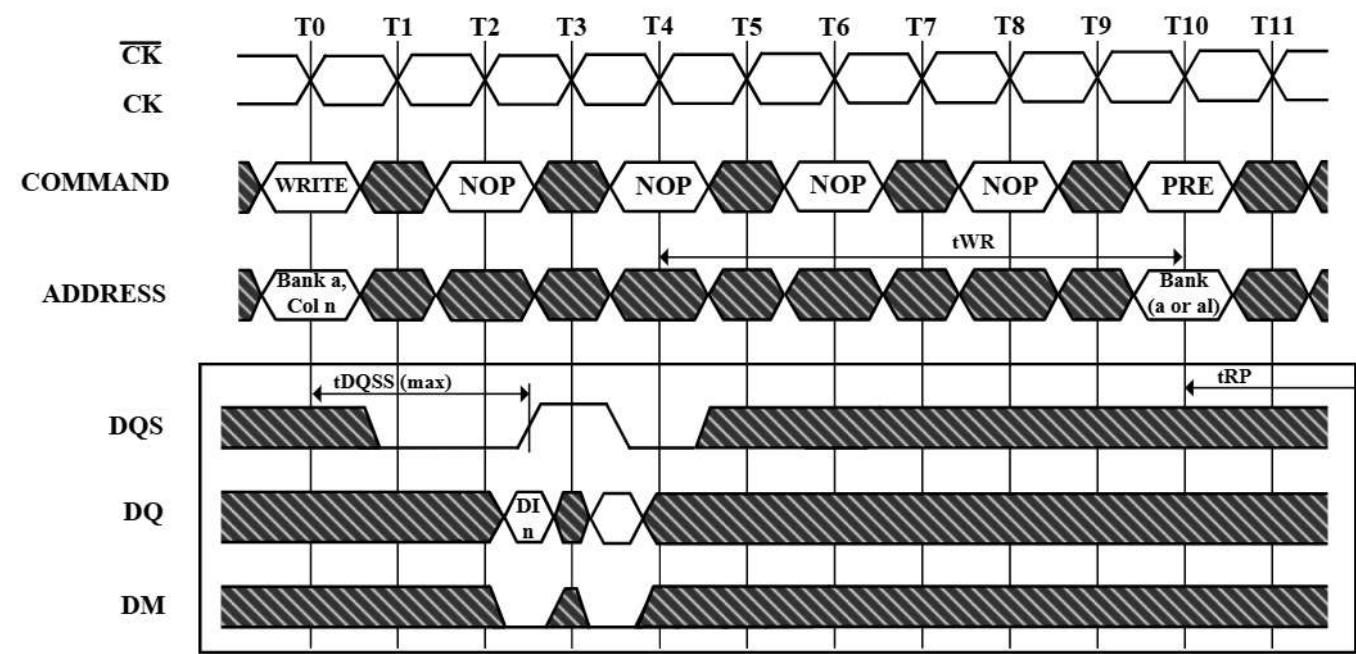


Figure 24. Write to Precharge Max tDQSS, NON- Interrupting



DI_n = Data In for column n
1 subsequent elements of Data In are applied in the programmed order following DI_n
A non-interrupted burst of 2 is shown
tWR is referenced from the first positive CK edge after the last Data In Pair
A10 is LOW with the WRITE command (AUTO PRECHARGE is disabled)
DM= UDM & LDM

 Don't Care

Figure 25. Write to Precharge Max tDQSS, Interrupting

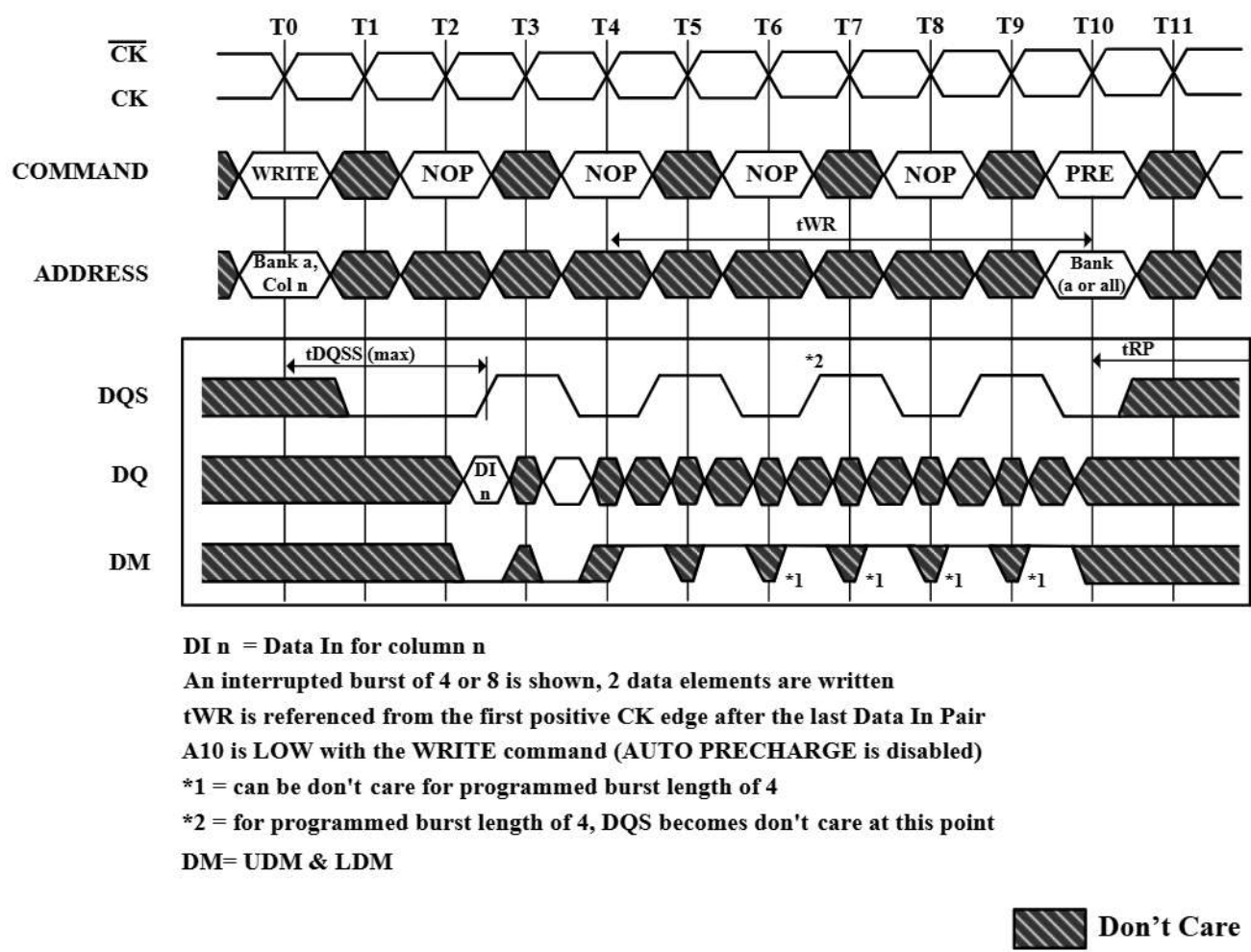
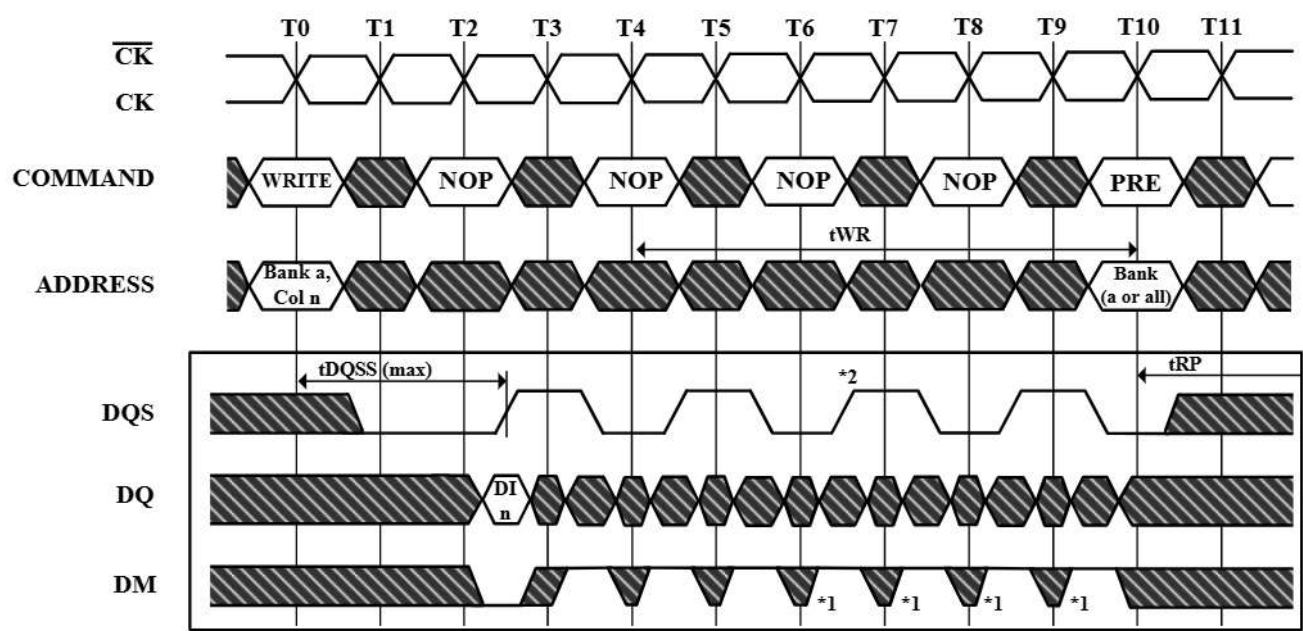


Figure 26. Write to Precharge Max tDQSS ODD Number of Data Interrupting



DI n = Data In for column n
An interrupted burst of 4 or 8 is shown, 1 data element is written
tWR is referenced from the first positive CK edge after the last Data In Pair
A10 is LOW with the WRITE command (AUTO PRECHARGE is disabled)
*1 = can be don't care for programmed burst length of 4
*2 = for programmed burst length of 4, DQS becomes don't care at this point
DM= UDM & LDM

 Don't Care

Figure 27. Precharge Command

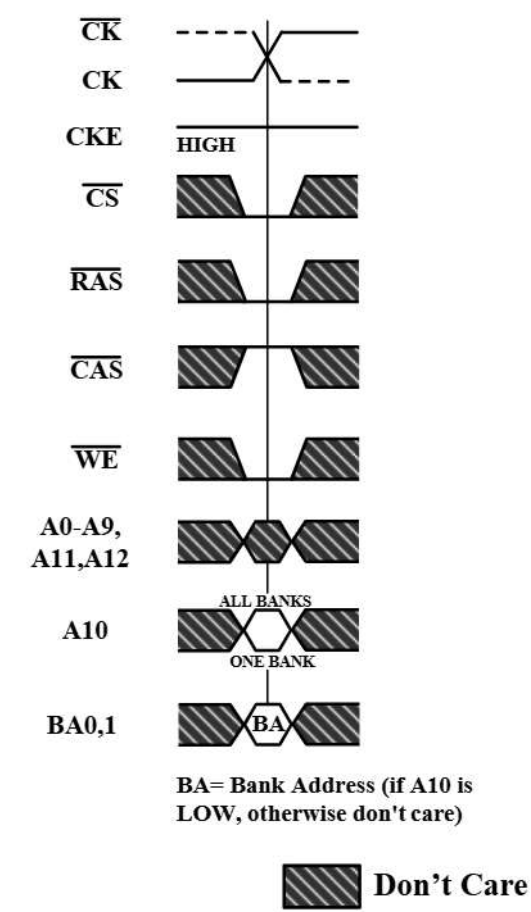


Figure 28. Power-Down

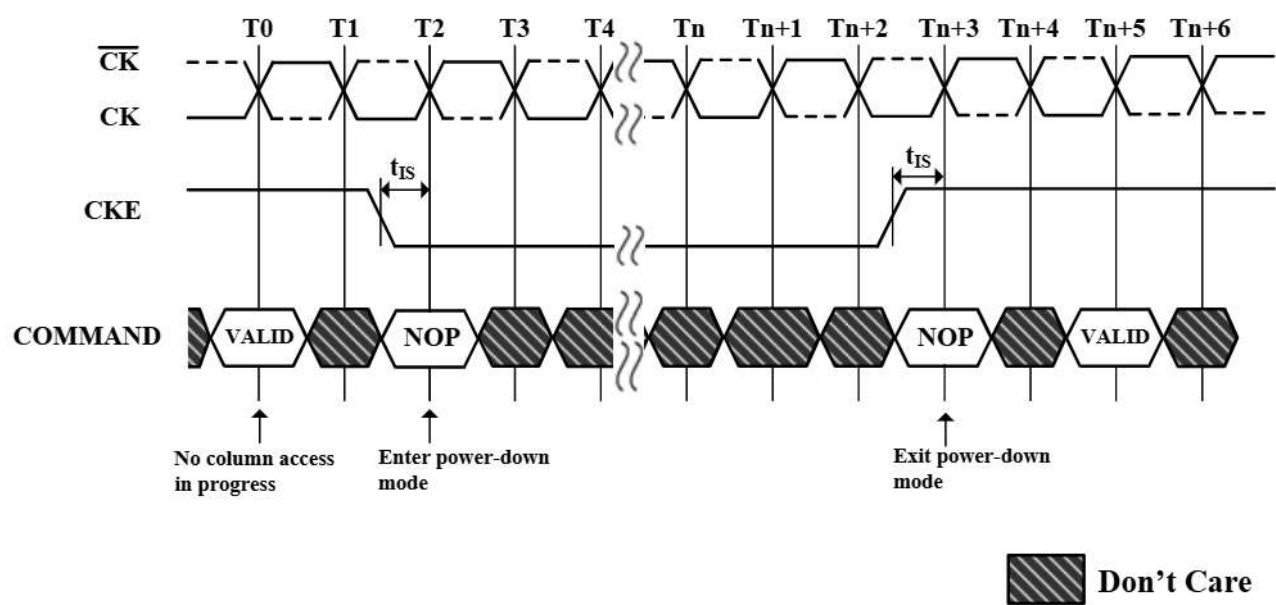


Figure 29. Clock Frequency Change in Precharge

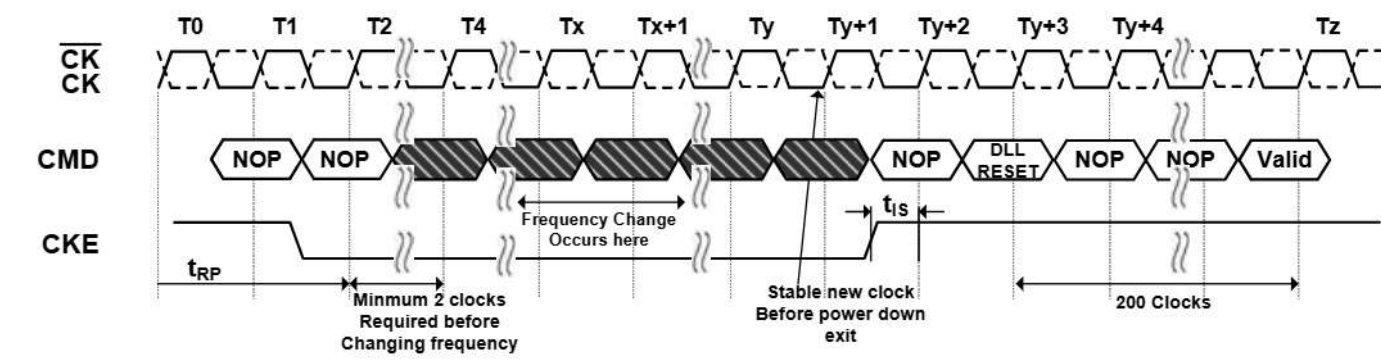


Figure 30. Data input (Write) Timing

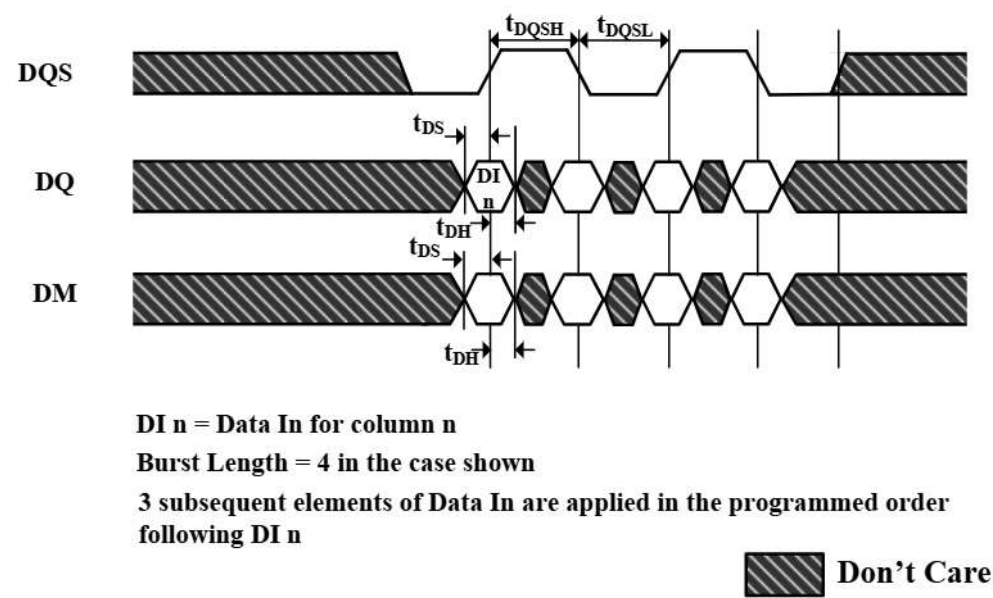


Figure 31. Data Output (Read) Timing

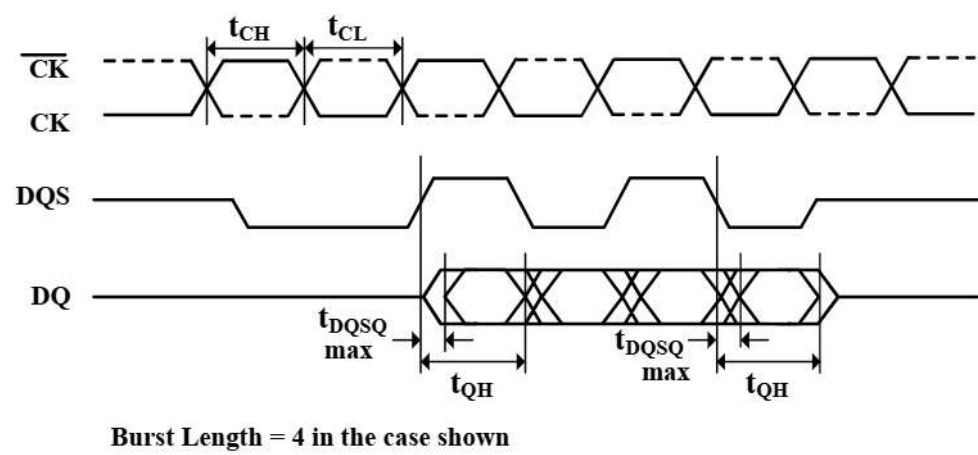
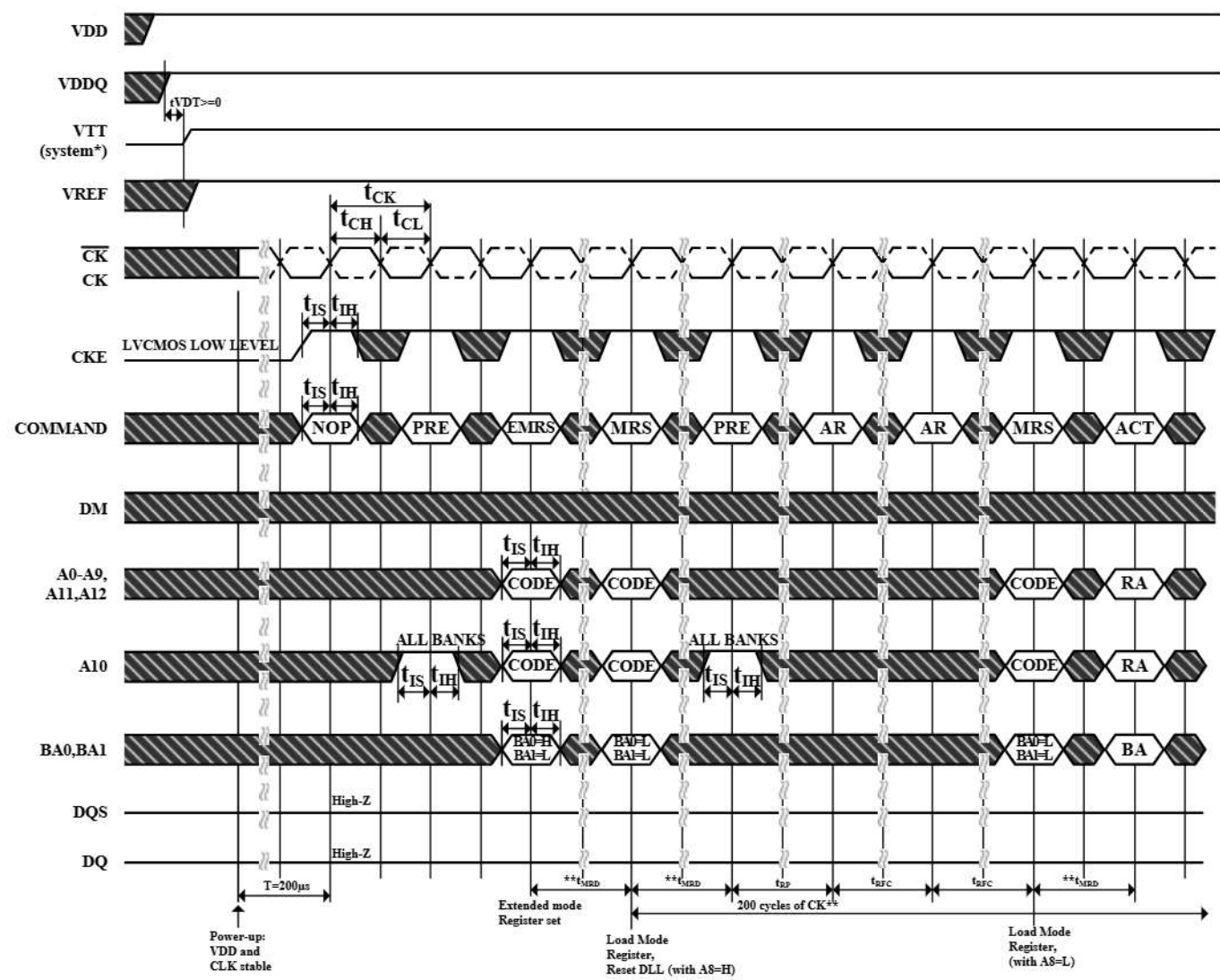


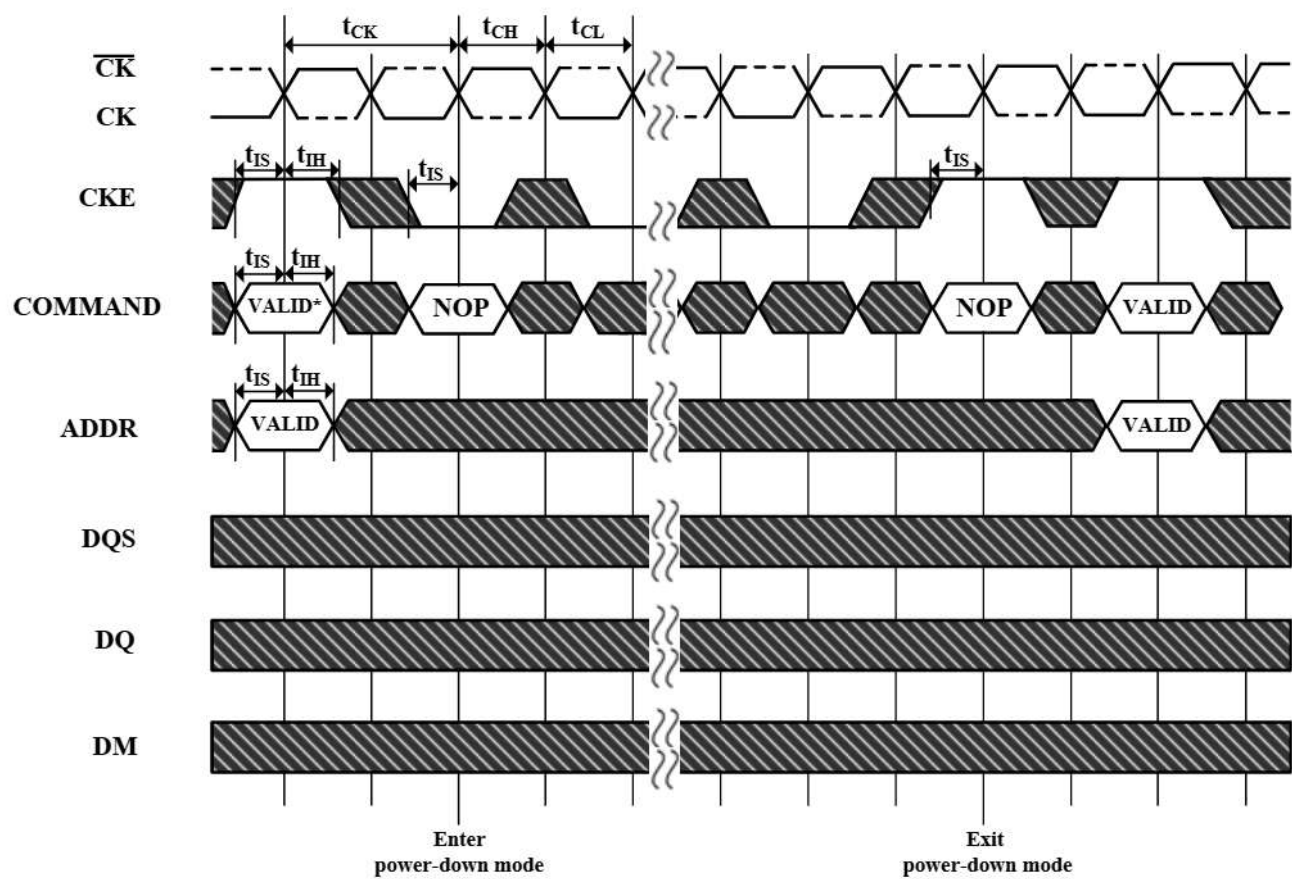
Figure 32. Initialize and Mode Register Sets



*=VTT is not applied directly to the device, however tVTD must be greater than or equal to zero to avoid device latch-up.
** = tMRD is required before any command can be applied, and 200 cycles of CK are required before any executable command can be applied the two auto Refresh commands may be moved to follow the first MRS but precede the second PRECHARGE ALL command.

 Don't Care

Figure 33. Power Down Mode



No column accesses are allowed to be in progress at the time Power-Down is entered
*=If this command is a PRECHARGE ALL (or if the device is already in the idle state) then the Power-Down mode shown is Precharge Power Down. If this command is an ACTIVE (or if at least one row is already active) then the Power-Down mode shown is active Power Down.

 Don't Care

Figure 34. Auto Refresh Mode

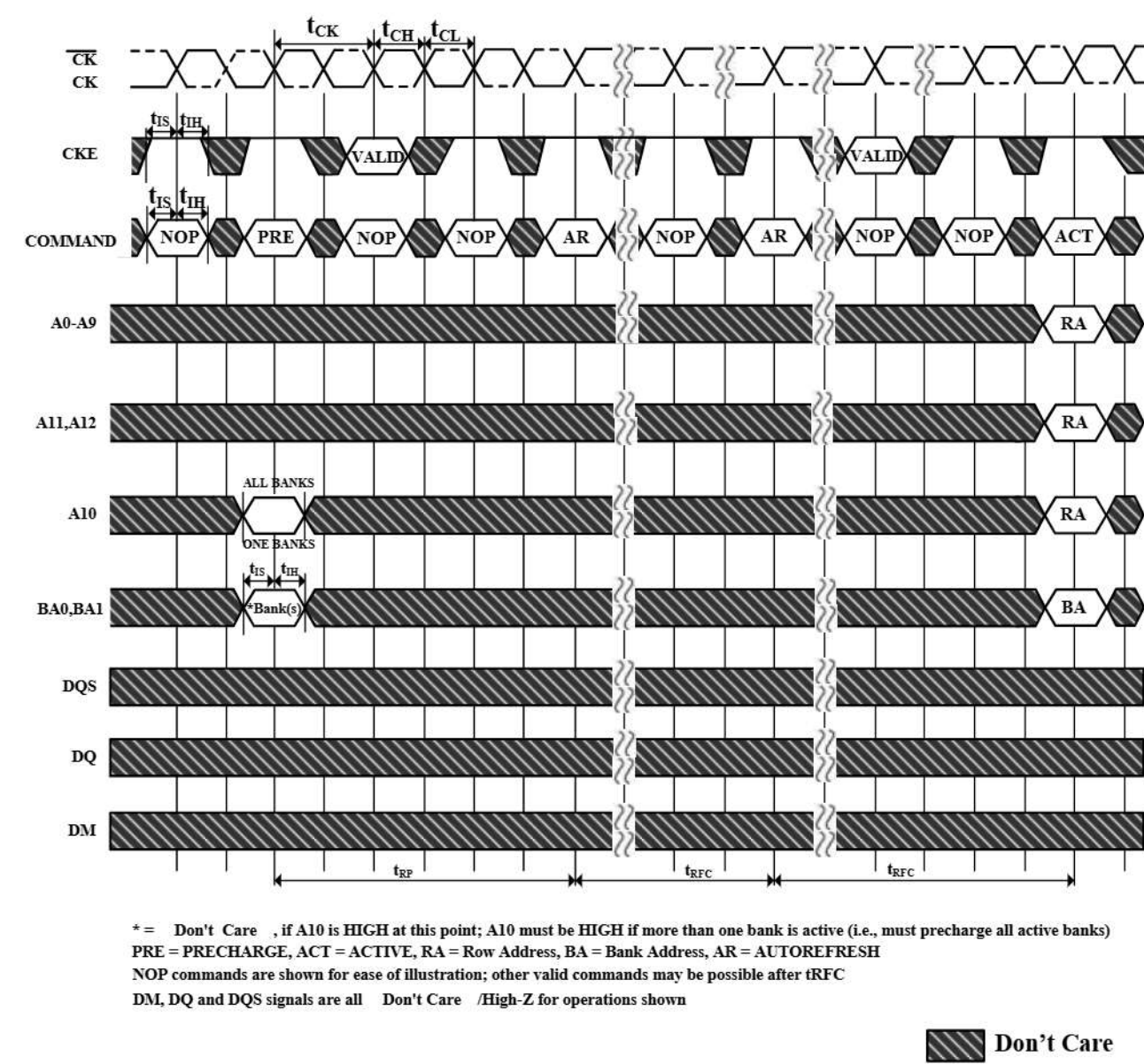


Figure 35. Self Refresh Mode

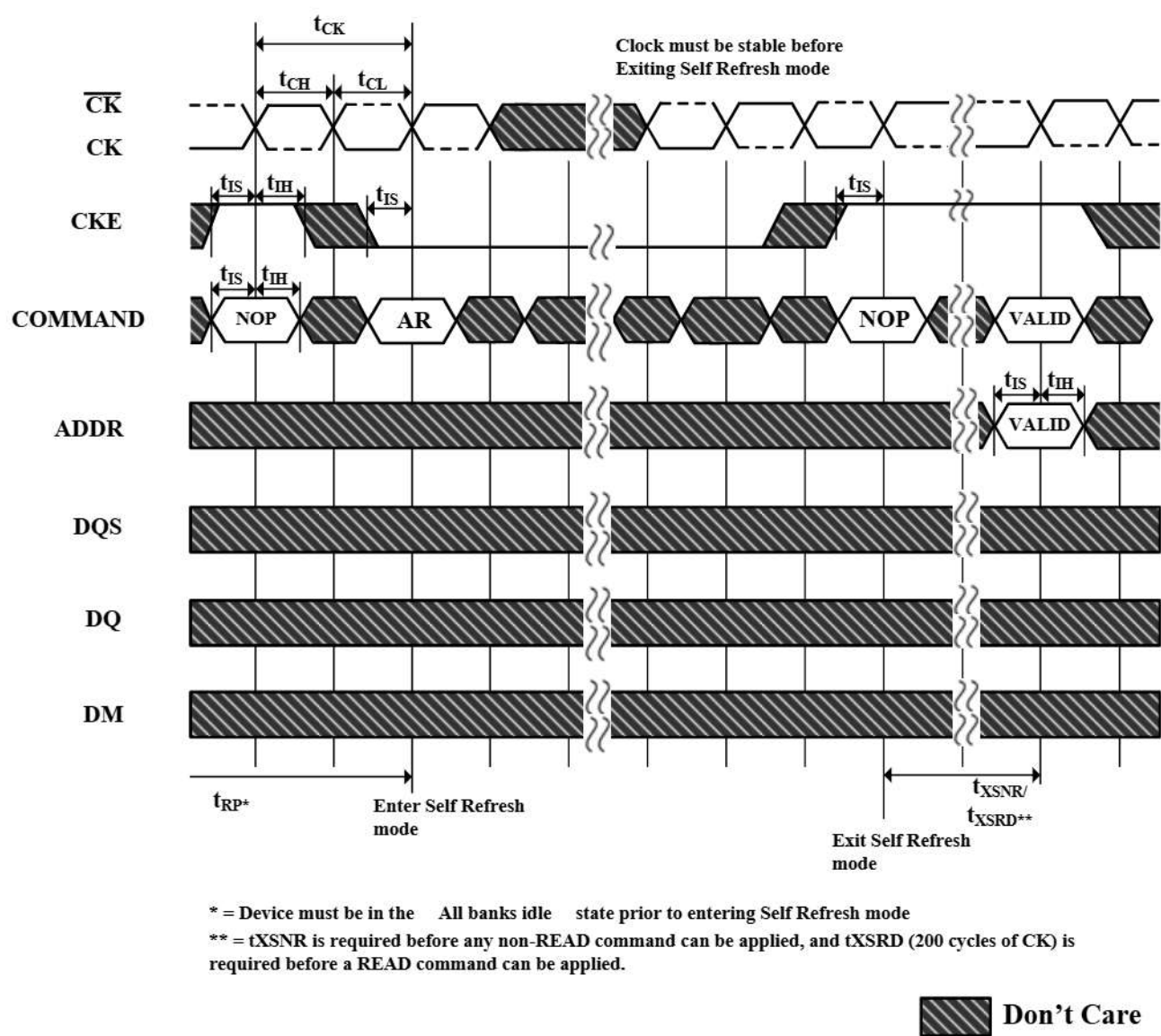


Figure 36. Read without Auto Precharge

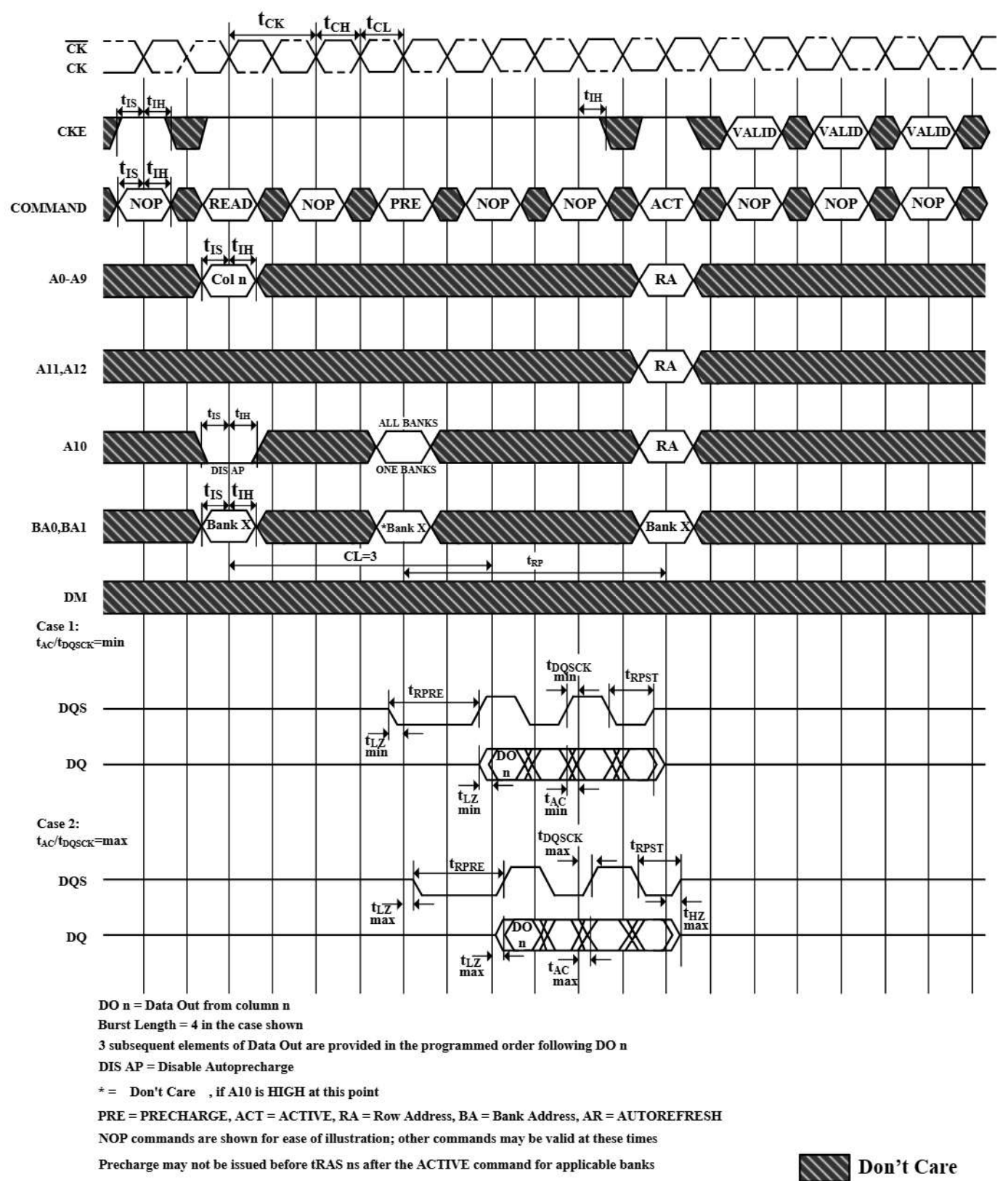
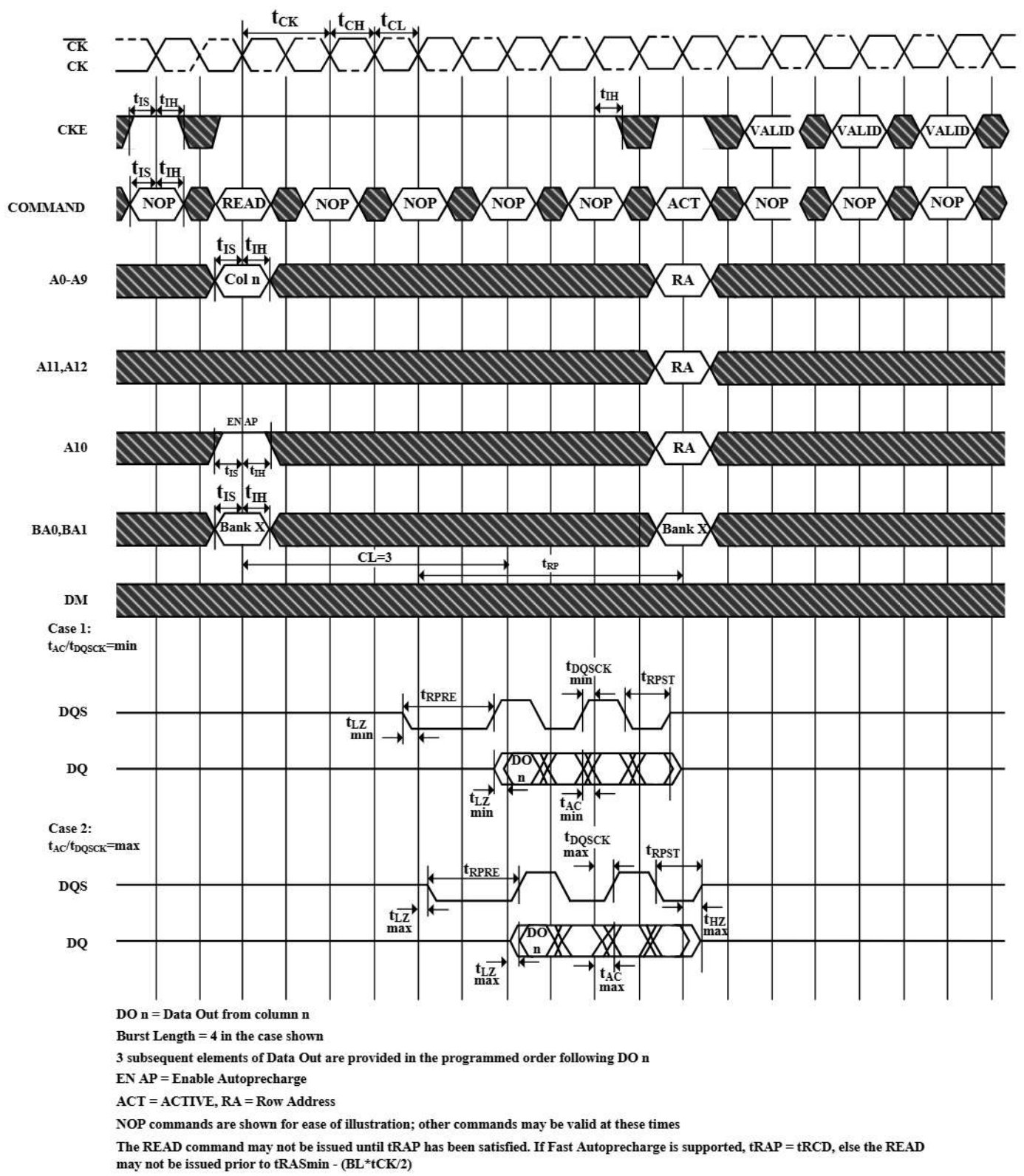


Figure 37. Read with Auto Precharge



Don't Care

Figure 38. Bank Read Access

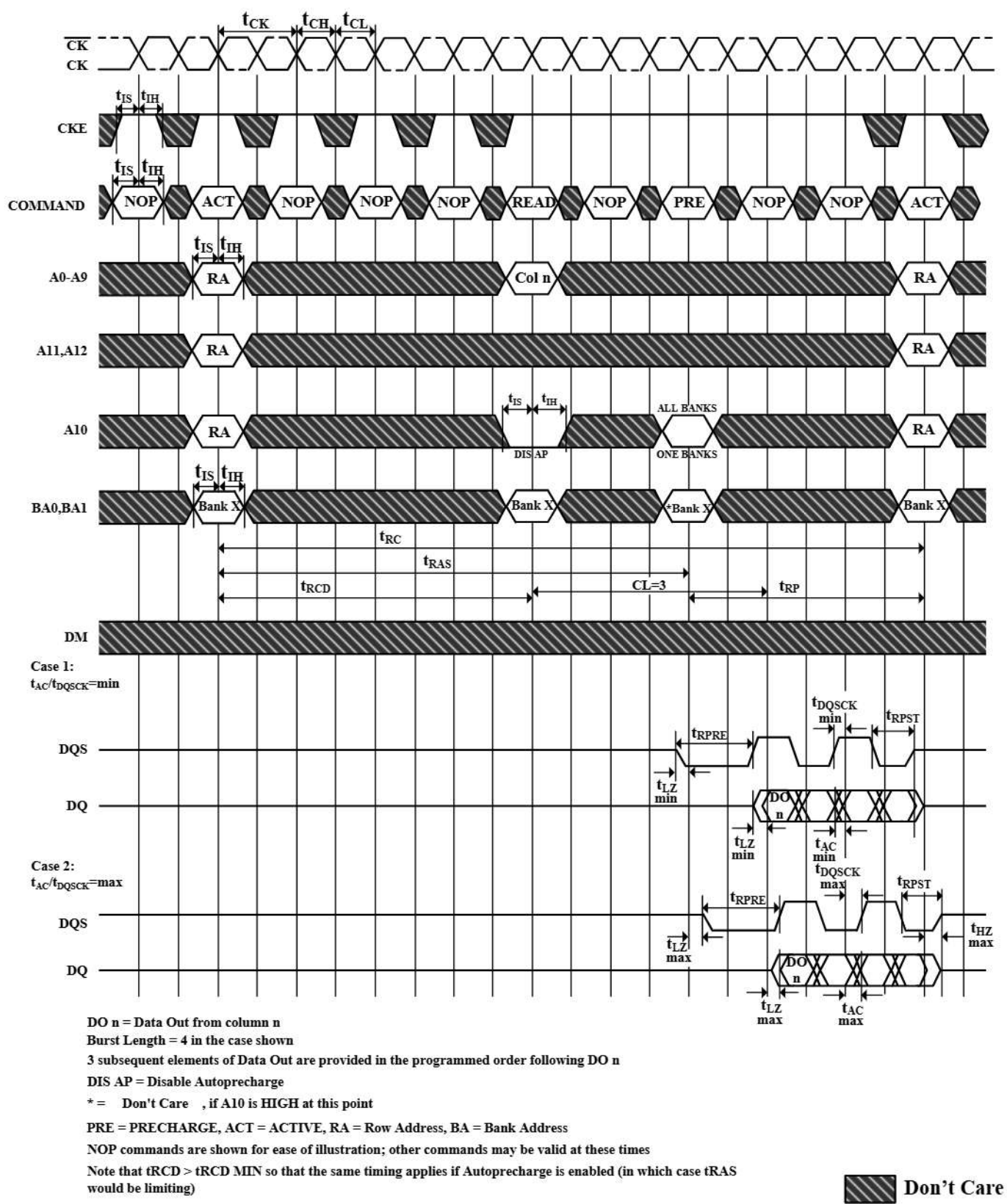


Figure 39. Write without Auto Precharge

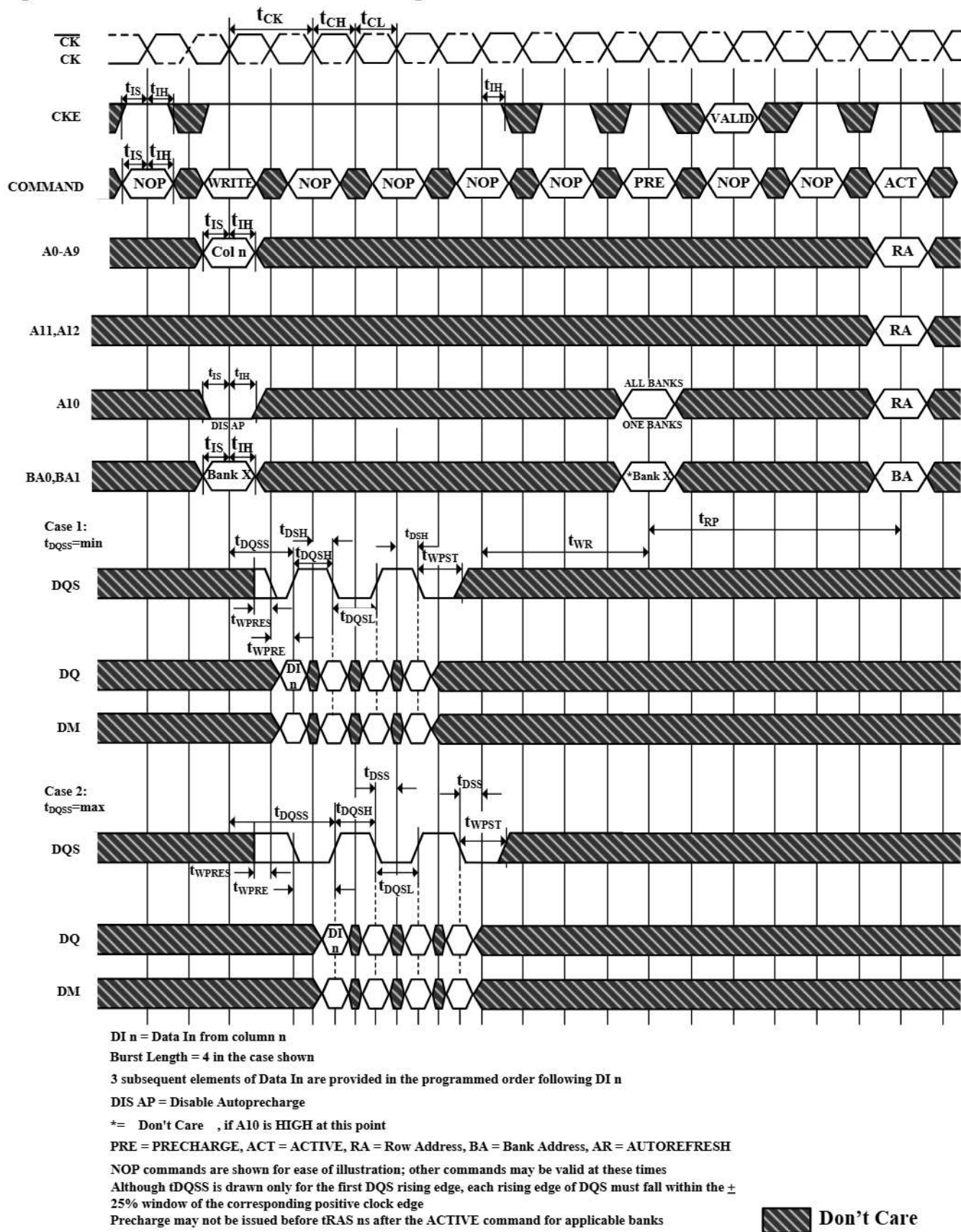


Figure 40. Write with Auto Precharge

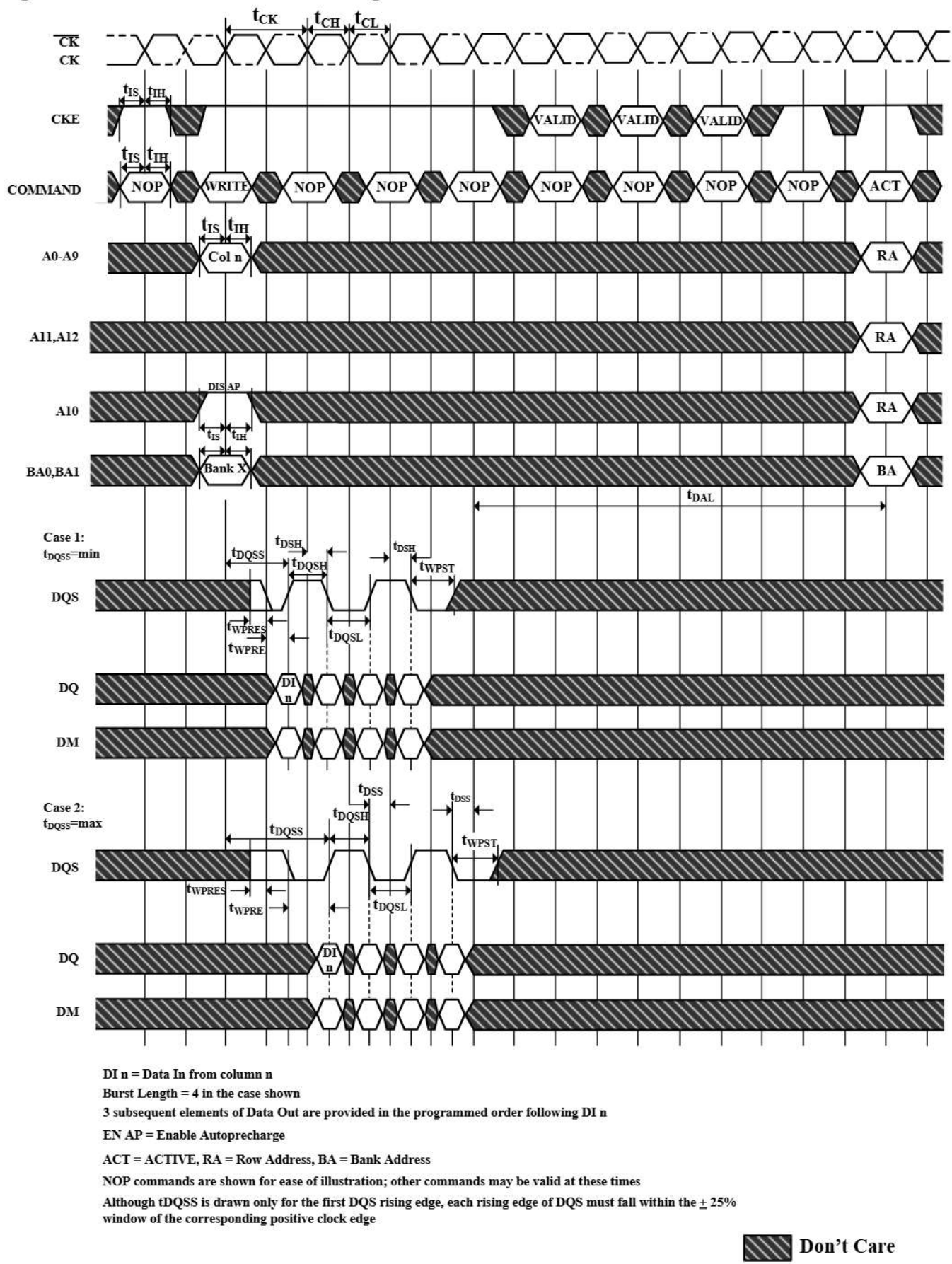


Figure 41. Bank Write Access

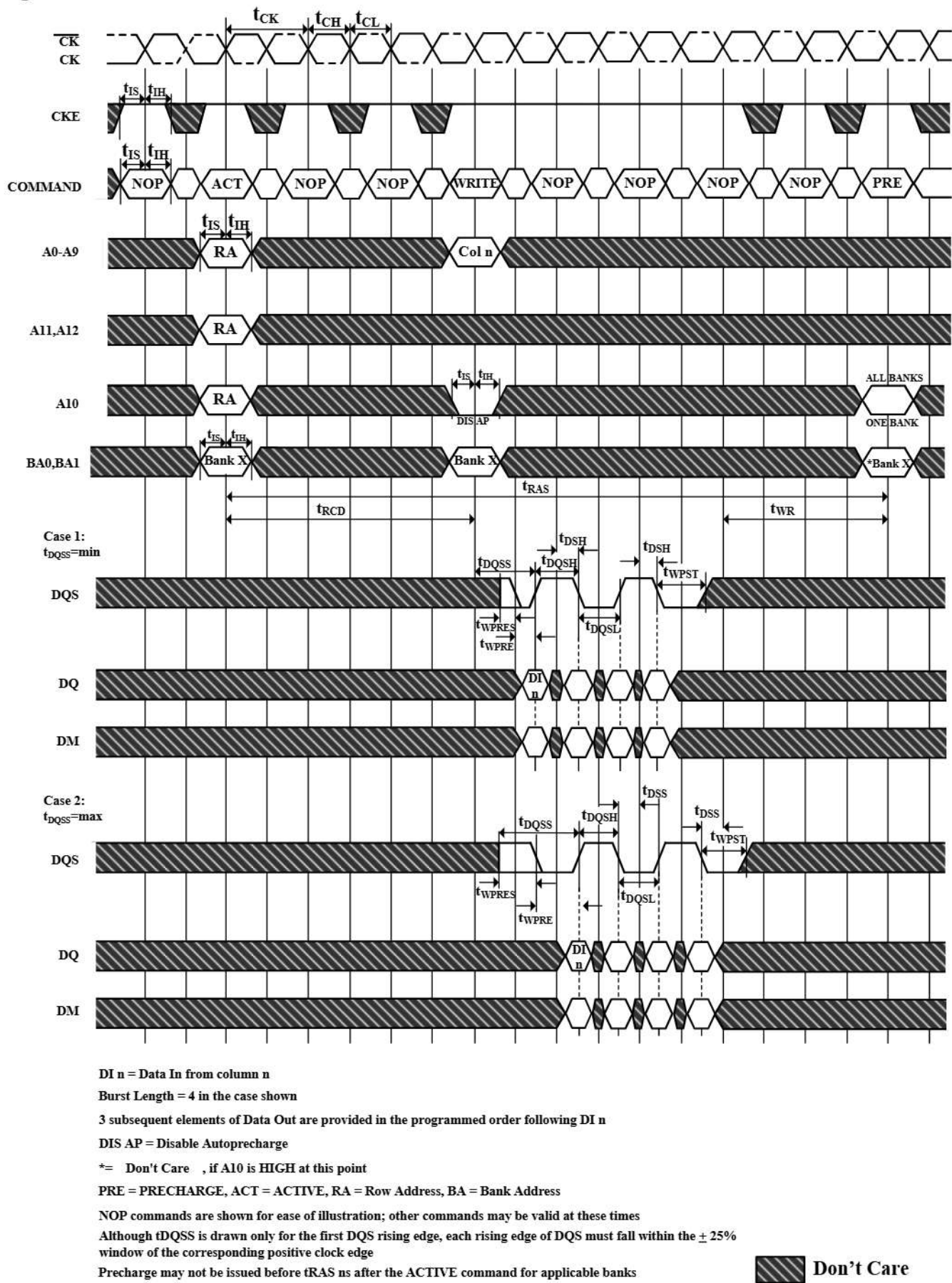


Figure 42. Write DM Operation

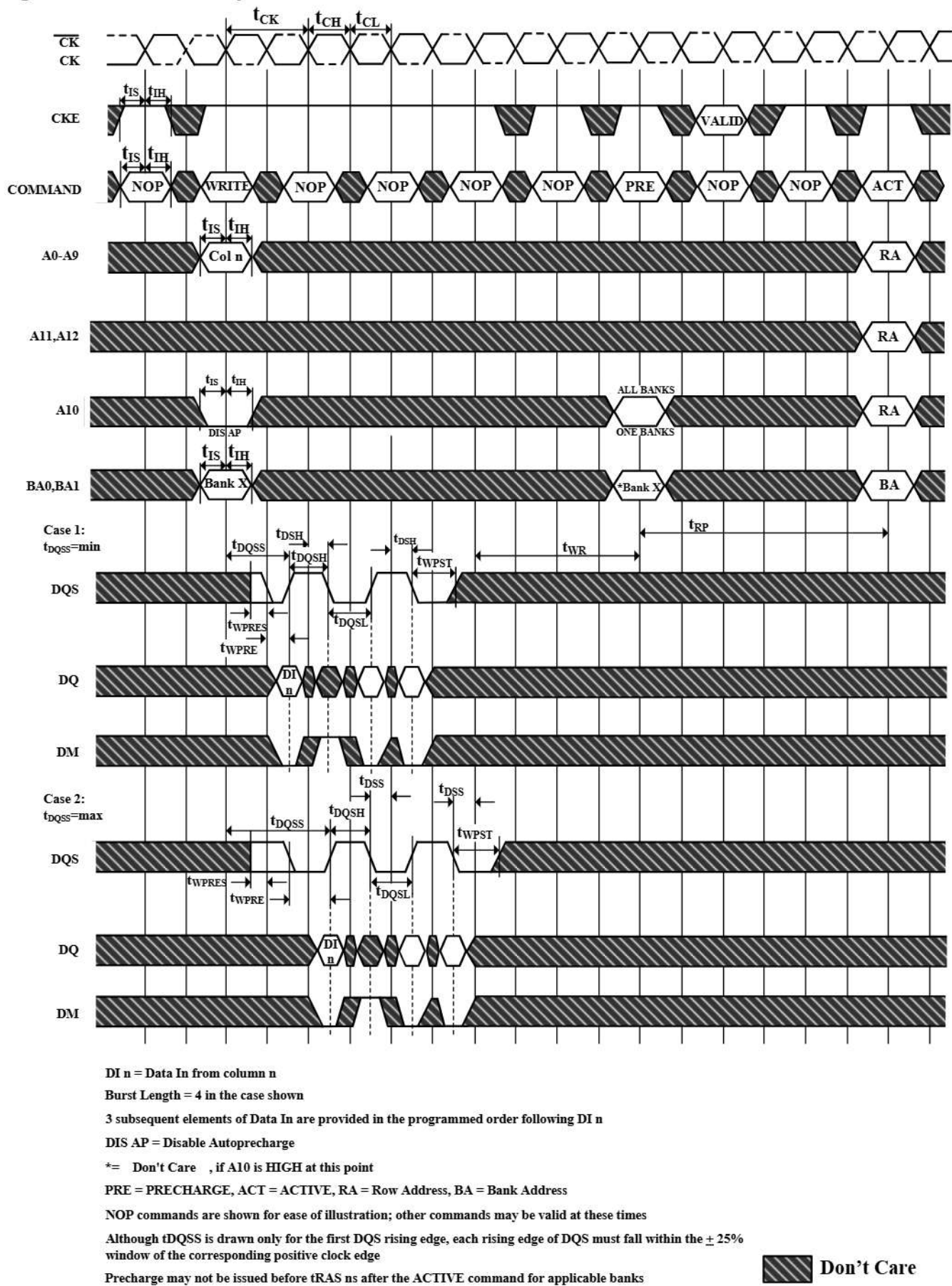
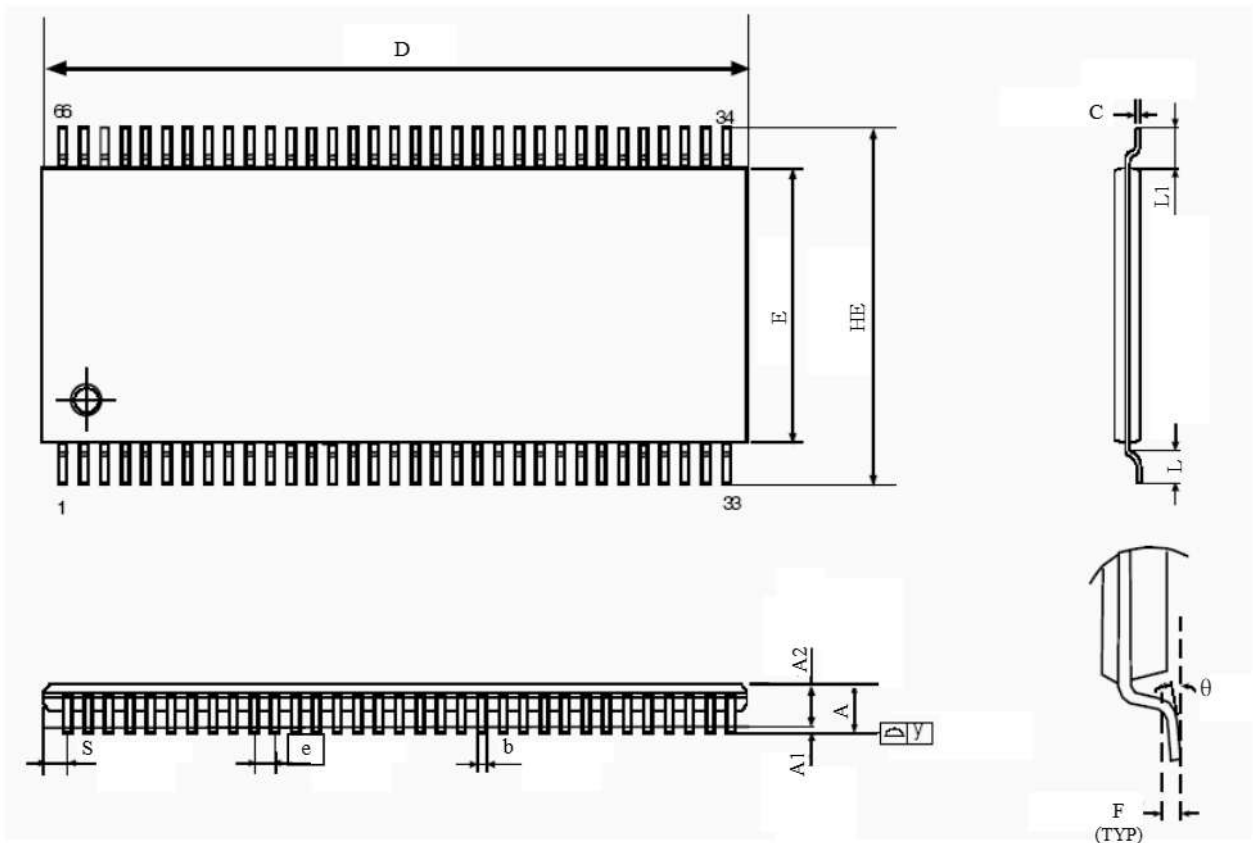
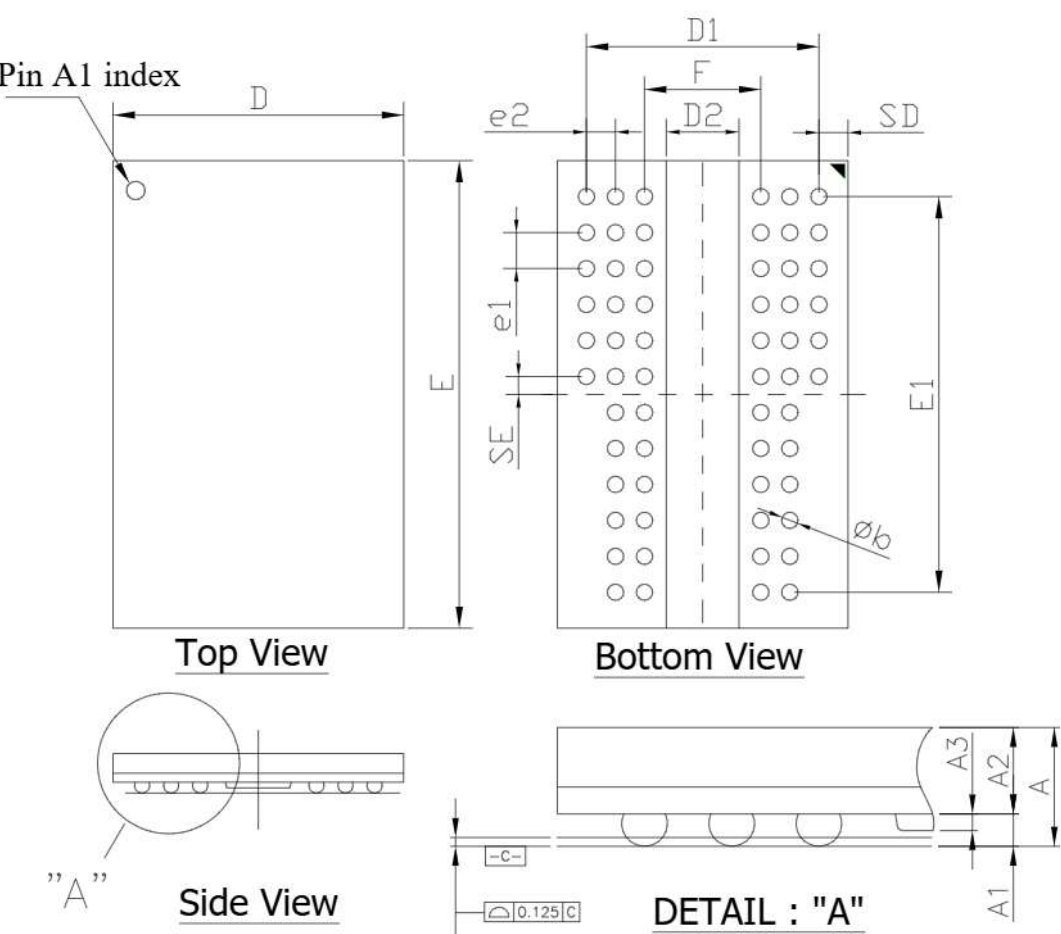


Figure 43. 66 Pin TSOP II Package Outline Drawing Information
Units: mm



Symbol	Dimension in mm			Dimension in inch		
	Min	Nom	Max	Min	Nom	Max
A	---	---	1.2	---	---	0.047
A1	0.05	---	0.2	0.002	---	0.008
A2	0.9	1.0	1.1	0.035	0.039	0.043
b	0.22	---	0.45	0.009	---	0.018
e	---	0.65	---	---	0.026	---
C	0.095	0.125	0.21	0.004	0.005	0.008
D	22.09	22.22	22.35	0.87	0.875	0.88
E	10.03	10.16	10.29	0.395	0.4	0.405
HE	11.56	11.76	11.96	0.455	0.463	0.471
L	0.40	0.5	0.6	0.016	0.02	0.024
L1	---	0.8	---	---	0.032	---
F	---	0.25	---	---	0.01	---
θ	0°	---	8°	0°	---	8°
S	---	0.71	---	---	0.028	---
Δy	---	---	0.10	---	---	0.004

Figure 44. FBGA 60ball package Outline Drawing Information



Symbol	Dimension (inch)			Dimension (mm)		
	Min	Nom	Max	Min	Nom	Max
A	--	--	0.047	--	--	1.20
A1	0.012	0.014	0.016	0.30	0.35	0.40
A2	--	--	0.031	--	--	0.8
A3	0.005	0.007	0.009	0.13	0.18	0.23
D	0.311	0.315	0.319	7.90	8.00	8.10
E	0.508	0.512	0.516	12.90	13.00	13.10
D1	--	0.252	--	--	6.40	--
E1	--	0.433	--	--	11.00	--
e1	--	0.039	--	--	1.00	--
e2	--	0.031	--	--	0.80	--
b	0.016	0.018	0.020	0.40	0.45	0.50
F	--	0.126	--	--	3.20	--
SD	--	0.031	--	--	0.80	--
SE	--	0.02	--	--	0.50	--
D2	--	--	0.081	--	--	2.05