

650V Enhancement-mode GaN Power Transistor

Features

- 650V GaN enhancement-mode power switch
- $R_{DS(on), max}$ 60m Ω
- Recommended gate drive voltage 6V
- Ultra-low FOM
- Ultra-high switching frequency
- Reverse current capability
- Zero reverse recovery loss
- Monolithic integrated ESD protection, HBM class 2, CDM class C3
- RoHS, Pb-free

Applications

- AC-DC converters, DC-DC converters
- Bridgeless totem pole PFC, data center, telecom, network SMPS
- Uninterruptable power supplies (UPS)
- Solar inverters, energy storage systems
- Wireless power transfer
- Power adapters, LED lighting drivers
- Laser drivers
- Industrial motor drives

Table 1 Key Performance Parameters at $T_j = 25^\circ\text{C}$

Parameters	Values	Units
$V_{DS, max}$	650	V
$R_{DS(on), max}$	60	m Ω
Q_G, typ	6	nC
$I_D, Pulse$	60	A
$Q_{OSS} @ 400\text{ V}$	94.7	nC
Q_{rr}	0	nC

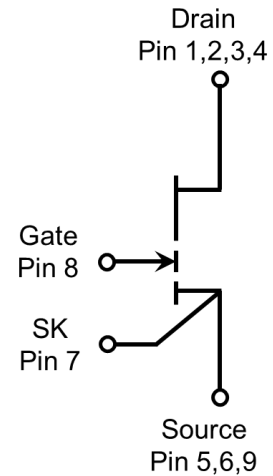


Table 2 Ordering Information

Ordering Code	Package	Marking	Packing
CID60N65D	DFN 8x8	CID60N65D	Reel

Maximum ratings

at $T_j = 25\text{ °C}$ unless otherwise specified. Continuous application of maximum ratings can deteriorate transistor lifetime.

Table 3 Maximum ratings

Parameters	Sym.	Values			Units	Notes/Test Conditions
		Min.	Typ.	Max.		
Drain-source voltage	$V_{DS, max}$	-	-	650	V	$V_{GS} = 0\text{ V}$; $I_D = 10\text{ }\mu\text{A}$
Drain-source voltage transient ¹	$V_{DS, transient}$	-	-	800	V	$V_{GS} = 0\text{ V}$
Continuous current, drain-source	I_D	-	-	26	A	$T_c = 25\text{ °C}$
Pulsed current, drain-source ²	$I_{D, pulse}$	-	-	60	A	$T_c = 25\text{ °C}$; $V_G = 6\text{ V}$
Pulsed current, drain-source ²	$I_{D, pulse}$	-	-	31	A	$T_c = 125\text{ °C}$; $V_G = 6\text{ V}$
Gate-source voltage, continuous ³	V_{GS}	-6	-	+7	V	$T_j = -55\text{ °C}$ to 150 °C
Gate-source voltage, pulsed	$V_{GS, pulse}$	-20	-	+10	V	$T_j = -55\text{ °C}$ to 150 °C ; $t_{Pulse} = 50\text{ ns}$; $f = 100\text{ kHz}$; open drain
Power dissipation	P_{tot}	-	-	250	W	$T_c = 25\text{ °C}$
Operating temperature	T_j	-55	-	+150	°C	
Storage temperature	T_{stg}	-55	-	+150	°C	

1. $V_{DS, transient}$ is intended for surge rating during non-repetitive events, $t_{Pulse} < 1\text{ }\mu\text{s}$.

2. Pulse width = $10\text{ }\mu\text{s}$.

3. The minimum V_{GS} is clamped by monolithic integrated ESD protection circuit.

Thermal characteristics

Table 4 Thermal characteristics

Parameters	Sym.	Values	Units	Notes/Test Conditions
Thermal resistance, junction-case	R_{thJC}	0.49	°C/W	
Thermal resistance, junction-ambient ¹	R_{thJA}	63.99	°C/W	
Reflow soldering temperature	T_{sold}	260	°C	MSL3

1. Device mounted on 1.6 mm PCB thickness FR4, 4-layer PCB with 2 oz copper on each layer. The recommendation for thermal vias under the thermal pad is 0.3 mm diameter (12mil) with 0.889 mm pitch (35mil). The copper layers under the thermal pad and drain pad are 25 x 25 mm² each. The PCB is mounted in horizontal position without air stream cooling.

Electrical characteristics

at $T_j = 25\text{ °C}$, unless otherwise specified.

Table 5 Static characteristics

Parameters	Sym.	Values			Units	Notes/Test Conditions
		Min.	Typ.	Max.		
Gate threshold voltage	$V_{GS(TH)}$	1.2	1.3	2.5	V	$I_D = 7.5\text{ mA}$; $V_{DS} = V_{GS}$; $T_j = 25\text{ °C}$
		-	1.2	-		$I_D = 7.5\text{ mA}$; $V_{DS} = V_{GS}$; $T_j = 125\text{ °C}$
Drain-source leakage current	I_{DSS}	-	6.5	18	μA	$V_{DS} = 650\text{ V}$; $V_{GS} = 0\text{ V}$; $T_j = 25\text{ °C}$
		-	23	-		$V_{DS} = 650\text{ V}$; $V_{GS} = 0\text{ V}$; $T_j = 125\text{ °C}$
Gate-source leakage current	I_{GSS}	-	0.3	-	μA	$V_{GS} = 6\text{ V}$; $V_{DS} = 0\text{ V}$
Reverse Gate leakage current	I_{RGL}	-	-5	-	μA	$V_{GS} = -6\text{ V}$; $V_{DS} = 0\text{ V}$
Drain-source on-state resistance	$R_{DS(on)}$	-	51	-	$\text{m}\Omega$	$V_{GS} = 6\text{ V}$; $I_D = 10\text{ A}$; $T_j = 25\text{ °C}$
		-	98.6	-	$\text{m}\Omega$	$V_{GS} = 6\text{ V}$; $I_D = 10\text{ A}$; $T_j = 125\text{ °C}$
Gate resistance	R_G	-	1.4	-	Ω	$f = 5\text{ MHz}$; open drain

Table 6 Dynamic characteristics

Parameters	Sym.	Values			Units	Notes/Test Conditions
		Min.	Typ.	Max.		
Input capacitance	C_{iss}	-	300	-	pF	$V_{GS} = 0\text{ V}$; $V_{DS} = 400\text{ V}$; $f = 1\text{ MHz}$
Output capacitance	C_{oss}	-	135	-	pF	
Reverse transfer capacitance	C_{rss}	-	2.3	-	pF	
Effective output capacitance, energy related ¹	$C_{o(er)}$	-	190	-	pF	$V_{GS} = 0\text{ V}$; $V_{DS} = 0\text{ to }400\text{ V}$
Effective output capacitance, time related ²	$C_{o(tr)}$	-	240	-	pF	
Output charge	Q_{oss}	-	94.7	-	nC	
Output Capacitance Stored Energy	E_{oss}	-	240	-	μJ	
Turn-on delay time	$t_{d(on)}$	-	7	-	ns	$V_{DS} = 400\text{ V}$; $I_D = 10\text{ A}$; $L = 200\text{ }\mu\text{H}$; $V_{GS} = 6\text{ V}$; $R_{on} = 15\text{ }\Omega$; $R_{off} = 2\text{ }\Omega$
Turn-off delay time	$t_{d(off)}$	-	6.8	-	ns	
Rise time	t_r	-	5.4	-	ns	
Fall time	t_f	-	2.6	-	ns	
Switching Energy during turn-on	E_{on}	-	76.1	-	μJ	
Switching Energy during turn-off	E_{off}	-	2.4	-	μJ	

1. $C_{o(er)}$ is the fixed capacitance that gives the same stored energy as C_{oss} while V_{DS} is rising from 0 to 400 V.

2. $C_{o(tr)}$ is the fixed capacitance that gives the same charging time as C_{oss} while V_{DS} is rising from 0 to 400 V.

Table 7 Gate charge characteristics

Parameters	Sym.	Values			Units	Notes/Test Conditions
		Min.	Typ.	Max.		
Gate charge	Q_G	-	8.5	-	nC	$V_{GS} = 0 \text{ to } 6 \text{ V}; V_{DS} = 400 \text{ V};$ $I_D = 10 \text{ A}$
Gate-source charge	Q_{GS}	-	0.7	-	nC	
Gate-drain charge	Q_{GD}	-	3.6	-	nC	
Gate plateau voltage	V_{plat}	-	2.3	-	V	$V_{DS} = 400 \text{ V}; I_D = 10 \text{ A}$

Table 8 Reverse conduction characteristics

Parameters	Sym.	Values			Units	Notes/Test Conditions
		Min.	Typ.	Max.		
Source-drain reverse voltage	V_{SD}	-	2.4	-	V	$V_{GS} = 0 \text{ V}; I_{SD} = 10 \text{ A}$
Pulsed current, reverse	$I_{S, \text{pulse}}$	-	-	58	A	$V_{GS} = 6 \text{ V}$
Reverse recovery charge ¹	Q_{rr}	-	0	-	nC	$I_{SD} = 10 \text{ A}; V_{DS} = 400 \text{ V}$
Reverse recovery time	t_{rr}	-	0	-	ns	
Peak reverse recovery current	I_{rrm}	-	0	-	A	

1. Excluding Q_{oss}

Electrical characteristics diagrams

at $T_j = 25\text{ }^{\circ}\text{C}$, unless otherwise specified.

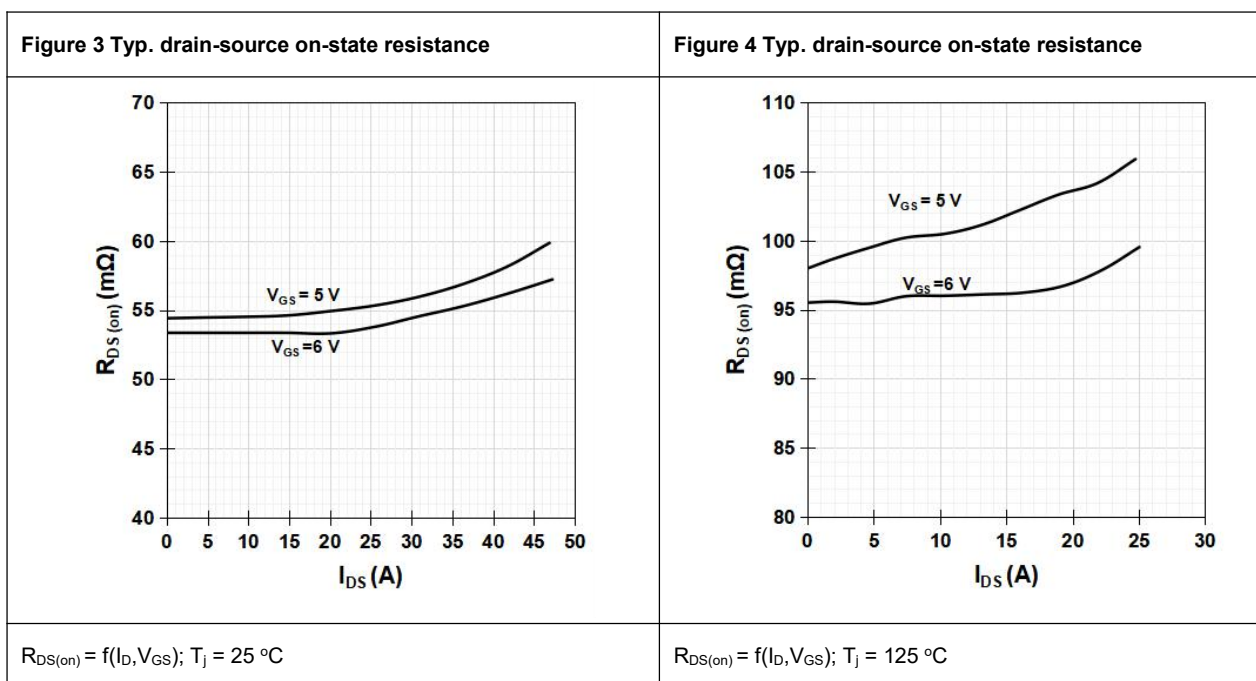
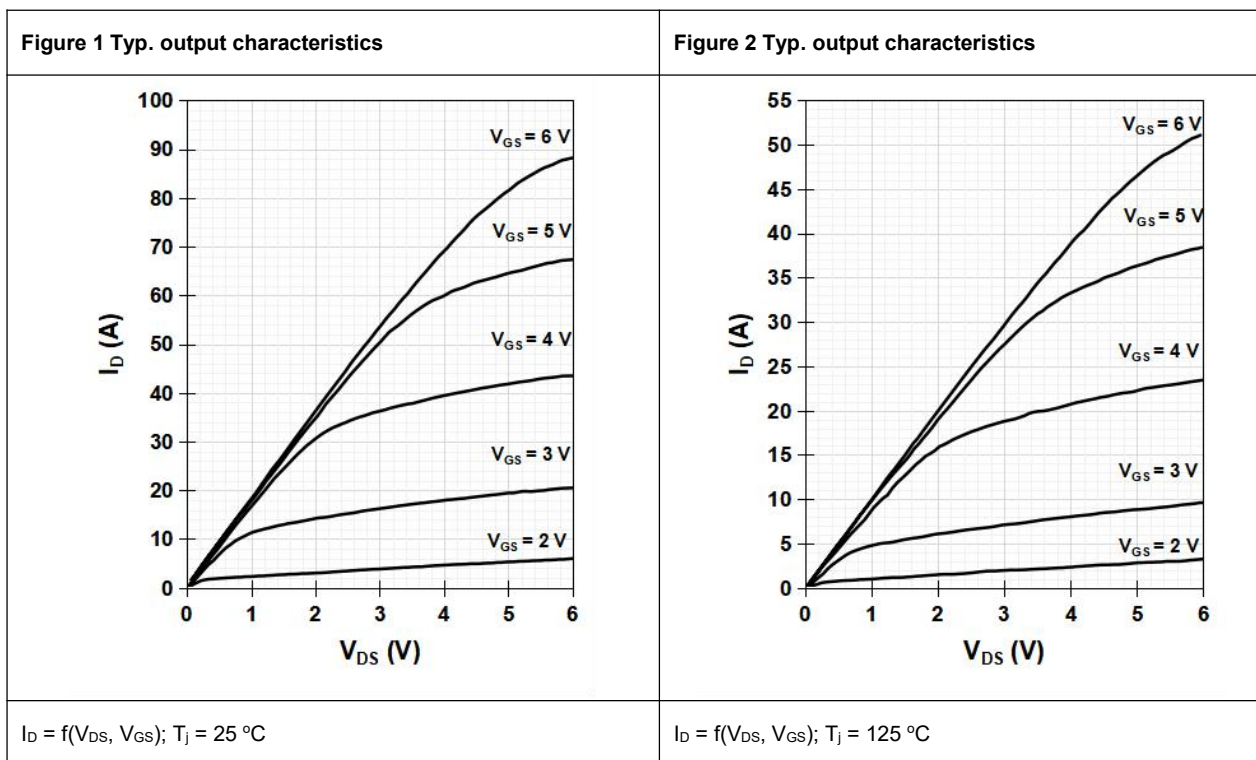
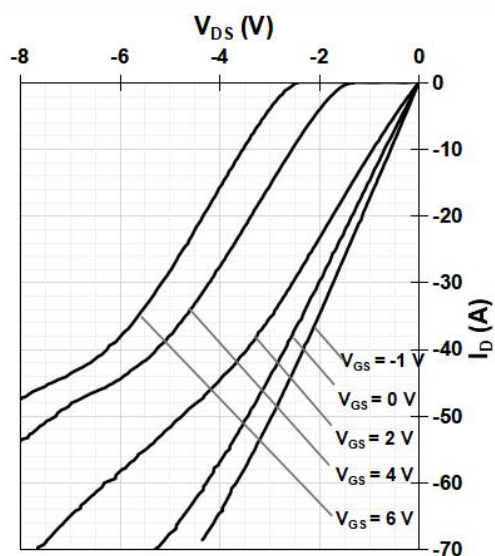
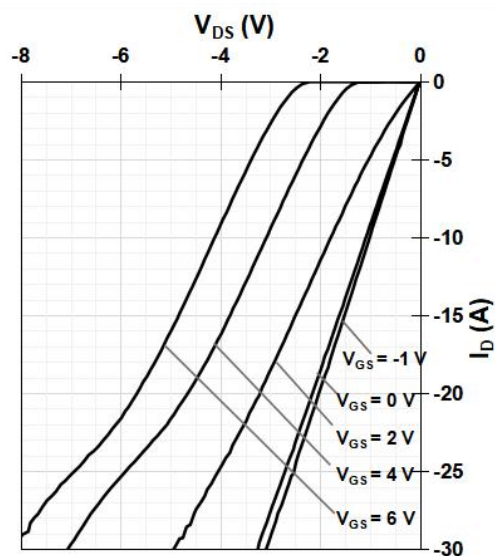


Figure 5 Typ. channel reverse characteristics



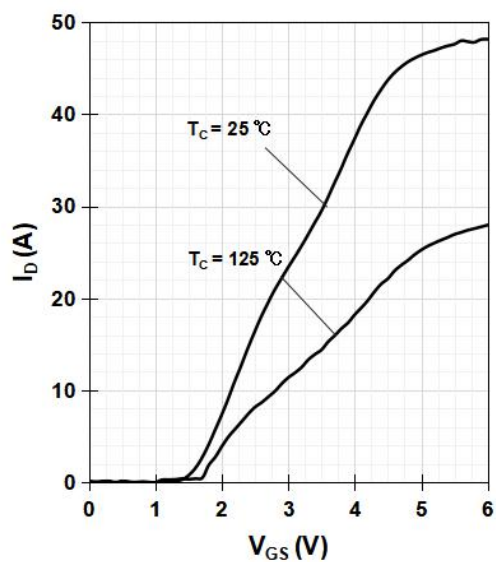
$$I_D = f(V_{DS}, V_{GS}); T_J = 25^\circ\text{C}$$

Figure 6 Typ. channel reverse characteristics



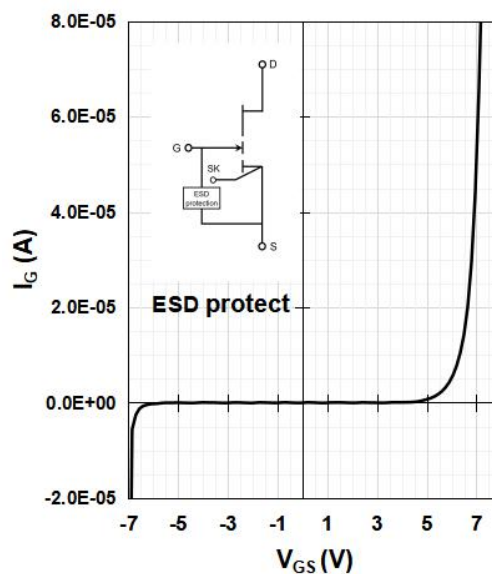
$$I_D = f(V_{DS}, V_{GS}); T_J = 125^\circ\text{C}$$

Figure 7 Typ. transfer characteristics



$$I_D = f(V_{GS}); V_{DS} = 3\text{ V}$$

Figure 8 Typ. gate-to-source leakage



$$I_G = f(V_{GS}); V_D = \text{open}$$

Figure 9 Typ. capacitances

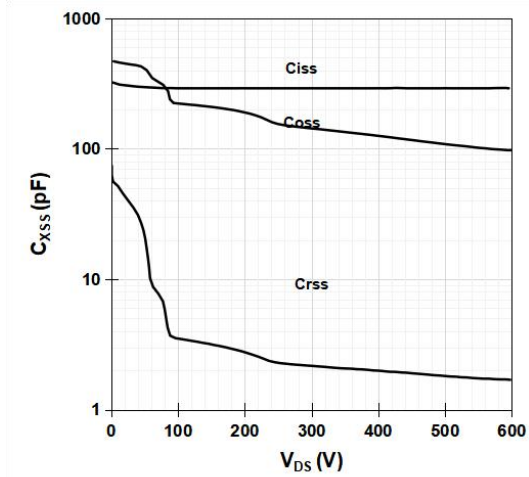

 $C_{XSS} = f(V_{DS})$; Freq. = 1 MHz

Figure 10 Typ. gate charge

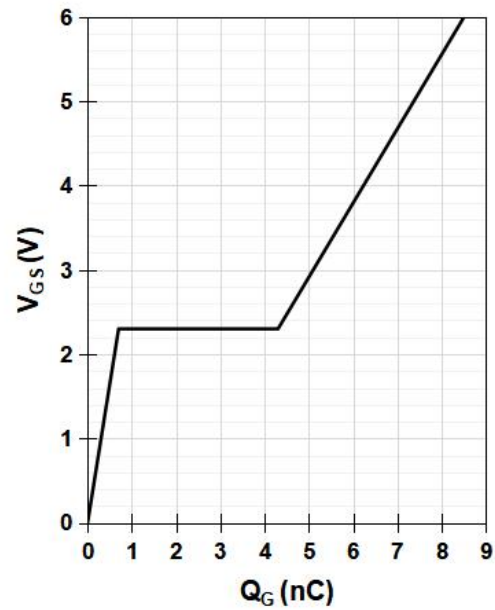

 $V_{GS} = f(Q_G)$; V_{DS} = 400 V; I_D = 10 A

Figure 11 Typ. output charge

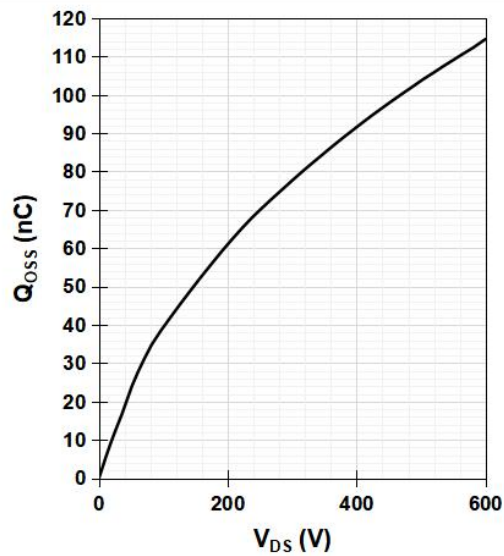

 $Q_{OSS} = f(V_{DS})$; Freq. = 1 MHz

Figure 12 Typ. Coss stored energy

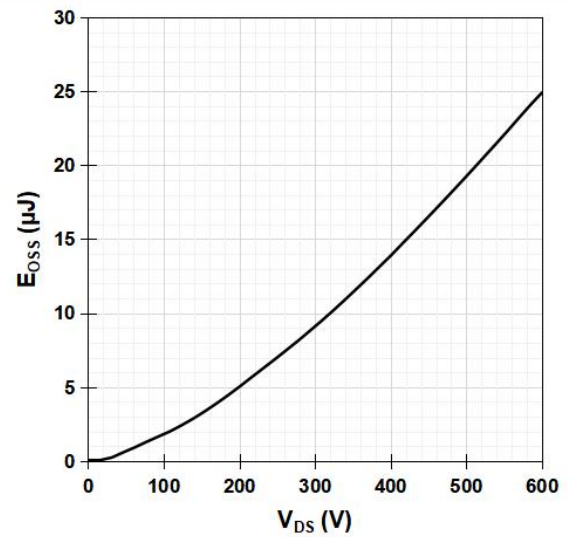
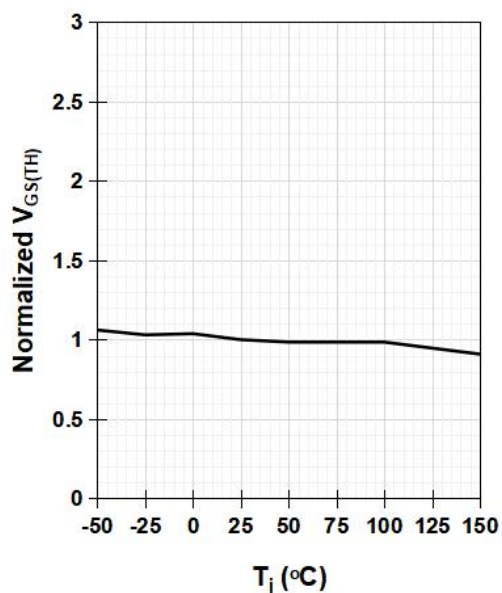
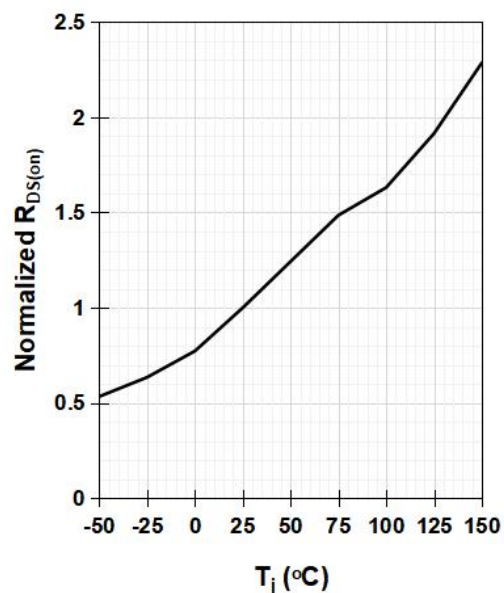

 $E_{OSS} = f(V_{DS})$; Freq. = 1 MHz

Figure 13 Gate threshold voltage



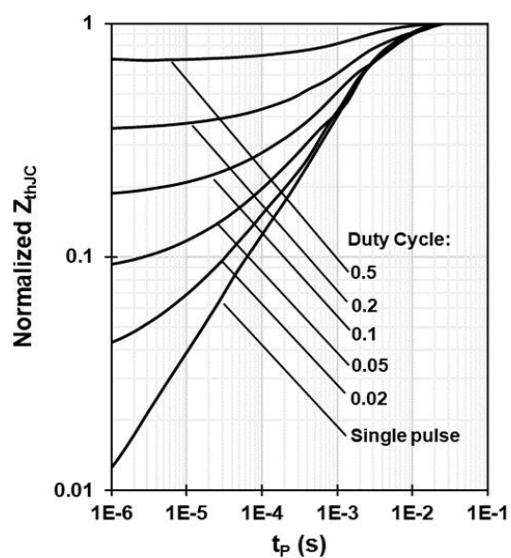
$$V_{GS(TH)} = f(T_J); V_{GS} = V_{DS}; I_D = 7.5 \text{ mA}$$

Figure 14 Drain-source on-state resistance



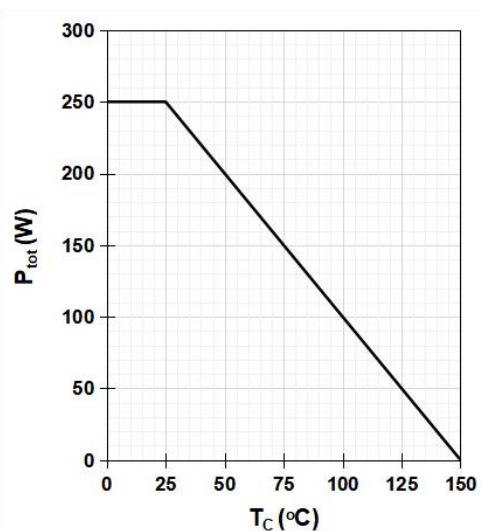
$$R_{DS(on)} = f(T_J); I_D = 9.5 \text{ A}; V_{GS} = 6 \text{ V}$$

Figure 15 Max. transient thermal impedance



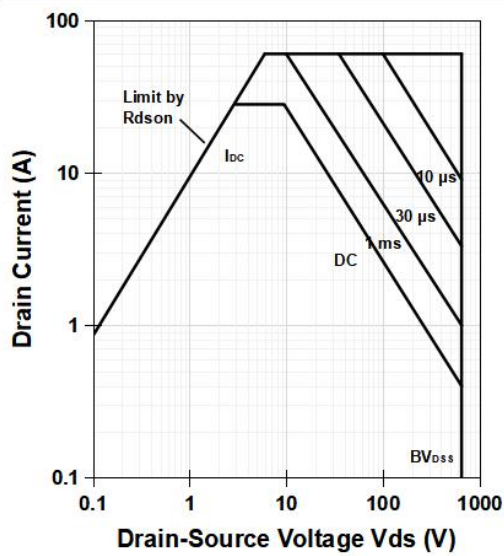
$$Z_{thJC} = f(t_p, D)$$

Figure 16 Power dissipation



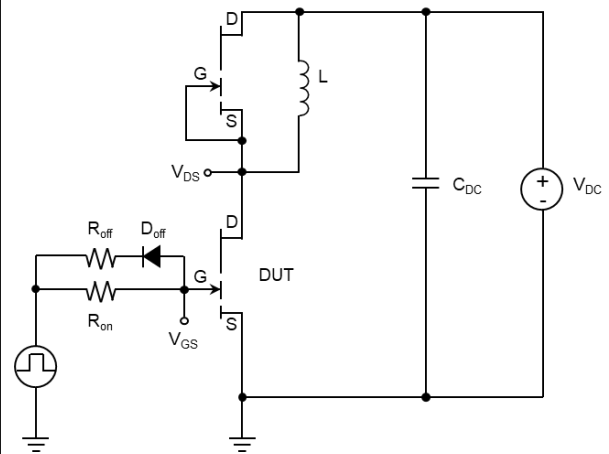
$$P_{tot} = f(T_C)$$

Figure 17 Safe operating area



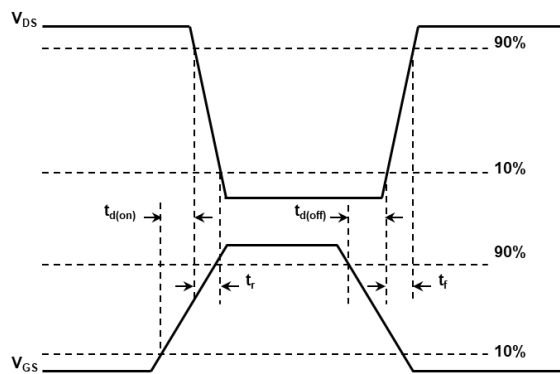
$$I_D = f(V_{DS}); T_C = 25^\circ\text{C}$$

Figure 18 Switching time test circuit

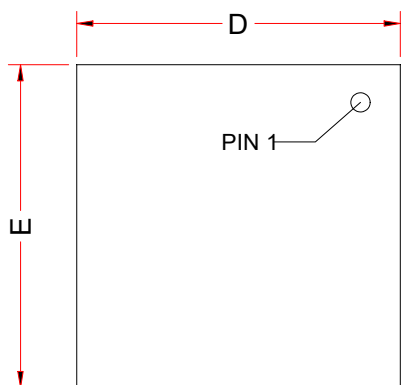


$$V_{DS} = 400\text{ V}, I_D = 10\text{ A}, L = 200\text{ }\mu\text{H}, V_{GS} = 6\text{ V}, \\ R_{on} = 15\text{ }\Omega, R_{off} = 2\text{ }\Omega$$

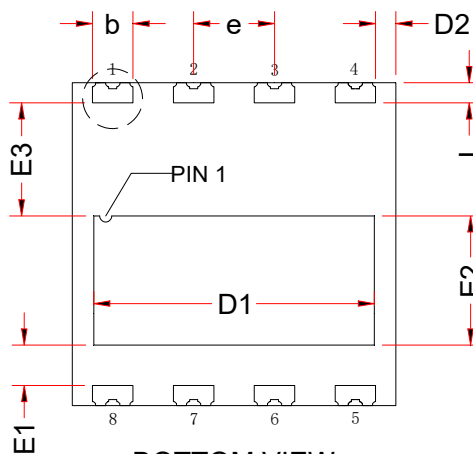
Figure 19 Typ. switching time waveform



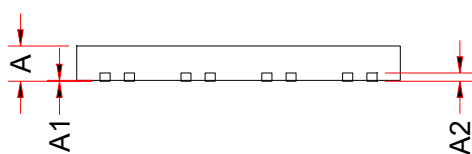
Package outlines



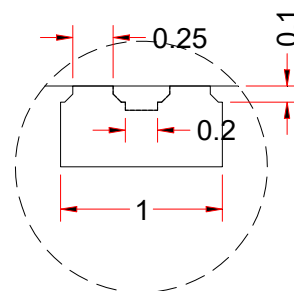
TOP VIEW



BOTTOM VIEW



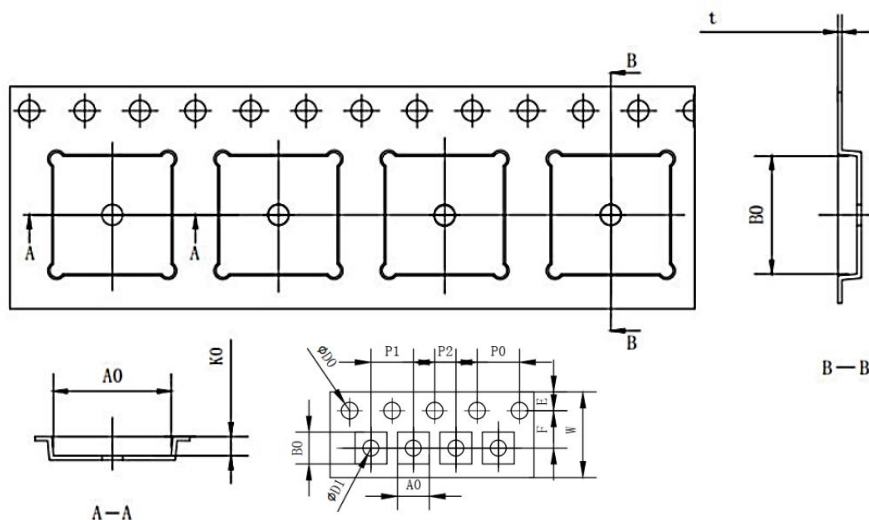
SIDE VIEW



LEAD DETAIL

	MIN	MID	MAX
A	0.75	0.85	0.95
A1	0.00	0.02	0.05
A2	0.203REF		
b	0.95	1.00	1.05
D	8.00BSC		
D1	6.84	6.94	7.04
D2	0.40	0.50	0.60
E	8.00BSC		
E1	0.90	1.00	1.10
E2	3.10	3.20	3.30
E3	2.70	2.80	2.90
e	2.00BSC		
L	0.40	0.50	0.60

Tape and reel information



SYMBOL	DIMENSION	SYMBOL	DIMENSION
W	16.00±0.30	10P0	40.00±0.20
E	1.75±0.10	P1	12.00±0.10
F	7.50±0.10	A0	8.30±0.10
D0	1.50±0.10	B0	8.30±0.10
D1	1.50±0.10	K0	1.10±0.10
P0	4.00±0.10	t	0.30±0.05
P2	2.00±0.10		

