P-Channel Enhancement Mode MOSFET

1 Features

- V_{DS} = -20V, I_D =-6.0A
- $R_{DS(ON)}$ < 45mΩ @ V_{GS}=-4.5V
- $R_{DS(ON)}$ < 60mΩ @ V_{GS}=-2.5V
- High density cell design for extremely low $R_{DS(ON)}$
- Lead free product is acquired
- ESD Protected Up to 2.0KV (HBM)
- Package SOT-23

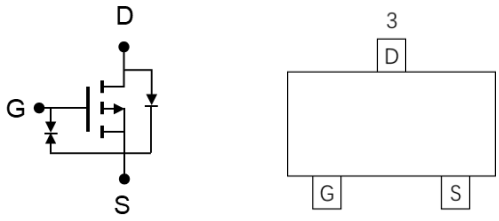
2 Applications

- Cellular Handsets and Accessories
- Personal Digital Assistants
- Portable Instrumentation
- Load switch

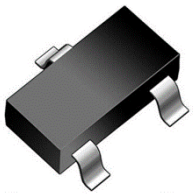
3 Description

The SLMT320V4CPE provide the best combination of fast switching, low on-resistance and cost-effectiveness. The MOSFET is the P-Channel enhancement mode power field effect transistors with high cell density, trench technology. This high density process and design have been optimized switching performance and especially tailored to minimize on-state resistance.

4 Pin Configuration and Top View



Schematic Diagram



SOT-23

5 Device Information

PART NUMBER	PACKAGE	BODY SIZE (NOM)
SLMT320V4CPE	SOT-23	2.90 mm x 2.40mm

6 Absolute maximum Ratings @25℃

RATING	SYMBOL	VALUE	UNITS
Drain-Source Voltage	V_{DS}	-20	V
Gate-Source Voltage	V_{GS}	±10	V
Continuous Drain Current	I_D	-6.0	A
Pulsed Drain Current	I_{DP}	-30	A
Total power dissipation	P_D	1.5	W
Channel temperature	T_J	-55 to +150	℃
Range of storage temperature	T_{STG}	-55 to +150	℃
Thermal Resistance, Junction to Ambient	$R_{\theta JA}$	83	℃/W

7 Electrical characteristics (@25℃ unless otherwise specified)

PARAMETER	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNITS
Static Characteristics						
Drain-Source Breakdown Voltage	BV_{DSS}	I_D = -250μA, V_{GS} = 0V	-20			V
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = 250μA	-0.45	-0.8	-1.2	V
Drain Cut Off Current	I_{DSS}	V_{DS} = -20V, V_{GS} = 0V			-1	μA
Gate Leakage Current	I_{GSS}	V_{GS} = ±10V, V_{DS} = 0V			±10	μA
Drain-Source ON Resistance	$R_{DS(ON)}$	V_{GS} = -4.5V, I_D = -3A		30	45	mΩ
		V_{GS} = -2.5V, I_D = -2A		47	60	mΩ
Dynamic Characteristics						
Total Gate Charge	Q_G	V_{DS} =-10V,		13		nC
Gate-Source Charge	Q_{GS}	I_D =-4A,		3		nC
Gate-Drain Charge	Q_{GD}	V_{GS} = -4.5V		2		nC
Input Capacitance	C_{ISS}	V_{DS} = -10V,		540		pF
Reverse Transfer Capacitance	C_{RSS}	V_{GS} = 0V,		100		pF
Output Capacitance	C_{OSS}	f = 1MHz		120		pF
Turn-On Delay Time	$t_{d(on)}$	V_{GS} =-4.5V, V_{DS} =-10V, R_L =2.5Ω, R_G =3Ω		5		ns
Turn-Off Delay Time	$t_{d(off)}$			50		ns
Rise Time	t_r			45		ns
Fall Time	t_f			68		ns
Drain-Source Body Diode Characteristics						
Source-Drain Diode Forward Voltage	V_{SD}	I_S = -4A, V_{GS} = 0V		-0.8	-1.2	V

8 Typical Characteristics

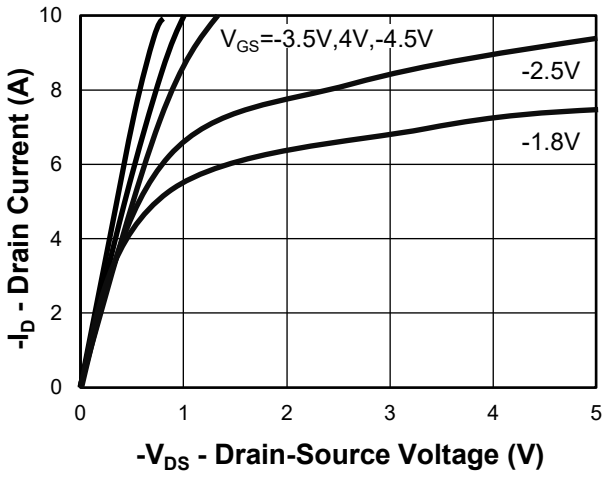


Fig 1. Output Characteristics

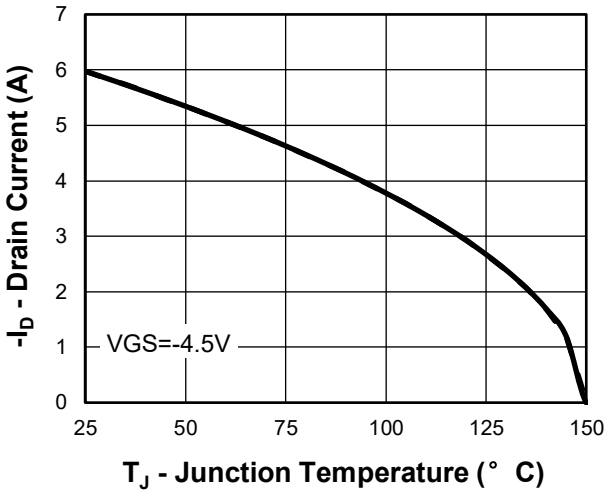


Fig 2. Drain Current

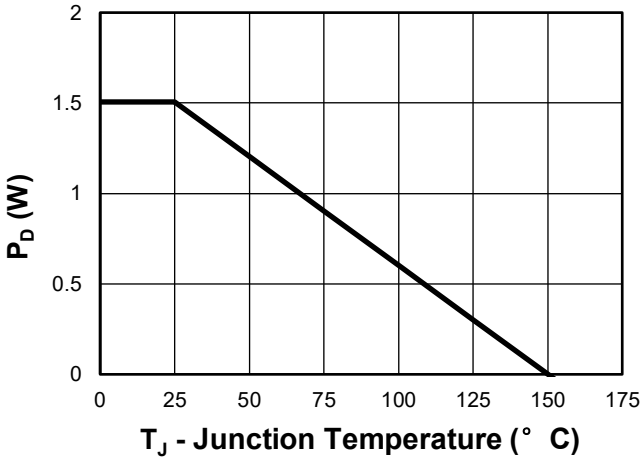


Fig 3. Power Dissipation

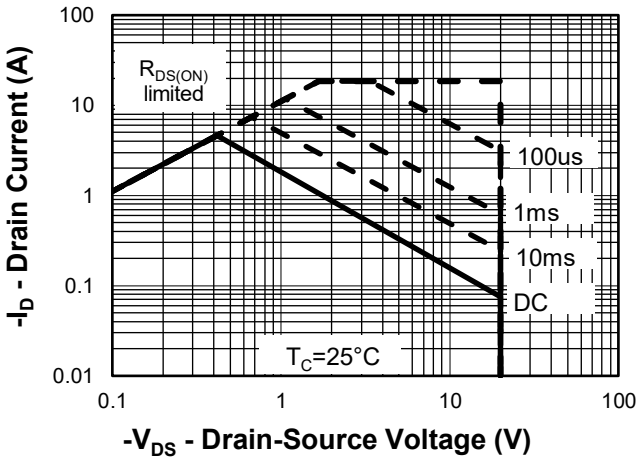


Fig 4. Safe Operation Area(SOA)

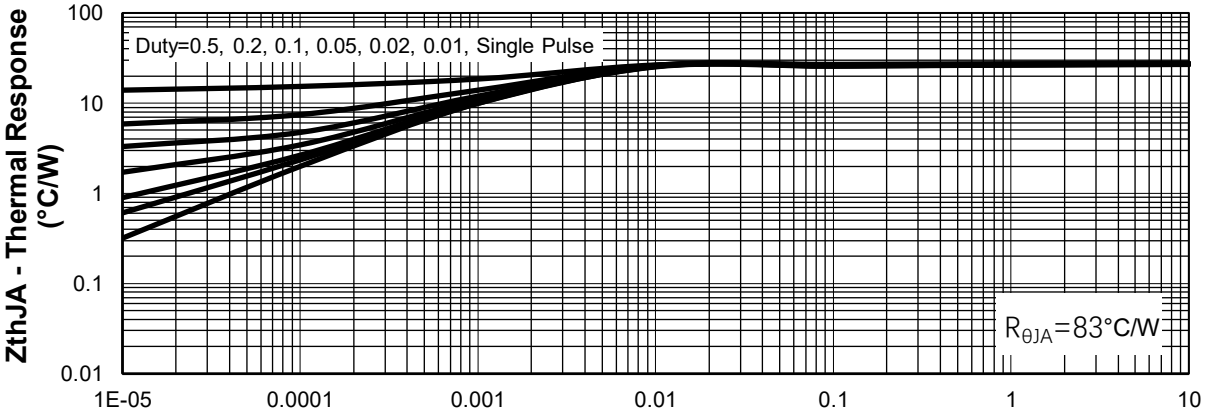


Fig 5. Thermal Transient Impedance

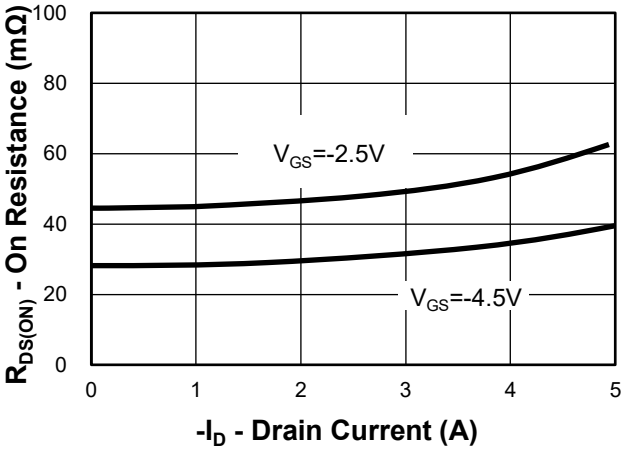


Fig 6. Rdson vs. Drain Current Characteristics

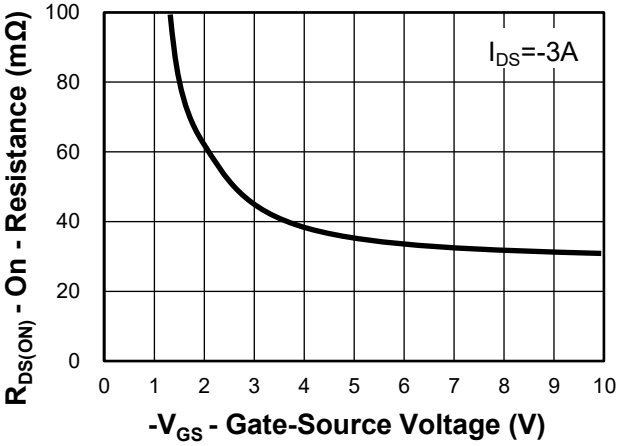


Fig 7. Gate-Source on Resistance

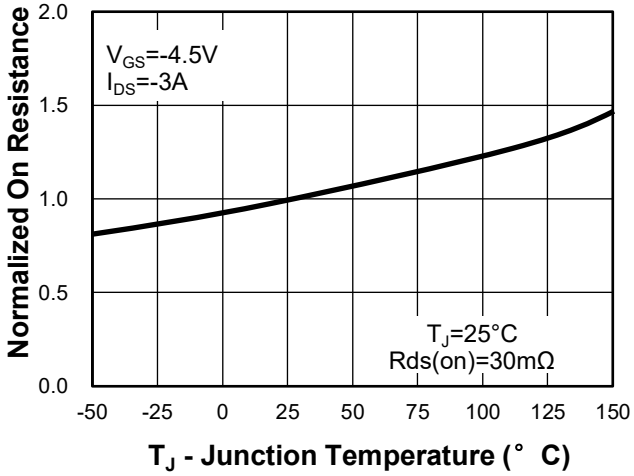


Fig 8. Rdson vs. Junction Tem Characteristics

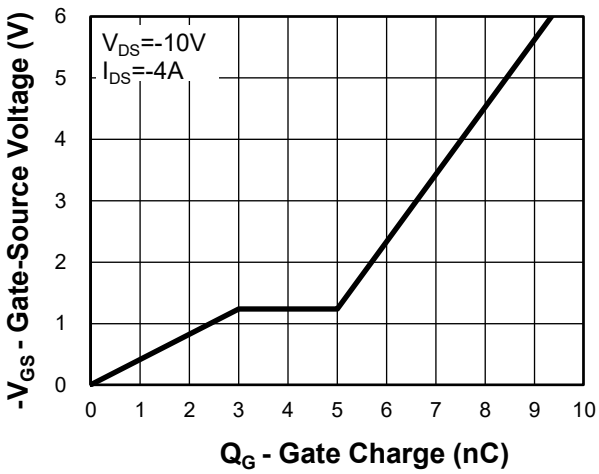


Fig 9. Gate Charge Characteristics

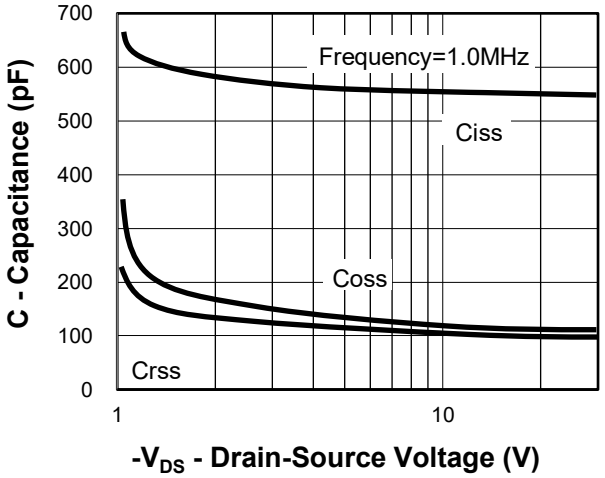


Fig 10. Capacitance Characteristics

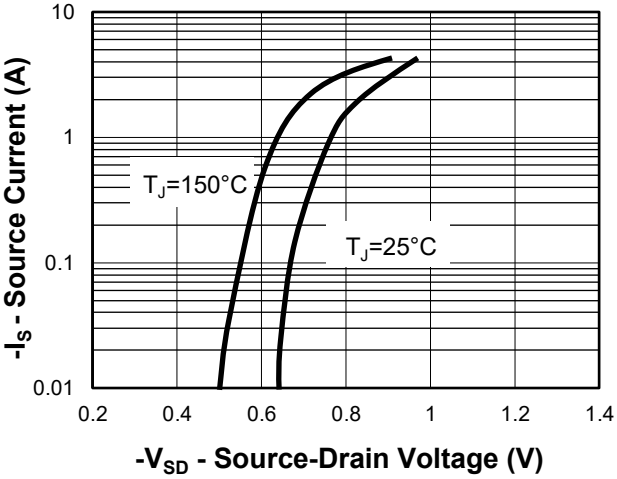
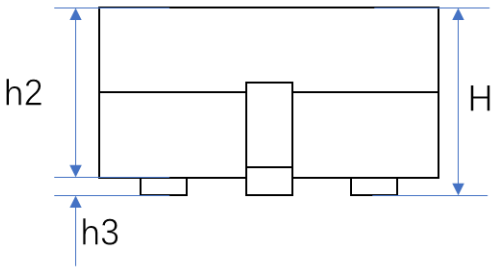
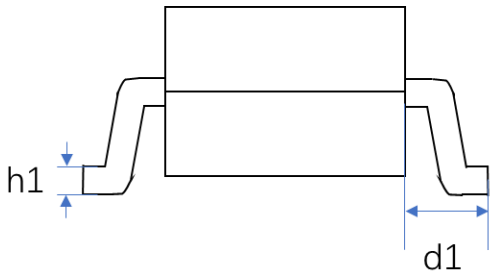


Fig 11. Source-Drain Diode Forward

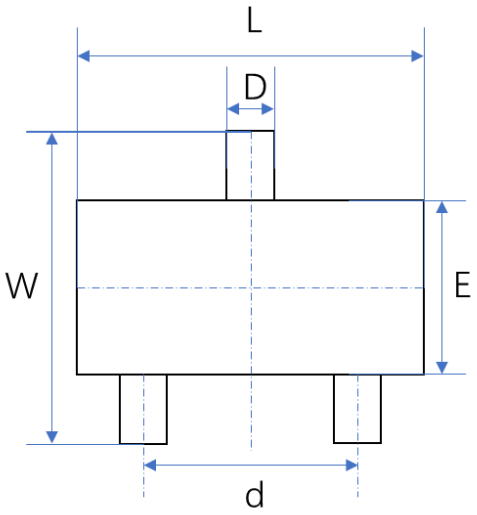
9 Product dimension

SOT-23

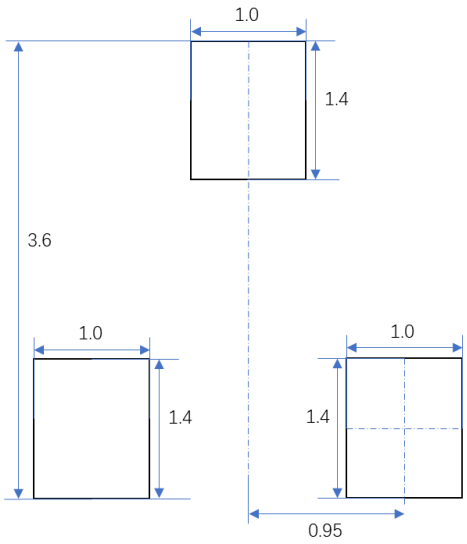




DIM	UNITS (mm)		
	MIN.	TYP.	MAX.
L	2.70	-	3.12
W	2.10	-	2.64
D	0.30	-	0.50
E	1.10	-	1.50
d	1.80	-	2.00
d1	-	0.55	-
H	0.90	-	1.15
h1	0.08	-	0.21
h2	0.86	-	1.05
h3	0.04	-	0.15



10 PCB Layout Footprints (Units: mm)



11 Ordering Information

Part Number	Packaging	Reel Size
SLMT320V4CPE	3000/Tape & Reel	7 inch