LPDDR4/4X Datasheet

RS256M32LZ4D2BNP-62BT

200-ball

Revision 1.2

Mar. 20. 2025

Revision History

Version	Date	Changes
V1.0	2023-4-16	Basic spec and architecture
V1.1	2024-7-4	1) Change discrete package dimension 2) Change pad definition
V1.2	2025-3-20	1) Add IDD parameters 2) Add Mode Registers

Notes: *This data sheet contains minimum and maximum limits specified over the power supply and temperature range set forth herein. Although considered final, these specifications are subject to change at any time without notice, as further product development and data characterization sometimes occur.*

Contents

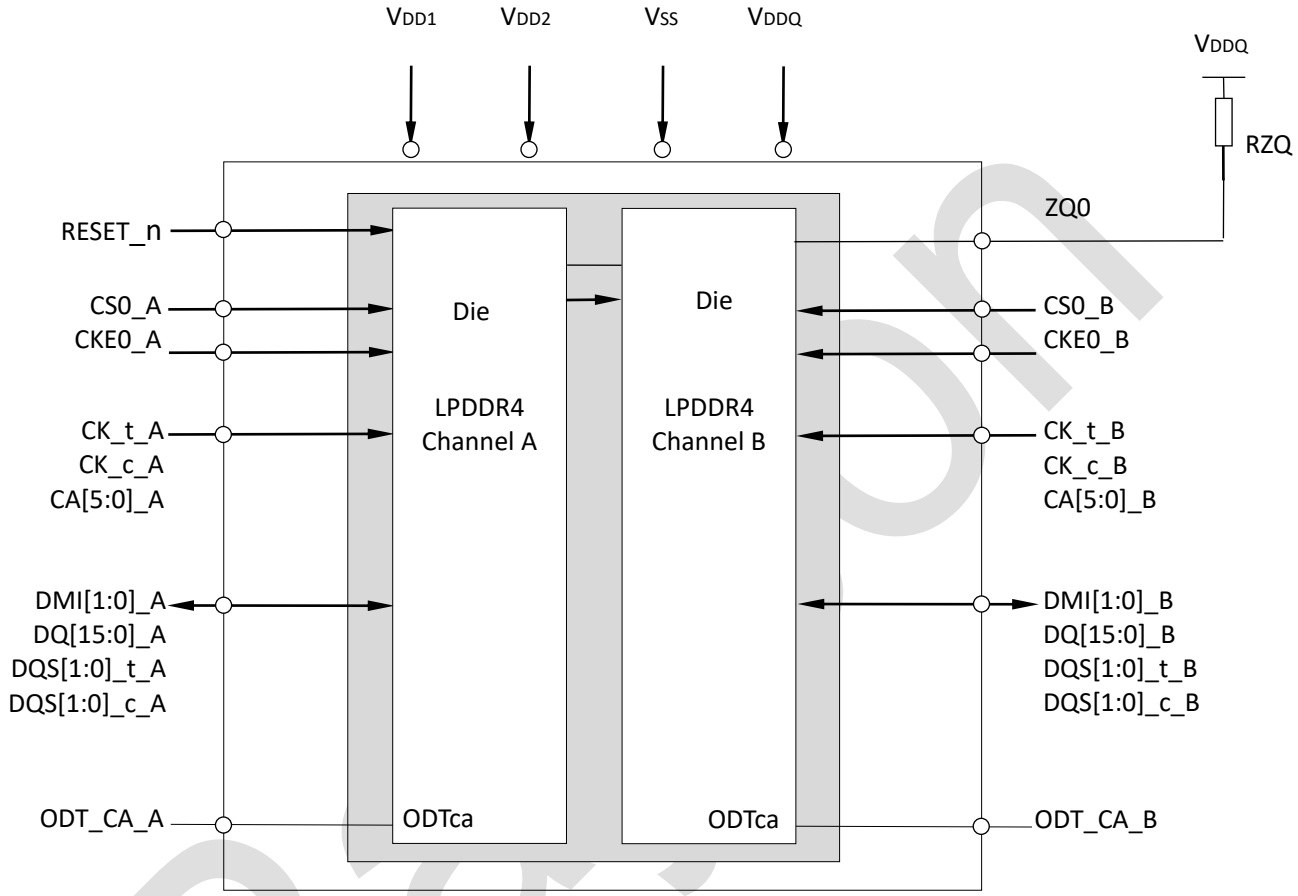
1. Product Overview

1.1. Feature Overview

- Ultra-low-voltage core and I/O power supplies
  - V_{DD1} = 1.70-1.95V; 1.80V nominal
  - V_{DD2} = 1.06-1.17V; 1.10V nominal
  - V_{DDQ} = 0.57-0.65V; 0.60V nominal Or V_{DDQ} = 1.06-1.17V; 1.10V nominal
- Frequency range
  - 1600-10 MHz (data rate range per pin:3200-20Mbp/s)
- 16n prefetch DDR architecture
- 8 internal banks per channel for concurrent operation
- Single-data-rate CMD / ADR entry
- Bidirectional / differential data strobe per byte lane
- Programmable READ and WRITE latencies (RL / WL)
- Programmable and on-the-fly burst lengths (BL = 16, 32)
- Directed per-bank refresh for concurrent bank operation and ease of command scheduling
- Up to 8.53 GB / s per die x16 channel
- On-chip temperature sensor to control self refresh rate
- Partial-array self refresh (PASR)
- Selectable output drive strength (DS)
- Clock-stop capability
- RoHS-compliant, “green” packaging
- V_{DD1}/V_{DD2}/V_{DDQ}: 1.80V/1.10V/0.60V or 1.10V
- Array configuration
  - 256 Meg x 32 (2 channels x 16 I/O)
  - 256M16 x 2 die in package
- FBGA “green” package
  - 200-ball FBGA (10mm x14.5mm x1.02mm Max)
- Speed grade,cycle time
  - 625ps@ RL = 28/32
- Operating temperature range
  - -25°C to + 85°C

2. Physical Specifications

2.1. Function Block Diagram



Dual-Die, Dual-Channel Single-Rank Package Block Diagram

2.2. Package ballout & Addressing

200-Ball Dual-Channel, Single-Rank Discrete FBGA

	1	2	3	4	5	6	7	8	9	10	11	12
A	DNU	DNU	V_{SS}	V_{DD2}	ZQ0			NC	V_{DD2}	V_{SS}	DNU	DNU
B	DNU	DQ0_A	V_{DDQ}	DQ7_A	V_{DDQ}			V_{DDQ}	DQ15_A	V_{DDQ}	DQ8_A	DNU
C	V_{SS}	DQ1_A	DMI0_A	DQ6_A	V_{SS}			V_{SS}	DQ14_A	DMI1_A	DQ9_A	V_{SS}
D	V_{DDQ}	V_{SS}	DQS0_t_A	V_{SS}	V_{DDQ}			V_{DDQ}	V_{SS}	DQS1_t_A	V_{SS}	V_{DDQ}
E	V_{SS}	DQ2_A	DQS0_c_A	DQ5_A	V_{SS}			V_{SS}	DQ13_A	DQS1_c_A	DQ10_A	V_{SS}
F	V_{DD1}	DQ3_A	V_{DDQ}	DQ4_A	V_{DD2}			V_{DD2}	DQ12_A	V_{DDQ}	DQ11_A	V_{DD1}
G	V_{SS}	ODT_CA_A	V_{SS}	V_{DD1}	V_{SS}			V_{SS}	V_{DD1}	V_{SS}	NC	V_{SS}
H	V_{DD2}	CA0_A	NC	CS0_A	V_{DD2}			V_{DD2}	CA2_A	CA3_A	CA4_A	V_{DD2}
J	V_{SS}	CA1_A	V_{SS}	CKE0_A	NC			CK_t_A	CK_c_A	V_{SS}	CA5_A	V_{SS}
K	V_{DD2}	V_{SS}	V_{DD2}	V_{SS}	NC			NC	V_{SS}	V_{DD2}	V_{SS}	V_{DD2}
L												
M												
N	V_{DD2}	V_{SS}	V_{DD2}	V_{SS}	NC			NC	V_{SS}	V_{DD2}	V_{SS}	V_{DD2}
P	V_{SS}	CA1_B	V_{SS}	CKE0_B	NC			CK_t_B	CK_c_B	V_{SS}	CA5_B	V_{SS}
R	V_{DD2}	CA0_B	NC	CS0_B	V_{DD2}			V_{DD2}	CA2_B	CA3_B	CA4_B	V_{DD2}
T	V_{SS}	ODT_CA_B	V_{SS}	V_{DD1}	V_{SS}			V_{SS}	V_{DD1}	V_{SS}	RESET_n	V_{SS}
U	V_{DD1}	DQ3_B	V_{DDQ}	DQ4_B	V_{DD2}			V_{DD2}	DQ12_B	V_{DDQ}	DQ11_B	V_{DD1}
V	V_{SS}	DQ2_B	DQS0_c_B	DQ5_B	V_{SS}			V_{SS}	DQ13_B	DQS1_c_B	DQ10_B	V_{SS}
W	V_{DDQ}	V_{SS}	DQS0_t_B	V_{SS}	V_{DDQ}			V_{DDQ}	V_{SS}	DQS1_t_B	V_{SS}	V_{DDQ}
Y	V_{SS}	DQ1_B	DMI0_B	DQ6_B	V_{SS}			V_{SS}	DQ14_B	DMI1_B	DQ9_B	V_{SS}
AA	DNU	DQ0_B	V_{DDQ}	DQ7_B	V_{DDQ}			V_{DDQ}	DQ15_B	V_{DDQ}	DQ8_B	DNU
AB	DNU	DNU	V_{SS}	V_{DD2}	V_{SS}			V_{SS}	V_{DD2}	V_{SS}	DNU	DNU

Top View

LPDDR4_A(Channel A） LPDDR4_B(Channel B） ZQ,ODT_CA,RESET Supply Ground

2.3. Pad Definition

"_A" and "_B" indicate DRAM channels. "_A" pads are present in all devices while "_B" pads are present in dual channel SDRAM devices only.

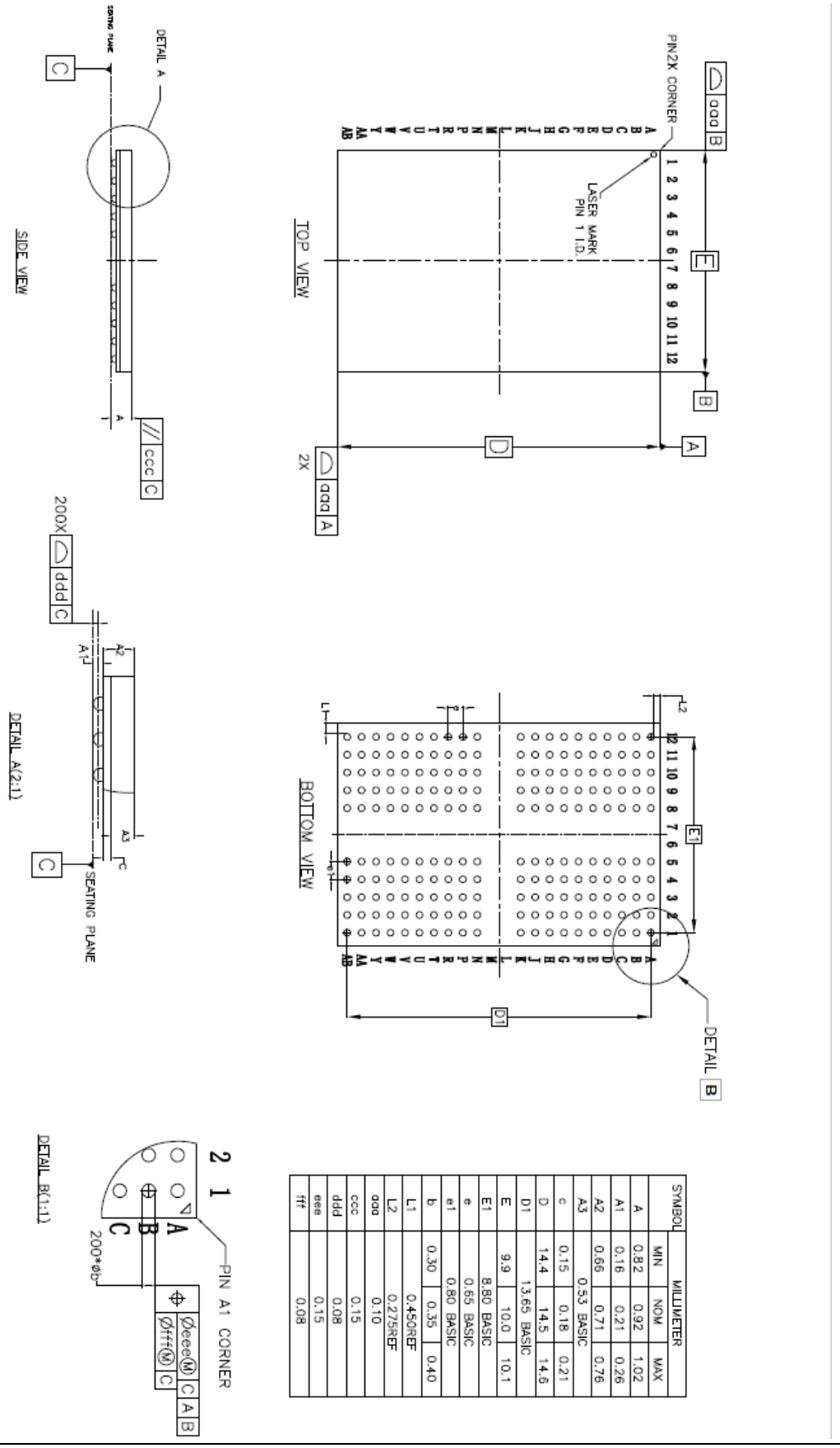
LPDDR4X pad definitions are the same as LPDDR4, except ODT_CA pins as described in the following Table

Symbol	Type	Description
CK_t_A, CK_c_A CK_t_B, CK_c_B	Input	**Clock:** CK_t and CK_c are differential clock inputs. All address, command and control input signals are sampled on positive edge of CK_t and the negative edge of CK_c.AC timings for CA parameters are referenced to clock. Each channel (A, B) has its own clock pair.
CKE0_A, CKE0_B	Input	**Clock enable:** CKE HIGH activates and CKE LOW deactivates the internal clock signals, input buffers, and output drivers. Power-saving modes are entered and exited via CKE transitions. CKE is sampled at the rising edge of CK.
CS0_A, CS0_B	Input	**Chip select:** Each channel (A, B) has its own CS signals.
CA[5:0]_A CA[5:0]_B	Input	**Command/address inputs:** Provide the command and address inputs according to the command truth table. Each channel (A, B) has its own CA signals.
ODT_CA_A ODT_CA_B	Input	**CA ODT Control:** The ODT_CA pin is ignored by LPDDR4X devices. CA ODT is fully controlled through MR11 and MR22. The ODT_CA pin shall be connected to a valid logic level.
DQ[15:0]_A DQ[15:0]_B	I/O	**Data input/output:** Bidirectional data bus.
DQS[1:0]_t_A DQS[1:0]_c_A DQS[1:0]_t_B DQS[1:0]_c_B	I/O	**Data strobe:** DQS_t and DQS_c are bidirectional differential output clock signals used to strobe data during a READ or WRITE. The data strobe is generated by the DRAM for a READ and is edge-aligned with data. The data strobe is generated by the SoC memory controller for a WRITE and is trained to precede data. Each byte of data has a data strobe signal pair. Each channel (A, B) has its own DQS_t and DQS_c strobes.
DMI[1:0]_A DMI[1:0]_B	I/O	**Data mask/Data bus inversion:** DMI is a dual use bidirectional signal used to indicate data to be masked, and data which is inverted on the bus. For data bus inversion(DBI), the DMI signal is driven HIGH when the data on the data bus is inverted, or driven LOW when the data is in its normal state. DBI can be disabled via a mode register setting. For data mask, the DMI signal is used in combination with the data lines to indicate data to be masked in a MASK WRITE command (see the Data Mask (DM) and Data Bus Inversion (DBI) sections for details). The data mask function can be disabled via a mode register setting. Each byte of data has a DMI signal. Each channel has its own DMI signals.

Symbol	Type	Description
ZQ0	Reference	**ZQ calibration reference:** Used to calibrate the output drive strength and the termination resistance. The ZQ pin shall be connected to V_{DDQ} through a 240Ω ±1% resistor.
V_{DDQ}, V_{DD1}, V_{DD2}	Supply	**Power supplies:** Isolated on the die for improved noise immunity.
V_{SS}	Supply	**Ground reference:** Power supply ground reference.
RESET_n	Input	**RESET:** When asserted LOW, the RESET pin resets all channels of the die.
DNU	–	**Do not use:** Must be grounded or left floating.
NC	–	**No connect:** Not internally connected.

2.4. Discrete Package Dimension

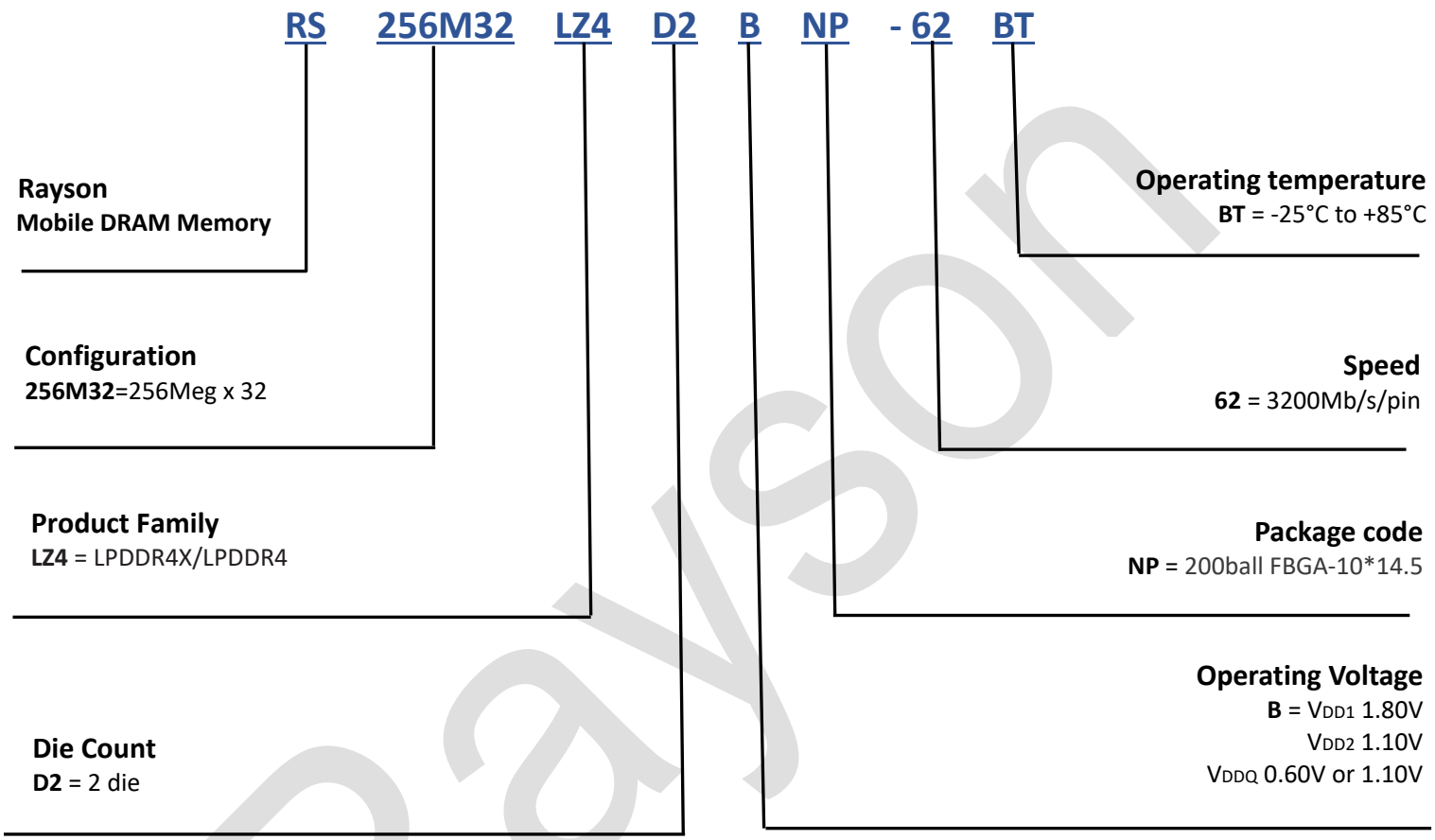
10mm X14.5mm



SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	0.82	0.92	1.02
A1	0.16	0.21	0.26
A2	0.66	0.71	0.76
A3		0.53 BASIC	
c	0.15	0.18	0.21
D	14.4	14.5	14.6
D1		13.65 BASIC	
E	9.9	10.0	10.1
E1		8.80 BASIC	
e		0.65 BASIC	
e1		0.80 BASIC	
b	0.30	0.35	0.40
L1		0.450REF	
L2		0.275REF	
aaa		0.10	
ccc		0.15	
ddd		0.08	
eee		0.15	
fff		0.08	

3. Core Specifications

3.1. Part Number Decoding



3.2. Ordering Options

Table 1: Key Timing Parameters

Speed Grade	Clock Rate (MHz)	Data Rate (Mb/s/pin)	WRITE Latency		READ Latency	
			Set A	Set B	DBI Disabled	DBI Enabled
-62	1600	3200	14	26	28	32

Table 2: Part Number List

Part Number	Total Density	Data Rate	Operating temperature
RS256M32LZ4D2BNP-62BT	1GB(8Gb)	3200Mb/s/pin	-25°C to + 85°C

Table 3: Refresh Requirement Parameters

Parameter	Symbol	4Gb Per Channel	unit
REFRESH cycle time (all banks)	^{t}RFCab	180	ns
REFRESH cycle time (per bank)	^{t}RFCpb	90	ns
Per bank refresh to per bank refresh time (different bank)	^{t}PBR2PBR	90	ns

3.3. Die Addressing Table

Configuration		256M32 (8Gb/package)
Die Configuration	Channel A, rank 0	x16 mode × 1 die
	Channel B, rank 0	x16 mode × 1 die
	Channel A, rank 1	-
	Channel B, rank 1	
Die Addressing	Memory density (per die)	4Gb
	Memory density (per channel)	4Gb
	Configuration	32Mb × 16 DQ × 8 banks x 2channels x 1 rank
	Number of channels (per die)	1
	Number of banks (per channel)	8
	Array prefetch (bits, per channel)	256
	Number of rows (per channel)	32,768
	Number of columns (fetch boundaries)	64
	Page size (bytes)	2048
	Channel density (bits per channel)	4,294,967,296
	Total density (bits per die)	4,294,967,296
	Bank address	BA[2:0]
	Row address	R[14:0]
	Column address	C[9:0]
	Burst starting address boundary	64-bit

Notes： *1、Refer to Package Block Diagrams section in Product specification and SDRAM Addressing Section in General LPDDR4X specification.*

2、Refer to Byte Mode section for further information

3.4. Mode Register Contens

MR0		
OP7		**OP[0] = 0b:** Both legacy and modified refresh mode supported **OP[1] = 0b:** Device supports normal latency **OP[5] = 1b:** Device supports Single-ended Mode
OP6		
OP5	Single-ended Mode	
OP4		
OP3		
OP2		
OP1	Latency Mode	
OP0	REF	

MR3		
OP7		**OP[2] = 0b**:PPR protection disabled (default) **1b:** PPR protection enabled
OP6		
OP5		
OP4		
OP3		
OP2	PPRP3	
OP1		
OP0		

MR5		
OP7	Manufacturer ID	1111 1111b : Micron
OP6		
OP5		
OP4		
OP3		
OP2		
OP1		
OP0		

MR6		
OP7	Revision ID1	**1000 0000b**
OP6		
OP5		
OP4		
OP3		
OP2		
OP1		
OP0		

MR8		
OP7	I/O width	**OP[7:6] = 00b:** x16/channel
OP6		
OP5	Density	**OP[5:2]** = **0010b:** 4Gb single channel die
OP4		
OP3		
OP2		
OP1		
OP0		

MR13		
OP7		**OP[2]=0b**:Normal operation (default) **1b**: Output the $V_{REF(CA)}$ value on DQ7 and $V_{REF(DQ)}$ value on DQ6
OP6		
OP5		
OP4		
OP3		
OP2	VR0	
OP1		
OP0		

Notes : *1、The contents of Product Specific Mode Register definition will reflect information specific to each die in these package.*

2、Other bits not defined above and other mode registers are referred to in Mode Register Assignments and Definitions section.

4. Mode Registers

Mode register definitions are provided in the Mode Register Assignments table. In the access column of the table, R indicates read-only; W indicates write-only; R/W indicates read- or write-capable or enabled. The MRR command is used to read from a register. The MRW command is used to write to a register.

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MR#	MA[5:0]	Function	Access	OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
0	00h	Device info	R	RFU			RZQI		RFU	Latency mode	REF
1	01h	Device feature 1	W	RD-PST	*n*WR (for AP)			RD-PRE	WR-PRE	BL	
2	02h	Device feature 2	W	WR Lev	WLS	WL			RL		
3	03h	I/O config-1	W	DBI-WR	DBI-RD	PDDS			PPRP	WR-PST	PU-CAL
4	04h	Refresh and training	R /W	TUF	Thermal offset		PPRE	SR abort	Refresh rate		
5	05h	Basic config-1	R	Manufacturer ID							
6	06h	Basic config-2	R	Revision ID1							
7	07h	Basic config-3	R	Revision ID2							
8	08h	Basic config-4	R	I/O width		Density				Type	
9	09h	Test mode	W	Vendor-specific test mode							
10	0Ah	I/O calibration	W	RFU							ZQ RST
11	0Bh	ODT	W	RFU	CA ODT			RFU	DQ ODT		
12	0Ch	$V_{REF(CA)}$	R/W	RFU	VR_{CA}	$V_{REF(CA)}$					
13	0Dh	Register control	W	FSP-OP	FSP-WR	DMD	RRO	VRCG	VRO	RPT	CBT
14	0Eh	$V_{REF(DQ)}$	R/W	RFU	VR_{DQ}	$V_{REF(DQ)}$					
15	0Fh	DQI-LB	W	Lower-byte invert register for DQ calibration							
16	10h	PASR_Bank	W	PASR bank mask							
17	11h	PASR_Seg	W	PASR segment mask							
18	12h	IT-LSB	R	DQS oscillator count – LSB							
19	13h	IT-MSB	R	DQS oscillator count – MSB							
20	14h	DQI-UB	W	Upper-byte invert register for DQ calibration							
21	15h	Vendor use	W	RFU							
22	16h	ODT feature 2	W	ODTD for x8_2ch		ODTD -CA	ODTE -CS	ODTE -CK	SoC ODT		

Table 1: Mode Register Assignments (Continued)

Notes 1–5 apply to entire table

MR#	MA[5:0]	Function	Access	OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
23	17h	DQS oscillator stop	W	DQS oscillator run-time setting							
24	18h	TRR control	R/W	TRR mode	TRR mode BAn			Unltd MAC	MAC value		
25	19h	PPR resources	R	B7	B6	B5	B4	B3	B2	B1	B0
26–29	1Ah~1Dh	–	–	Reserved for future use							
30	1Eh	Reserved for test	W	SDRAM will ignore							
31	1Fh	–	–	Reserved for future use							
32	20h	DQ calibration pattern A	W	See DQ calibration section							
33–38	21h≈26h	Do not use	–	Do not use							
39	27h	Reserved for test	W	SDRAM will ignore							
40	28h	DQ calibration pattern B	W	See DQ calibration section							
41–47	29h≈2Fh	Do not use	–	Do not use							
48–63	30h≈3Fh	Reserved	–	Reserved for future use							

Notes:
1. RFU bits must be set to 0 during MRW commands.
2. RFU bits are read as 0 during MRR commands.
3. All mode registers that are specified as RFU or write-only shall return undefined data when read via an MRR command.
4. RFU mode registers must not be written.
5. Writes to read-only registers will not affect the functionality of the device.

Table 2: MR0 Device Feature 0 (MA[5:0] = 00h)

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
RFU			RZQI		RFU	Latency mode	REF

Table 3: MR0 Op-Code Bit Definitions

Register Information	Type	OP	Definition	Notes
Refresh mode	Read-only	OP[0]	0b: Both legacy and modified refresh mode supported 1b: Only modified refresh mode supported	
Latency mode	Read-only	OP[1]	0b: Device supports normal latency 1b: Device supports byte mode latency	5, 6

Table 3: MR0 Op-Code Bit Definitions (Continued)

Register Information	Type	OP	Definition	Notes
Built-in self-test for RZQ information	Read-only	OP[4:3]	00b: RZQ self-test not supported 01b: ZQ may connect to V_{SSQ} or float 10b: ZQ may short to V_{DDQ} 11b: ZQ pin self-test completed, no error condition detected (ZQ may not connect to V_{SSQ}, float, or short to V_{DDQ})	1–4

Notes:
1. RZQI MR value, if supported, will be valid after the following sequence:
   - Completion of MPC[ZQCAL START] command to either channel
   - Completion of MPC[ZQCAL LATCH] command to either channel then ^{t}ZQLAT is satisfied

   RZQI value will be lost after reset.
2. If ZQ is connected to V_{SSQ} to set default calibration, OP[4:3] must be set to 01b. If ZQ is not connected to V_{SSQ}, either OP[4:3] = 01b or OP[4:3] = 10b might indicate a ZQ pin assembly error. It is recommended that the assembly error be corrected.
3. In the case of possible assembly error, the device will default to factory trim settings for R_{ON}, and will ignore ZQ CALIBRATION commands. In either case, the device may not function as intended.
4. If the ZQ pin self-test returns OP[4:3] = 11b, the device has detected a resistor connected to the ZQ pin. However, this result cannot be used to validate the ZQ resistor value or that the ZQ resistor meets the specified limits (that is, 240Ω ±1%).
5. See byte mode addendum spec for byte mode latency details.
6. Byte mode latency for 2Ch. x16 device is only allowed when it is stacked in a same package with byte mode device.

Table 4: MR1 Device Feature 1 (MA[5:0] = 01h)

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
RD-PST	*n*WR (for AP)			RD-PRE	WR-PRE	BL	

Table 5: MR1 Op-Code Bit Definitions

Feature	Type	OP	Definition	Notes
BL Burst length	Write-only	OP[1:0]	00b: BL = 16 sequential (default) 01b: BL = 32 sequential 10b: BL = 16 or 32 sequential (on-the-fly) 11b: Reserved	1
WR-PRE Write preamble length	Write-only	OP[2]	0b: Reserved 1b: WR preamble = 2 × ^{t}CK	5, 6
RD-PRE Read preamble type	Write-only	OP[3]	0b: RD preamble = Static (default) 1b: RD preamble = Toggle	3, 5, 6

Table 5: MR1 Op-Code Bit Definitions (Continued)

Feature	Type	OP	Definition	Notes
*n*WR Write-recovery for AUTO PRECHARGE command	Write-only	OP[6:4]	000b: *n*WR = 6 (default) 001b: *n*WR = 10 010b: *n*WR = 16 011b: *n*WR = 20 100b: *n*WR = 24 101b: *n*WR = 30 110b: *n*WR = 34 111b: *n*WR = 40	2, 5, 6
RD-PST Read postamble length	Write-only	OP[7]	0b: RD postamble = 0.5 × ^{t}CK (default) 1b: RD postamble = 1.5 × ^{t}CK	4, 5, 6

Notes:
1. Burst length on-the-fly can be set to either BL = 16 or BL = 32 by setting the BL bit in the command operands. See the Command Truth Table.
2. The programmed value of *n*WR is the number of clock cycles the device uses to determine the starting point of an internal precharge after a write burst with auto precharge (AP) enabled. See Frequency Ranges for RL, WL, and *n*WR Settings table.
3. For READ operations, this bit must be set to select between a toggling preamble and a non-toggling preamble (see the Preamble section).
4. OP[7] provides an optional read postamble with an additional rising and falling edge of DQS_t. The optional postamble cycle is provided for the benefit of certain memory controllers.
5. There are two physical registers assigned to each bit of this MR parameter: designated set point 0 and set point 1. Only the registers for the set point determined by the state of the FSP-WR bit (MR13 OP[6]) will be written to with an MRW command to this MR address.
6. There are two physical registers assigned to each bit of this MR parameter: designated set point 0 and set point 1. The device will operate only according to the values stored in the registers for the active set point, that is, the set point determined by the state of the FSP-OP bit (MR13 OP[7]). The values in the registers for the inactive set point will be ignored by the device and may be changed without affecting device operation.

Table 6: Burst Sequence for Read

C4	C3	C2	C1	C0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32
16-Bit READ Operation																																				
V	**0**	**0**	**0**	**0**	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F																
V	**0**	**1**	**0**	**0**	4	5	6	7	8	9	A	B	C	D	E	F	0	1	2	3																
V	**1**	**0**	**0**	**0**	8	9	A	B	C	D	E	F	0	1	2	3	4	5	6	7																
V	**1**	**1**	**0**	**0**	C	D	E	F	0	1	2	3	4	5	6	7	8	9	A	B																
32-Bit READ Operation																																				
0	**0**	**0**	**0**	**0**	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F	10	11	12	13	14	15	16	17	18	19	1A	1B	1C	1D	1E	1F
0	**0**	**1**	**0**	**0**	4	5	6	7	8	9	A	B	C	D	E	F	0	1	2	3	14	15	16	17	18	19	1A	1B	1C	1D	1E	1F	10	11	12	13
0	**1**	**0**	**0**	**0**	8	9	A	B	C	D	E	F	0	1	2	3	4	5	6	7	18	19	1A	1B	1C	1D	1E	1F	10	11	12	13	14	15	16	17
0	**1**	**1**	**0**	**0**	C	D	E	F	0	1	2	3	4	5	6	7	8	9	A	B	1C	1D	1E	1F	10	11	12	13	14	15	16	17	18	19	1A	1B
1	**0**	**0**	**0**	**0**	10	11	12	13	14	15	16	17	18	19	1A	1B	1C	1D	1E	1F	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
1	**0**	**1**	**0**	**0**	14	15	16	17	18	19	1A	1B	1C	1D	1E	1F	10	11	12	13	4	5	6	7	8	9	A	B	C	D	E	F	0	1	2	3
1	**1**	**0**	**0**	**0**	18	19	1A	1B	1C	1D	1E	1F	10	11	12	13	14	15	16	17	8	9	A	B	C	D	E	F	0	1	2	3	4	5	6	7
1	**1**	**1**	**0**	**0**	1C	1D	1E	1F	10	11	12	13	14	15	16	17	18	19	1A	1B	C	D	E	F	0	1	2	3	4	5	6	7	8	9	A	B

Notes:
1. C[1:0] are not present on the CA bus; they are implied to be zero.
2. The starting burst address is on 64-bit (4*n*) boundaries.

Table 7: Burst Sequence for Write

C4	C3	C2	C1	C0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32
16-Bit WRITE Operation																																				
V	**0**	**0**	**0**	**0**	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F																
32-Bit WRITE Operation																																				
0	**0**	**0**	**0**	**0**	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F	10	11	12	13	14	15	16	17	18	19	1A	1B	1C	1D	1E	1F

Notes:
1. C[1:0] are not present on the CA bus; they are implied to be zero.
2. The starting burst address is on 256-bit (16*n*) boundaries for burst length 16.
3. The starting burst address is on 512-bit (32*n*) boundaries for burst length 32.
4. C[3:2] must be set to 0 for all WRITE operations.

Table 8: MR2 Device Feature 2 (MA[5:0] = 02h)

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
WR Lev	WLS	WL			RL		

Table 9: MR2 Op-Code Bit Definitions

Feature	Type	OP	Definition	Notes
RL READ latency	Write-only	OP[2:0]	RL and *n*RTP for DBI-RD disabled (MR3 OP[6] = 0b) 000b: RL = 6, *n*RTP = 8 (default) 001b: RL = 10, *n*RTP = 8 010b: RL = 14, *n*RTP = 8 011b: RL = 20, *n*RTP = 8 100b: RL = 24, *n*RTP = 10 101b: RL = 28, *n*RTP = 12 110b: RL = 32, *n*RTP = 14 111b: RL = 36, *n*RTP = 16	1, 3, 4
			RL and *n*RTP for DBI-RD enabled (MR3 OP[6] = 1b) 000b: RL = 6, *n*RTP = 8 001b: RL = 12,*n*RTP = 8 010b: RL = 16, *n*RTP = 8 011b: RL = 22, *n*RTP = 8 100b: RL = 28, *n*RTP = 10 101b: RL = 32, *n*RTP = 12 110b: RL = 36, *n*RTP = 14 111b: RL = 40, *n*RTP = 16	

Table 9: MR2 Op-Code Bit Definitions (Continued)

Feature	Type	OP	Definition	Notes
WL WRITE latency	Write-only	OP[5:3]	WL set A (MR2 OP[6] = 0b) 000b: WL = 4 (default) 001b: WL = 6 010b: WL = 8 011b: WL = 10 100b: WL = 12 101b: WL = 14 110b: WL = 16 111b: WL = 18	1, 3, 4
			WL set B (MR2 OP[6] = 1b) 000b: WL = 4 001b: WL = 8 010b: WL = 12 011b: WL = 18 100b: WL = 22 101b: WL = 26 110b: WL = 30 111b: WL = 34	
WLS WRITE latency set	Write-only	OP[6]	0b: Use WL set A (default) 1b: Use WL set B	1, 3, 4
WR Lev Write leveling	Write-only	OP[7]	0b: Disable write leveling (default) 1b: Enable write leveling	2

Notes:
1. See Latency Code Frequency Table for allowable frequency ranges for RL/WL/*n*WR.
2. After an MRW command to set the write leveling enable bit (OP[7] = 1b), the device remains in the MRW state until another MRW command clears the bit (OP[7] = 0b). No other commands are allowed until the write leveling enable bit is cleared.
3. There are two physical registers assigned to each bit of this MR parameter: designated set point 0 and set point 1. Only the registers for the set point determined by the state of the FSP-WR bit (MR13 OP[6]) will be written to with an MRW command this MR address, or read from with an MRR command to this address.
4. There are two physical registers assigned to each bit of this MR parameter: designated set point 0 and set point 1. The device will operate only according to the values stored in the registers for the active set point, that is, the set point determined by the state of the FSP-OP bit (MR13 OP[7]). The values in the registers for the inactive set point will be ignored by the device and may be changed without affecting device operation.
5. *n*RTP is valid for BL16 only. For BL32, the SDRAM will add 8 clocks to the *n*RTP value before starting a precharge.

Table 10: Frequency Ranges for RL, WL, *n*WR, and *n*RTP Settings

READ Latency		WRITE Latency		*n*WR	*n*RTP	Lower Frequency Limit (>)	Upper Frequency Limit(≤)	Units	Notes
No DBI	w/DBI	Set A	Set B						
6	6	4	4	6	8	10	266	MHz	1–6
10	12	6	8	10	8	266	533		
14	16	8	12	16	8	533	800		
20	22	10	18	20	8	800	1066		
24	28	12	22	24	10	1066	1333		
28	32	14	26	30	12	1333	1600		
32	36	16	30	34	14	1600	1866		
36	40	18	34	40	16	1866	2133		

Notes:
1. The device should not be operated at a frequency above the upper frequency limit or below the lower frequency limit shown for each RL, WL, or *n*WR value.
2. DBI for READ operations is enabled in MR3 OP[6]. When MR3 OP[6] = 0, then the "No DBI" column should be used for READ latency. When MR3 OP[6] = 1, then the "w/DBI" column should be used for READ latency.
3. WRITE latency set A and set B are determined by MR2 OP[6]. When MR2 OP[6] = 0, then WRITE latency set A should be used. When MR2 OP[6] = 1, then WRITE latency set B should be used.
4. The programmed value for *n*RTP is the number of clock cycles the device uses to determine the starting point of an internal PRECHARGE operation after a READ burst with AP (auto precharge) enabled . It is determined by RU(^{t}RTP/^{t}CK).
5. The programmed value of *n*WR is the number of clock cycles the device uses to determine the starting point of an internal PRECHARGE operation after a WRITE burst with AP (auto precharge) enabled. It is determined by RU(^{t}WR/^{t}CK).
6. *n*RTP shown in this table is valid for BL16 only. For BL32, the device will add 8 clocks to the *n*RTP value before starting a precharge.

Table 11: MR3 I/O Configuration 1 (MA[5:0] = 03h)

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
DBI-WR	DBI-RD	PDDS			PPRP	WR-PST	PU-CAL

Table 12: MR3 Op-Code Bit Definitions

Feature	Type	OP	Definition	Notes
PU-CAL (Pull-up calibration point)	Write-only	OP[0]	0b: V_{DDQ} × 0.6	1–4
			1b: V_{DDQ} × 0.5 (default)	
WR-PST (WR postamble length)		OP[1]	0b: WR postamble = 0.5 × ^{t}CK (default)	2, 3, 5
			1b: WR postamble = 1.5 × ^{t}CK	
PPRP (Post-package repair protection)		OP[2]	0b: PPR protection disabled (default)	6
			1b: PPR protection enabled	
PDDS (Pull-down drive strength)		OP[5:3]	000b: RFU	1, 2, 3
			001b: R_{ZQ}/1	
			010b: R_{ZQ}/2	
			011b: R_{ZQ}/3	
			100b: R_{ZQ}/4	
			101b: R_{ZQ}/5	
			110b: R_{ZQ}/6 (default)	
			111b: Reserved	
DBI-RD (DBI-read enable)		OP[6]	0b: Disabled (default)	2, 3
			1b: Enabled	
DBI-WR (DBI-write enable)		OP[7]	0b: Disabled (default)	2, 3
			1b: Enabled	

Notes:
1. All values are typical. The actual value after calibration will be within the specified tolerance for a given voltage and temperature. Recalibration may be required as voltage and temperature vary.
2. There are two physical registers assigned to each bit of this MR parameter: designated set point 0 and set point 1. Only the registers for the set point determined by the state of the FSP-WR bit (MR13 OP[6]) will be written to with an MRW command to this MR address, or read from with an MRR command to this address.
3. There are two physical registers assigned to each bit of this MR parameter: designated set point 0 and set point 1.The device will operate only according to the values stored in the registers for the active set point, for example, the set point determined by the state of the FSP-OP bit (MR13 OP[7]). The values in the registers for the inactive set point will be determined by the state of the FSP-OP bit (MR13 OP[7]). The values in the registers for the inactive set point will be ignored by the device, and may be changed without affecting device operation.
4. For dual-channel device, PU-CAL (MR3-OP[0]) must be set the same for both channels on a die. The SDRAM will read the value of only one register (Ch.A or Ch.B); the choice is vendor-specific, so both channels must be set the same.
5. 1.5 × ^{t}CK apply > 1.6 GHz clock.
6. If MR3 OP[2] is set to 1b, PPR protection mode is enabled. The PPR protection bit is a sticky bit and can only be set to 0b by a power on reset. MR4 OP[4] controls entry to PPR mode. If PPR protection is enabled then the DRAM will not allow writing of 1b to MR4 OP[4].

Table 13: MR4 Device Temperature (MA[5:0] = 04h)

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
TUF	Thermal offset		PPRE	SR abort	Refresh rate		

Table 14: MR4 Op-Code Bit Definitions

Feature	Type	OP	Definition	Notes
Refresh rate	Read-only	OP[2:0]	000b: SDRAM low temperature operating limit exceeded 001b: 4x refresh 010b: 2x refresh 011b: 1x refresh (default) 100b: 0.5x refresh 101b: 0.25x refresh, no derating 110b: 0.25x refresh, with derating 111b: SDRAM high temperature operating limit exceeded	1–4, 7–9
SR abort (Self refresh abort)	Write	OP[3]	0b: Disable (default) 1b: Device dependent	9
PPRE (Post-package repair entry/exit)	Write	OP[4]	0b: Exit PPR mode (default) 1b: Enter PPR mode (Reference MR25 OP[7:0] for available PPR resources)	5, 9
Thermal offset-controller offset to TCSR	Write	OP[6:5]	00b: No offset, 0~5°C gradient (default) 01b: 5°C offset, 5~10°C gradient 10b: 10°C offset, 10~15°C gradient 11b: Reserved	9
TUF (Temperature update flag)	Read-only	OP7	0b: OP[2:0] No change in OP[2:0] since last MR4 read (default) 1b: Change in OP[2:0] since last MR4 read	6–8

Notes:
1. The refresh rate for each MR4 OP[2:0] setting applies to ^{t}REFI, ^{t}REFIpb, and ^{t}REFW. MR4 OP[2:0] = 011b corresponds to a device temperature of 85°C. Other values require either a longer (2x, 4x) refresh interval at lower temperatures or a shorter (0.5x, 0.25x) refresh interval at higher temperatures. If MR4 OP[2] = 1b, the device temperature is greater than 85°C.
2. At higher temperatures (>85°C), AC timing derating may be required. If derating is required the device will set MR4 OP[2:0] = 110b. See derating timing requirements in the AC Timing section.
3. DRAM vendors may or may not report all of the possible settings over the operating temperature range of the device. Each vendor guarantees that their device will work at any temperature within the range using the refresh interval requested by their device.
4. The device may not operate properly when MR4 OP[2:0] = 000b or 111b.
5. Post-package repair can be entered or exited by writing to MR4 OP[4].
6. When MR4 OP[7] = 1b, the refresh rate reported in MR4 OP[2:0] has changed since the last MR4 read. A mode register read from MR4 will reset MR4 OP[7] to 0b.

7. MR4 OP[7] = 0b at power-up. MR4 OP[2:0] bits are valid after initialization sequence (Te).
8. See the Temperature Sensor section for information on the recommended frequency of reading MR4.
9. MR4 OP[6:3] can be written in this register. All other bits will be ignored by the device during an MRW command to this register.

Table 15: MR5 Basic Configuration 1 (MA[5:0] = 05h)

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
Manufacturer ID							

Table 16: MR5 Op-Code Bit Definitions

Feature	Type	OP	Definition
Manufacturer ID	Read-only	OP[7:0]	1111 1111b : Micron All others: Reserved

Table 17: MR6 Basic Configuration 2 (MA[5:0] = 06h)

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
Revision ID1							

Note: 1. MR6 is vendor-specific.

Table 18: MR6 Op-Code Bit Definitions

Feature	Type	OP	Definition
Revision ID1	Read-only	OP[7:0]	xxxx xxxxb: Revision ID1

Note: 1. MR6 is vendor-specific.

Table 19: MR7 Basic Configuration 3 (MA[5:0] = 07h)

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
Revision ID2							

Table 20: MR7 Op-Code Bit Definitions

Feature	Type	OP	Definition
Revision ID2	Read-only	OP[7:0]	xxxx xxxxb: Revision ID2

Note: 1. MR7 is vendor-specific.

Table 21: MR8 Basic Configuration 4 (MA[5:0] = 08h)

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
I/O width		Density				Type	

Table 22: MR8 Op-Code Bit Definitions

Feature	Type	OP	Definition
Type	Read-only	OP[1:0]	00b: S16 SDRAM (16*n* prefetch) All others: Reserved
Density	Read-only	OP[5:2]	0000b: 4Gb dual-channel die/2Gb single-channel die 0001b: 6Gb dual-channel die/3Gb single-channel die 0010b: 8Gb dual-channel die/4Gb single-channel die 0011b: 12Gb dual-channel die/6Gb single-channel die 0100b: 16Gb dual-channel die/8Gb single-channel die 0101b: 24Gb dual-channel die/12Gb single-channel die 0110b: 32Gb dual-channel die/16Gb single-channel die 1100b: 2Gb dual-channel die/1Gb single-channel die All others: Reserved
I/O width	Read-only	OP[7:6]	00b: x16/channel 01b: x8/channel All others: Reserved

Table 23: MR9 Test Mode (MA[5:0] = 09h)

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
Vendor-specific test mode							

Table 24: MR9 Op-Code Definitions

Feature	Type	OP	Definition
Test mode	Write-only	OP[7:0]	0000000b; Vendor-specific test mode disabled (default)

Table 25: MR10 Calibration (MA[5:0] = 0Ah)

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
RFU							ZQ RESET

Table 26: MR10 Op-Code Bit Definitions

Feature	Type	OP	Definition
ZQ reset	Write-only	OP[0]	0b: Normal operation (default) 1b: ZQ reset

Notes:
1. See AC Timing table for calibration latency and timing.
2. If ZQ is connected to V_{DDQ} through R_{ZQ}, either the ZQ CALIBRATION function or default calibration (via ZQ reset) is supported. If ZQ is connected to V_{SS}, the device operates with default calibration and ZQ CALIBRATION commands are ignored. In both cases, the ZQ connection must not change after power is supplied to the device.

Table 27: MR11 ODT Control (MA[5:0] = 0Bh)

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
RFU	CA ODT			RFU	DQ ODT		

Table 28: MR11 Op-Code Bit Definitions

Feature	Type	OP	Definition	Notes
DQ ODT DQ bus receiver on-die termination	Write-only	OP[2:0]	000b: Disable (default) 001b: RZQ/1 010b: RZQ/2 011b: RZQ/3 100b: RZQ/4 101b: RZQ/5 110b: RZQ/6 111b: RFU	1, 2, 3
CA ODT CA bus receiver on-die termination	Write-only	OP[6:4]	000b: Disable (default) 001b: RZQ/1 010b: RZQ/2 011b: RZQ/3 100b: RZQ/4 101b: RZQ/5 110b: RZQ/6 111b: RFU	1, 2, 3

Notes:
1. All values are typical. The actual value after calibration will be within the specified tolerance for a given voltage and temperature. Re-calibration may be required as voltage and temperature vary.
2. There are two physical registers assigned to each bit of this MR parameter: designated set point 0 and set point 1. Only the registers for the set point determined by the state of the FSP-WR bit (MR13 OP[6]) will be written to with an MRW command to this MR address, or read from with an MRR command to this address.
3. There are two physical registers assigned to each bit of this MR parameter: designated set point 0 and set point 1. The device will operate only according to the values stored

in the registers for the active set point, for example, the set point determined by the state of the FSP-OP bit (MR13 OP[7]). The values in the registers for the inactive set point will be ignored by the device and may be changed without affecting device operation.

Table 29: MR12 Register Information (MA[5:0] = 0Ch)

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
RFU	VR_{CA}	$V_{REF(CA)}$					

Table 30: MR12 Op-Code Bit Definitions

Feature	Type	OP	Data	Notes
$V_{REF(CA)}$ $V_{REF(CA)}$ settings	Read/ Write	OP[5:0]	000000b–110010b: See V_{REF} Settings table All others: Reserved	1–3, 5, 6
VR_{CA} $V_{REF(CA)}$ range	Read/ Write	OP[6]	0b: $V_{REF(CA)}$ range[0] enabled 1b: $V_{REF(CA)}$ range[1] enabled (default)	1, 2, 4, 5, 6

Notes:
1. This register controls the $V_{REF(CA)}$ levels for frequency set point[1:0]. Values from either VR(ca)[0] or VR(ca)[1] may be selected by setting MR12 OP[6] appropriately.
2. A read to MR12 places the contents of OP[7:0] on DQ[7:0]. Any RFU bits and unused DQ will be set to 0. See the MRR Operation section.
3. A write to MR12 OP[5:0] sets the internal $V_{REF(CA)}$ level for FSP[0] when MR13 OP[6] = 0b or sets the internal $V_{REF(CA)}$ level for FSP[1] when MR13 OP[6] = 1b. The time required for $V_{REF(CA)}$ to reach the set level depends on the step size from the current level to the new level. See the $V_{REF(CA)}$ training section.
4. A write to MR12 OP[6] switches the device between two internal $V_{REF(CA)}$ ranges. The range (range[0] or range[1]) must be selected when setting the $V_{REF(CA)}$ register. The value, once set, will be retained until overwritten or until the next power-on or reset event.
5. There are two physical registers assigned to each bit of this MR parameter: designated set point 0 and set point 1. Only the registers for the set point determined by the state of the FSP-WR bit (MR13 OP[6]) will be written to with an MRW command to this MR address, or read from with an MRR command to this address.
6. There are two physical registers assigned to each bit of this MR parameter: designated set point 0 and set point 1. The device will operate only according to the values stored in the registers for the active set point, for example, the set point determined by the state of the FSP-OP bit (MR13 OP[7]). The values in the registers for the inactive set point will be ignored by the device, and may be changed without affecting device operation.

Table 31: MR13 Register Control (MA[5:0] = 0Dh)

OP[7]	OP[6]	OP[5]	OP[4]	OP[3]	OP[2]	OP[1]	OP[0]
FSP-OP	FSP-WR	DMD	RRO	VRCG	VRO	RPT	CBT

Table 32: MR13 Op-Code Bit Definition

Feature	Type	OP	Definition	Notes
CBT Command bus training	Write-only	OP[0]	0b: Normal operation (default) 1b: Command bus training mode enabled	1
RPT Read preamble training		OP[1]	0b: Disabled (default) 1b: Read preamble training mode enabled	
VRO V_{REF} output		OP[2]	0b: Normal operation (default) 1b: Output the $V_{REF(CA)}$ and $V_{REF(DQ)}$ values on DQ bits	2
VRCG V_{REF} current generator		OP[3]	0b: Normal operation (default) 1b: Fast response (high current) mode	3
RRO Refresh rate option		OP[4]	0b: Disable codes 001 and 010 in MR4 OP[2:0] 1b: Enable all codes in MR4 OP[2:0]	4, 5
DMD Data mask disable		OP[5]	0b: DATA MASK operation enabled (default) 1b: DATA MASK operation disabled	6
FSP-WR Frequency set point write/ read		OP[6]	0b: Frequency set point[0] (default) 1b: Frequency set point[1]	7
FSP-OP FREQUENCY SET POINT operation mode		OP[7]	0b: Frequency set point[0] (default) 1b: Frequency set point[1]	8

Notes:
1. A write to set OP[0] = 1 causes the LPDDR4 SDRAM to enter the command bus training mode. When OP[0] = 1 and CKE goes LOW, commands are ignored and the contents of CA[5:0] are mapped to the DQ bus. CKE must be brought HIGH before doing a MRW to clear this bit (OP[0] = 0) and return to normal operation. See the Command Bus Training section for more information.
2. When set, the device will output the $V_{REF(CA)}$ and $V_{REF(DQ)}$ voltage on DQ pins. Only the "active" frequency set point, as defined by MR13 OP[7], will be output on the DQ pins. This function allows an external test system to measure the internal V_{REF} levels. The DQ pins used for V_{REF} output are vendor-specific.
3. When OP[3] = 1, the V_{REF} circuit uses a high current mode to improve V_{REF} settling time.
4. MR13 OP[4] RRO bit is valid only when MR0 OP[0] = 1. For LPDDR4 SDRAM with MR0 OP[0] = 0, MR4 OP[2:0] bits are not dependent on MR13 OP[4].
5. When OP[4] = 0, only 001b and 010b in MR4 OP[2:0] are disabled. LPDDR4 SDRAM must report 011b instead of 001b or 010b in this case. Controller should follow the refresh mode reported by MR4 OP[2:0], regardless of RRO setting. TCSR function does not depend on RRO setting.
6. When enabled (OP[5] = 0b) data masking is enabled for the device. When disabled (OP[5] = 1b), the device will ignore any mask patterns issued during a MASKED WRITE command. See the Data Mask section for more information.
7. FSP-WR determines which frequency set point registers are accessed with MRW and MRR commands for the following functions such as $V_{REF(CA)}$ setting, $V_{REF(CA)}$ range, $V_{REF(DQ)}$ setting, $V_{REF(DQ)}$ range. For more information, refer to Frequency Set Point section.
8. FSP-OP determines which frequency set point register values are currently used to specify device operation for the following functions such as $V_{REF(CA)}$ setting, $V_{REF(CA)}$ range, $V_{REF(DQ)}$ setting, $V_{REF(DQ)}$ range. For more information, refer to Frequency Set Point section.

Table 33: Mode Register 14 (MA[5:0] = 0Eh)

OP[7]	OP[6]	OP[5]	OP[4]	OP[3]	OP[2]	OP[1]	OP[0]
RFU	VR_{DQ}	$V_{REF(DQ)}$					

Table 34: MR14 Op-Code Bit Definition

Feature	Type	OP	Definition	Notes
$V_{REF(DQ)}$ $V_{REF(DQ)}$ setting	Read/ Write	OP[5:0]	000000b–110010b: See V_{REF} Settings table All others: Reserved	1–3, 5, 6
VR_{DQ} $V_{REF(DQ)}$ range		OP[6]	0b: $V_{REF(DQ)}$ range[0] enabled 1b: $V_{REF(DQ)}$ range[1] enabled (default)	1, 2, 4–6

Notes:
1. This register controls the $V_{REF(DQ)}$ levels for frequency set point[1:0]. Values from either VR_{DQ}[0] (vendor defined) or VR_{DQ}[1] (vendor defined) may be selected by setting OP[6] appropriately.
2. A read (MRR) to this register places the contents of OP[7:0] on DQ[7:0]. Any RFU bits and unused DQ shall be set to 0. See the MRR Operation section.
3. A write to OP[5:0] sets the internal $V_{REF(DQ)}$ level for FSP[0] when MR13 OP[6] = 0b, or sets FSP[1] when MR13 OP[6] = 1b. The time required for $V_{REF(DQ)}$ to reach the set level depends on the step size from the current level to the new level. See the $V_{REF(DQ)}$ training section.
4. A write to OP[6] switches the device between two internal $V_{REF(DQ)}$ ranges. The range (range[0] or range[1]) must be selected when setting the $V_{REF(DQ)}$ register. The value, once set, will be retained until overwritten, or until the next power-on or reset event.
5. There are two physical registers assigned to each bit of this MR parameter: designated set point 0 and set point 1. Only the registers for the set point determined by the state of the FSP-WR bit (MR13 OP[6]) will be written to with an MRW command to this MR address, or read from with an MRR command to this address.
6. There are two physical registers assigned to each bit of this MR parameter: designated set point 0 and set point 1. The device will operate only according to the values stored in the registers for the active set point, for example, the set point determined by the state of the FSP-OP bit (MR13 OP[7]). The values in the registers for the inactive set point will be ignored by the device, and may be changed without affecting device operation.

Table 35: V_{REF} Setting for Range[0] and Range[1]

Notes 1-3 apply to entire table

Function	OP	Range[0] Values		Range[1] Values	
		$V_{REF(CA)}$ (% of V_{DDQ}) $V_{REF(DQ)}$ (% of V_{DDQ})		$V_{REF(CA)}$ (% of V_{DDQ}) $V_{REF(DQ)}$ (% of V_{DDQ})	
V_{REF} setting for MR12 and MR14	OP[5:0]	000000b: 15.0%	011010b: 30.5%	000000b: 32.9%	011010b: 48.5%
		000001b: 15.6%	011011b: 31.1%	000001b: 33.5%	011011b: 49.1%
		000010b: 16.2%	011100b: 31.7%	000010b: 34.1%	011100b: 49.7%
		000011b: 16.8%	011101b: 32.3%	000011b: 34.7%	011101b: 50.3% (default)
		000100b: 17.4%	011110b: 32.9%	000100b: 35.3%	011110b: 50.9%
		000101b: 18.0%	011111b: 33.5%	000101b: 35.9%	011111b: 51.5%
		000110b: 18.6%	100000b: 34.1%	000110b: 36.5%	100000b: 52.1%
		000111b: 19.2%	100001b: 34.7%	000111b: 37.1%	100001b: 52.7%
		001000b: 19.8%	100010b: 35.3%	001000b: 37.7%	100010b: 53.3%
		001001b: 20.4%	100011b: 35.9%	001001b: 38.3%	100011b: 53.9%
		001010b: 21.0%	100100b: 36.5%	001010b: 38.9%	100100b: 54.5%
		001011b: 21.6%	100101b: 37.1%	001011b: 39.5%	100101b: 55.1%
		001100b: 22.2%	100110b: 37.7%	001100b: 40.1%	100110b: 55.7%
		001101b: 22.8%	100111b: 38.3%	001101b: 40.7%	100111b: 56.3%
		001110b: 23.4%	101000b: 38.9%	001110b: 41.3%	101000b: 56.9%
		001111b: 24.0%	101001b: 39.5%	001111b: 41.9%	101001b: 57.5%
		010000b: 24.6%	101010b: 40.1%	010000b: 42.5%	101010b: 58.1%
		010001b: 25.1%	101011b: 40.7%	010001b: 43.1%	101011b: 58.7%
		010010b: 25.7%	101100b: 41.3%	010010b: 43.7%	101100b: 59.3%
		010011b: 26.3%	101101b: 41.9%	010011b: 44.3%	101101b: 59.9%
		010100b: 26.9%	101110b: 42.5%	010100b: 44.9%	101110b: 60.5%
		010101b: 27.5%	101111b: 43.1%	010101b: 45.5%	101111b: 61.1%
		010110b: 28.1%	110000b: 43.7%	010110b: 46.1%	110000b: 61.7%
		010111b: 28.7%	110001b: 44.3%	010111b: 46.7%	110001b: 62.3%
		011000b: 29.3%	110010b: 44.9%	011000b: 47.3%	110010b: 62.9%
		011001b: 29.9%	All others: Reserved	011001b: 47.9%	All others: Reserved

Notes:
1. These values may be used for MR14 OP[5:0] and MR12 OP[5:0] to set the $V_{REF(CA)}$ or $V_{REF(DQ)}$ levels in the device.
2. The range may be selected in each of the MR14 or MR12 registers by setting OP[6] appropriately.
3. Each of the MR14 or MR12 registers represents either FSP[0] or FSP[1]. Two frequency set points each for CA and DQ are provided to allow for faster switching between terminated and unterminated operation or between different high-frequency settings, which may use different terminations values.

Table 36: MR15 Register Information (MA[5:0] = 0Fh)

OP[7]	OP[6]	OP[5]	OP[4]	OP[3]	OP[2]	OP[1]	OP[0]
Lower-byte invert register for DQ calibration							

Table 37: MR15 Op-code Bit Definition

Feature	Type	OP	Definition	Notes
Lower-byte invert for DQ calibration	Write-only	OP[7:0]	The following values may be written for any operand OP[7:0] and will be applied to the corresponding DQ locations DQ[7:0] within a byte lane 0b: Do not invert 1b: Invert the DQ calibration patterns in MR32 and MR40 Default value for OP[7:0] = 55h	1–3

Notes:
1. This register will invert the DQ calibration pattern found in MR32 and MR40 for any single DQ or any combination of DQ. Example: If MR15 OP[7:0] = 00010101b, then the DQ calibration patterns transmitted on DQ[7, 6, 5, 3, 1] will not be inverted, but the DQ calibration patterns transmitted on DQ[4, 2, 0] will be inverted.
2. DM[0] is not inverted and always transmits the "true" data contained in MR32 and MR40.
3. No DATA BUS INVERSION (DBI) function is enacted during read DQ calibration, even if DBI is enabled in MR3-OP[6].

Table 38: MR15 Invert Register Pin Mapping

PIN	DQ0	DQ1	DQ2	DQ3	DMIO	DQ4	DQ5	DQ6	DQ7
MR15	OP0	OP1	OP2	OP3	No invert	OP4	OP5	OP6	OP7

Table 39: MR16 PASR Bank Mask (MA[5:0] = 010h)

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
PASR bank mask							

Table 40: MR16 Op-Code Bit Definitions

Feature	Type	OP	Definition
Bank[7:0] mask	Write-only	OP[7:0]	0b: Bank refresh enabled (default) 1b: Bank refresh disabled

OP[n]	Bank Mask	8-Bank SDRAM
0	xxxxxxx1	Bank 0
1	xxxxxx1x	Bank 1
2	xxxxx1xx	Bank 2

OP[n]	Bank Mask	8-Bank SDRAM
3	xxxx1xxx	Bank 3
4	xxx1xxxx	Bank 4
5	xx1xxxxx	Bank 5
6	x1xxxxxx	Bank 6
7	1xxxxxxx	Bank 7

Notes: 1. When a mask bit is asserted (OP[*n*] = 1), refresh to that bank is disabled.
2. PASR bank masking is on a per-channel basis; the two channels on the die may have different bank masking in dual-channel devices.

Table 41: MR17 PASR Segment Mask (MA[5:0] = 11h)

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
PASR segment mask							

Table 42: MR17 PASR Segment Mask Definitions

Feature	Type	OP	Definition
Segment[7:0] mask	Write-only	OP[7:0]	0b: Segment refresh enabled (default) 1b: Segment refresh disabled

Table 43: MR17 PASR Segment Mask

Segment	OP	Segment Mask	Density (per channel)							
			1Gb	2Gb	3Gb	4Gb	6Gb	8Gb	12Gb	16Gb
			R[12:10]	R[13:11]	R[14:12]	R[14:12]	R[15:13]	R[15:13]	R[16:14]	R[16:14]
0	0	XXXXXXX1	000b							
1	1	XXXXXX1X	001b							
2	2	XXXXX1XX	010b							
3	3	XXXX1XXX	011b							
4	4	XXX1XXXX	100b							
5	5	XX1XXXXX	101b							
6	6	X1XXXXXX	110b	110b	Not allowed	110b	Not allowed	110b	Not allowed	110b
7	7	1XXXXXXX	111b	111b		111b		111b		111b

Notes: 1. This table indicates the range of row addresses in each masked segment. "X" is “Don’t Care” for a particular segment.
2. PASR segment-masking is on a per-channel basis. The two channels on the die may have different segment masking in dual-channel devices.
3. For 3Gb, 6Gb, and 12Gb density per channel, OP[7:6] must always be LOW (= 00b).

Table 44: MR18 Register Information (MA[5:0] = 12h)

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
DQS oscillator count - LSB							

Table 45: MR18 LSB DQS Oscillator Count

Notes 1–3 apply to entire table

Function	Type	OP	Definition
DQS oscillator count (WR training DQS oscillator)	Read-only	OP[7:0]	0h–FFh LSB DRAM DQS oscillator count

Notes:
1. MR18 reports the LSB bits of the DRAM DQS oscillator count. The DRAM DQS oscillator count value is used to train DQS to the DQ data valid window. The value reported by the DRAM in this mode register can be used by the memory controller to periodically adjust the phase of DQS relative to DQ.
2. Both MR18 and MR19 must be read (MRR) and combined to get the value of the DQS oscillator count.
3. The value in this register is reset each time an MPC command is issued to start in the DQS oscillator counter.

Table 46: MR19 Register Information (MA[5:0] = 13h)

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
DQS oscillator count – MSB							

Table 47: MR19 DQS Oscillator Count

Notes 1–3 apply to the entire table

Function	Type	OP	Definition
DQS oscillator count – MSB (WR training DQS oscillator)	Read-only	OP[7:0]	0h–FFh MSB DRAM DQS oscillator count

Notes:
1. MR19 reports the MSB bits of the DRAM DQS oscillator count. The DRAM DQS oscillator count value is used to train DQS to the DQ data valid window. The value reported by the DRAM in this mode register can be used by the memory controller to periodically adjust the phase of DQS relative to DQ.
2. Both MR18 and MR19 must be read (MRR) and combined to get the value of the DQS oscillator count.
3. A new MPC[START DQS OSCILLATOR] should be issued to reset the contents of MR18/ MR19.

Table 48: MR20 Register Information (MA[5:0] = 14h)

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
Upper-byte invert register for DQ calibration							

Table 49: MR20 Register Information

Notes 1–3 apply to entire table

Function	Type	OP	Definition
Upper-byte invert for DQ calibration	Write-only	OP[7:0]	The following values may be written for any operand OP[7:0] and will be applied to the corresponding DQ locations DQ[15:8] within a byte lane 0b: Do not invert 1b: Invert the DQ calibration patterns in MR32 and MR40 Default value for OP[7:0] = 55h

Notes:
1. This register will invert the DQ calibration pattern found in MR32 and MR40 for any single DQ or any combination of DQ. For example, if MR20 OP[7:0] = 00010101b, the DQ calibration patterns transmitted on DQ[15, 14, 13, 11, 9] will not be inverted, but the DQ calibration patterns transmitted on DQ[12, 10, 8] will be inverted.
2. DM[1] is not inverted and always transmits the true data contained in MR32 and MR40.
3. No DATA BUS INVERSION (DBI) function is enacted during read DQ calibration, even if DBI is enabled in MR3 OP[6].

Table 50: MR20 Invert Register Pin Mapping

Pin	DQ8	DQ9	DQ10	DQ11	DMI1	DQ12	DQ13	DQ14	DQ15
MR20	OP0	OP1	OP2	OP3	No invert	OP4	OP5	OP6	OP7

Table 51: MR21 Register Information (MA[5:0] = 15h)

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
RFU							

Table 52: MR22 Register Information (MA[5:0] = 16h)

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
ODTD for x8_2ch		ODTD-CA	ODTE-CS	ODTE-CK	SOC ODT		

Table 53: MR22 Register Information

Function	Type	OP	Data	Notes
SOC ODT (controller ODT value for V_{OH} calibration)	Write-only	OP[2:0]	000b: Disable (default) 001b: R_{ZQ}/1 (Illegal if MR3 OP[0] = 0b) 010b: R_{ZQ}/2 011b: R_{ZQ}/3 (Illegal if MR3 OP[0] = 0b) 100b: R_{ZQ}/4 101b: R_{ZQ}/5 (Illegal if MR3 OP[0] = 0b) 110b: R_{ZQ}/6 (Illegal if MR3 OP[0] = 0b) 111b: RFU	1, 2, 3
ODTE-CK (CK ODT enabled for non-terminating rank)	Write-only	OP[3]	ODT bond PAD is ignored 0b: ODT-CK enable (default) 1b: ODT-CK disable	2, 3
ODTE-CS (CS ODT enabled for non-terminating rank)	Write-only	OP[4]	ODT bond PAD is ignored 0b: ODT-CS enable (default) 1b: ODT-CS disable	2, 3
ODTD-CA (CA ODT termination disable)	Write-only	OP[5]	ODT bond PAD is ignored 0b: CA ODT enable (default) 1b: CA ODT disable	2, 3
ODTD for x8_2ch (Byte) mode	Write-only	OP[7:6]	See Byte Mode section	

Notes:
1. All values are typical.
2. There are two physical registers assigned to each bit of this MR parameter: designated set point 0 and set point 1. Only the registers for the set point determined by the state of the FSP-WR bit (MR13 OP[6]) will be written to with an MRW command to this MR address, or read from with an MRR command to this address.
3. There are two physical registers assigned to each bit of this MR parameter: designated set point 0 and set point 1. The device will operate only according to the values stored in the registers for the active set point, for example, the set point determined by the state of the FSP-OP bit (MR13 OP[7]). The values in the registers for the inactive set point will be ignored by the device, and may be changed without affecting device operation.

Table 54: MR23 Register Information (MA[5:0] = 17h)

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
DQS interval timer run-time setting							

Table 55: MR23 Register Information

Notes 1–2 apply to entire table

Function	Type	OP	Data
DQS interval timer run-time	Write-only	OP[7:0]	00000000b: Disabled (default) 00000001b: DQS timer stops automatically at the 16th clock after timer start 00000010b: DQS timer stops automatically at the 32nd clock after timer start 00000011b: DQS timer stops automatically at the 48th clock after timer start 00000100b: DQS timer stops automatically at the 64th clock after timer start --------- Through --------- 00111111b: DQS timer stops automatically at the (63 × 16)th clock after timer start 01XXXXXXb: DQS timer stops automatically at the 2048th clock after timer start 10XXXXXXb: DQS timer stops automatically at the 4096th clock after timer start 11XXXXXXb: DQS timer stops automatically at the 8192nd clock after timer start

Notes:
1. MPC command with OP[6:0] = 1001101b (STOP DQS INTERVAL OSCILLATOR) stops the DQS interval timer in the case of MR23 OP[7:0] = 00000000b.
2. MPC command with OP[6:0] = 1001101b (STOP DQS INTERVAL OSCILLATOR) is illegal with valid nonzero values in MR23 OP[7:0].

Table 56: MR24 Register Information (MA[5:0] = 18h)

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
TRR mode	TRR mode BAn			Unlimited MAC	MAC value		

Table 57: MR24 Register Information

Function	Type	OP	Data	Notes
MAC value	Read	OP[2:0]	000b: Unknown (OP[3] = 0) or unlimited (OP[3] = 1) 001b: 700K 010b: 600K 011b: 500K 100b: 400K 101b: 300K 110b: 200K 111b: Reserved	1

Table 57: MR24 Register Information (Continued)

Function	Type	OP	Data	Notes
Unlimited MAC	Read	OP[3]	0b: OP[2:0] defines the MAC value 1b: Unlimited MAC value	2
TRR mode BAn	Write	OP[6:4]	000b: Bank 0 001b: Bank 1 010b: Bank 2 011b: Bank 3 100b: Bank 4 101b: Bank 5 110b: Bank 6 111b: Bank 7	
TRR mode	Write	OP[7]	0b: Disabled (default) 1b: Enabled	

Notes:
1. OP[2:0] = 000b Unknown means that the device is not tested for ^{t}MAC and pass/fail values are unknown. OP[2:0] = 000b Unlimited means that there is no restriction on the number of activates between refresh windows. However, specific attempts to by-pass TRR may result in data disturb.
2. When OP[3] = 1b, MR24 OP[2:0] set to 000b.

Table 58: MR25 Register Information (MA[5:0] = 19h)

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
Bank 7	Bank 6	Bank 5	Bank 4	Bank 3	Bank 2	Bank 1	Bank 0

Table 59: MR25 Register Information

Function	Type	OP	Data
PPR resources	Read-only	OP[7:0]	0b: PPR resource is not available 1b: PPR resource is available

Note:
1. When OP[*n*] = 0, there is no PPR resource available for that bank. When OP[*n*] = 1, there is a PPR resource available for that bank, and PPR can be initiated by the controller.

Table 60: MR26:29 Register Information (MA[5:0] = 1Ah–1Dh)

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
Reserved for future use							

Table 61: MR30 Register Information (MA[5:0] = 1Eh)

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
Valid 0 or 1							

Table 62: MR30 Register Information

Function	Type	OP	Data
SDRAM will ignore	Write-only	OP[7:0]	Don't care

Note: 1. This register is reserved for testing purposes. The logical data values written to OP[7:0] will have no effect on SDRAM operation; however, timings need to be observed as for any other MR access command.

Table 63: MR31 Register Information (MA[5:0] = 1Fh)

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
Reserved for future use							

Table 64: MR32 Register Information (MA[5:0] = 20h)

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
DQ calibration pattern A (default = 5Ah)							

Table 65: MR32 Register Information

Feature	Type	OP	Data	Notes
Return DQ calibration pattern MR32 + MR40	Write-only	OP[7:0]	Xb: An MPC command issued with OP[6:0] = 1000011b causes the device to return the DQ calibration pattern contained in this register and (followed by) the contents of MR40. A default pattern 5Ah is loaded at power-up or reset, or the pattern may be overwritten with a MRW to this register. The contents of MR15 and MR20 will invert the MR32/MR40 data pattern for a given DQ (see MR15/MR20 for more information).	1, 2, 3

Notes: 1. The patterns contained in MR32 and MR40 are transmitted on DQ[15:0] and DMI[1:0] when read DQ calibration is initiated via an MPC command. The pattern is transmitted serially on each data lane and organized little endian such that the low-order bit in a byte is transmitted first. If the data pattern is 27H, the first bit transmitted is a 1 followed by 1, 1, 0, 0, 1, 0, and 0. The bit stream will be 00100111.
2. MR15 and MR20 may be used to invert the MR32/MR40 data pattern on the DQ pins. See MR15 and MR20 for more information. Data is never inverted on the DMI[1:0] pins.
3. The data pattern is not transmitted on the DMI[1:0] pins if DBI-RD is disabled via MR3 OP[6].

4. No DATA BUS INVERSION (DBI) function is enacted during read DQ calibration, even if DBI is enabled in MR3 OP[6].

Table 66: MR33:38 Register Information (MA[5:0] = 21h–26h)

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
Do not use							

Table 67: MR39 Register Information (MA[5:0] = 27h)

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
Valid 0 or 1							

Table 68: MR39 Register Information

Function	Type	OP	Data
SDRAM will ignore	Write-only	OP[7:0]	Don't care

Note: 1. This register is reserved for testing purposes. The logical data values written to OP[7:0] will have no effect on SDRAM operation; however, timings need to be observed as for any other MR access command.

Table 69: MR40 Register Information (MA[5:0] = 28h)

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
DQ calibration pattern B (default = 3Ch)							

Table 70: MR40 Register Information

Function	Type	OP	Data	Notes
Return DQ calibration pattern MR32 + MR40	Write-only	OP[7:0]	Xb: A default pattern 3Ch is loaded at power-up or reset, or the pattern may be overwritten with a MRW to this register. See MR32 for more information.	1, 2, 3

Notes:
1. The pattern contained in MR40 is concatenated to the end of MR32 and transmitted on DQ[15:0] and DMI[1:0] when read DQ calibration is initiated via an MPC command. The pattern is transmitted serially on each data lane and organized little endian such that the low-order bit in a byte is transmitted first. If the data pattern in MR40 is 27H, the first bit transmitted will be a 1, followed by 1, 1, 0, 0, 1, 0, and 0. The bit stream will be 00100111.
2. MR15 and MR20 may be used to invert the MR32/MR40 data patterns on the DQ pins. See MR15 and MR20 for more information. Data is never inverted on the DMI[1:0] pins.
3. The data pattern is not transmitted on the DMI[1:0] pins if DBI-RD is disabled via MR3 OP[6].
4. No DATA BUS INVERSION (DBI) function is enacted during read DQ calibration, even if DBI is enabled in MR3 OP[6].

Table 71: MR41:47 Register Information (MA[5:0] = 29h–2Fh)

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
Do not use							

Table 72: MR48:63 Register Information (MA[5:0] = 30h–3Fh)

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
Reserved for future use							

5. I_{DD} Specifications

Table 1: I_{DD} Specifications – Single-Die (T_C = –30°C to +85°C)

V_{DD2}, V_{DDQ} = 1.06–1.17V; V_{DD1} = 1.70–1.95V

Parameter	Supply	Speed Grade	Unit	Note
		3200 Mbps		
I_{DD01}	V_{DD1}	4.1	mA	
I_{DD02}	V_{DD2}	72		
I_{DD0Q}	V_{DDQ}	0.72		
I_{DD2P1}	V_{DD1}	0.54	mA	
I_{DD2P2}	V_{DD2}	4.3		
I_{DD2PQ}	V_{DDQ}	0.4		
I_{DD2PS1}	V_{DD1}	0.54	mA	
I_{DD2PS2}	V_{DD2}	4.35		
I_{DD2PSQ}	V_{DDQ}	0.4		
I_{DD2N1}	V_{DD1}	0.65	mA	
I_{DD2N2}	V_{DD2}	41.5		
I_{DD2NQ}	V_{DDQ}	1		
I_{DD2NS1}	V_{DD1}	0.65	mA	
I_{DD2NS2}	V_{DD2}	37		
I_{DD2NSQ}	V_{DDQ}	1		
I_{DD3P1}	V_{DD1}	0.8	mA	
I_{DD3P2}	V_{DD2}	16.5		
I_{DD3PQ}	V_{DDQ}	0.4		
I_{DD3PS1}	V_{DD1}	0.8	mA	
I_{DD3PS2}	V_{DD2}	16.5		
I_{DD3PSQ}	V_{DDQ}	0.4		
I_{DD3N1}	V_{DD1}	1.3	mA	
I_{DD3N2}	V_{DD2}	51.5		
I_{DD3NQ}	V_{DDQ}	1		
I_{DD3NS1}	V_{DD1}	1.3	mA	
I_{DD3NS2}	V_{DD2}	47		
I_{DD3NSQ}	V_{DDQ}	1		
I_{DD4R1}	V_{DD1}	2.2	mA	3
I_{DD4R2}	V_{DD2}	420		
I_{DD4RQ}	V_{DDQ}	285		
I_{DD4W1}	V_{DD1}	2.2	mA	
I_{DD4W2}	V_{DD2}	355		
I_{DD4WQ}	V_{DDQ}	102		

Table 1: I_{DD} Specifications – Single-Die (T_C = –30°C to +85°C) (Continued)

V_{DD2}, V_{DDQ} = 1.06–1.17V; V_{DD1} = 1.70–1.95V

Parameter	Supply	Speed Grade	Unit	Note
		3200 Mbps		
I_{DD51}	V_{DD1}	14.5	mA	
I_{DD52}	V_{DD2}	100		
I_{DD5Q}	V_{DDQ}	0.95		
I_{DD5AB1}	V_{DD1}	1.05	mA	
I_{DD5AB2}	V_{DD2}	40		
I_{DD5ABQ}	V_{DDQ5}	0.95		
I_{DD5PB1}	V_{DD1}	1.35	mA	
I_{DD5PB2}	V_{DD2}	44.5		
I_{DD5PBQ}	V_{DDQ}	0.95		

Notes:
1. I_{DD} values reflect dual-channel operation with the same pattern for each channel.
2. Published I_{DD} values except I_{DD4RQ} are the maximum of the distribution of the arithmetic mean. Refer to another note for I_{DD4RQ}. And refer to another table for I_{DD6}.
3. I_{DD4RQ} value is reference only. Typical value. DBI disabled; $V_{OH} = V_{DDQ}/3$, T_C = 25°C.

Table 2: I_{DD} Specifications – Single-Die (T_C = –40°C to +95°C)

V_{DD2}, V_{DDQ} = 1.06–1.17V; V_{DD1} = 1.70–1.95V

Parameter	Supply	Speed Grade	Unit	Note
		3200 Mbps		
I_{DD01}	V_{DD1}	4.1	mA	
I_{DD02}	V_{DD2}	72		
I_{DD0Q}	V_{DDQ}	0.72		
I_{DD2P1}	V_{DD1}	0.54	mA	
I_{DD2P2}	V_{DD2}	4.3		
I_{DD2PQ}	V_{DDQ}	0.4		
I_{DD2PS1}	V_{DD1}	0.54	mA	
I_{DD2PS2}	V_{DD2}	4.35		
I_{DD2PSQ}	V_{DDQ}	0.4		
I_{DD2N1}	V_{DD1}	0.65	mA	
I_{DD2N2}	V_{DD2}	41.5		
I_{DD2NQ}	V_{DDQ}	1		
I_{DD2NS1}	V_{DD1}	0.8	mA	
I_{DD2NS2}	V_{DD2}	16.5		
I_{DD2NSQ}	V_{DDQ}	0.4		
I_{DD3P1}	V_{DD1}	0.8	mA	
I_{DD3P2}	V_{DD2}	16.5		
I_{DD3PQ}	V_{DDQ}	0.4		

Table 2: I_{DD} Specifications – Single-Die (T_C = –40°C to +95°C) (Continued)

V_{DD2}, V_{DDQ} = 1.06–1.17V; V_{DD1} = 1.70–1.95V

Parameter	Supply	Speed Grade	Unit	Note
		3200 Mbps		
I_{DD3PS1}	V_{DD1}	0.8	mA	
I_{DD3PS2}	V_{DD2}	16.5		
I_{DD3PSQ}	V_{DDQ}	0.4		
I_{DD3N1}	V_{DD1}	1.3	mA	
I_{DD3N2}	V_{DD2}	51.5		
I_{DD3NQ}	V_{DDQ}	1		
I_{DD3NS1}	V_{DD1}	1.3	mA	
I_{DD3NS2}	V_{DD2}	47		
I_{DD3NSQ}	V_{DDQ}	1		
I_{DD4R1}	V_{DD1}	2.2	mA	3
I_{DD4R2}	V_{DD2}	420		
I_{DD4RQ}	V_{DDQ}	285		
I_{DD4W1}	V_{DD1}	2.2	mA	
I_{DD4W2}	V_{DD2}	355		
I_{DD4WQ}	V_{DDQ}	102		
I_{DD51}	V_{DD1}	14.5	mA	
I_{DD52}	V_{DD2}	100		
I_{DD5Q}	V_{DDQ}	0.95		
I_{DD5AB1}	V_{DD1}	1.05	mA	
I_{DD5AB2}	V_{DD2}	40		
I_{DD5ABQ}	V_{DDQ5}	0.95		
I_{DD5PB1}	V_{DD1}	1.35	mA	
I_{DD5PB2}	V_{DD2}	44.5		
I_{DD5PBQ}	V_{DDQ}	0.95		

Notes:
1. I_{DD} values reflect dual-channel operation with the same pattern for each channel.
2. Published I_{DD} values except I_{DD4RQ} are the maximum of the distribution of the arithmetic mean. Refer to another note for I_{DD4RQ}. And refer to another table for I_{DD6}.
3. I_{DD4RQ} value is reference only. Typical value. DBI disabled; $V_{OH} = V_{DDQ}/3$, T_C = 25°C.

Table 3: I_{DD6} Full-Array Self Refresh Current

V_{DD2}, V_{DDQ} = 1.06–1.17V; V_{DD1} = 1.70–1.95V

Temperature	Supply	Full-Array Self Refresh Current	Unit
45°C	V_{DD1}	0.1	mA
	V_{DD2}	0.4	
	V_{DDQ}	0.01	
95°C	V_{DD1}	0.95	
	V_{DD2}	7.6	
	V_{DDQ}	0.6	

Notes:
1. I_{DD} values reflect dual-channel operation with the same pattern for each channel.
2. I_{DD6} 45°C is the typical, I_{DD6} 95°C is the maximum of the distribution of the arithmetic mean.