DDR3 Datasheet

RS128M16V8DB-107AT

96-Ball

Revision 1.0

Apr. 27. 2023

Revision History

Version	Date	Editor
V1.0	2023-4-27	Basic spec and architecture

Notes： *This data sheet contains minimum and maximum limits specified over the power supply and temperature range set forth herein. Although considered final, these specifications are subject to change at any time without notice, as further product development and data characterization sometimes occur.*

Contents

1. Product Overview

1.1. Feature Overview

- VDD = VDDQ = +1.5V ±0.075V
- 1.5V center-terminated push/pull I/O
- Differential bidirectional data strobe
- 8n-bit prefetch architecture
- Differential clock inputs (CK, CK#)
- 8 internal banks
- Nominal and dynamic on-die termination (ODT) for data, strobe, and mask signals
- Programmable CAS (READ) latency (CL)
- Posted CAS Addictive latency (AL)
- Programmable CAS (WRITE) latency (CWL) based on tCK
- Fixed burst length (BL) of 8 and burst chop (BC) of 4 (via the mode register set [MRS])
- Selectable BC4 or BL8 on-the-fly (OTF)
- Self refresh mode
- TC of 0°C to 95°C
  - 64ms, 8,192 cycle refresh at 0°C to 85°C
  - 32ms, 8,192 cycle refresh at 85°C to 95°C
- Self refresh temperature (SRT)
- Write leveling
- Multipurpose register
- Output driver calibrationRayson Memory
- Rayson Memory
- Array configuration
  - 128Meg x 16
- Product Code
  - DDR3
- Density
  - 2Gigabyte
- Voltage/Refresh
  - 1.5V/8K refresh
- FBGA package (Pb-free) - x16
  - 96-ball (8mm x 14mm x 1.2mm Max)
- Timing - cycle time
  - 1.07ns @ CL = 13 (DDR3-1866)

2. Physical Specification

2.1. Package ballout & Addressing

96-Ball FBGA – x16 Ball Assignments

	1	2	3	4	5	6	7	8	9	
A	VDDQ	DQ13	DQ15				DQ12	VDDQ	VSS	A
B	VSSQ	VDD	VSS				UDQS#	DQ14	VSSQ	B
C	VDDQ	DQ11	DQ9				UDQS	DQ10	VDDQ	C
D	VSSQ	VDDQ	UDM				DQ8	VSSQ	VDD	D
E	VSS	VSSQ	DQ0				LDM	VSSQ	VDDQ	E
F	VDDQ	DQ2	LDQS				DQ1	DQ3	VSSQ	F
G	VSSQ	DQ6	LDQS#				VDD	VSS	VSSQ	G
H	VREFDQ	VDDQ	DQ4				DQ7	DQ5	VDDQ	H
J	NC	VSS	RAS#				CK	VSS	NC	J
K	ODT	VDD	CAS#				CK#	VDD	CKE	K
L	NC	CS#	WE#				A10/AP	ZQ	NC	L
M	VSS	BA0	BA2				NC	VREFCA	VSS	M
N	VDD	A3	A0				A12/BC #	BA1	VDD	N
P	VSS	A5	A2				A1	A4	VSS	P
R	VDD	A7	A9				A11	A6	VDD	R
T	VSS	RESET#	A13				NC	A8	VSS	T

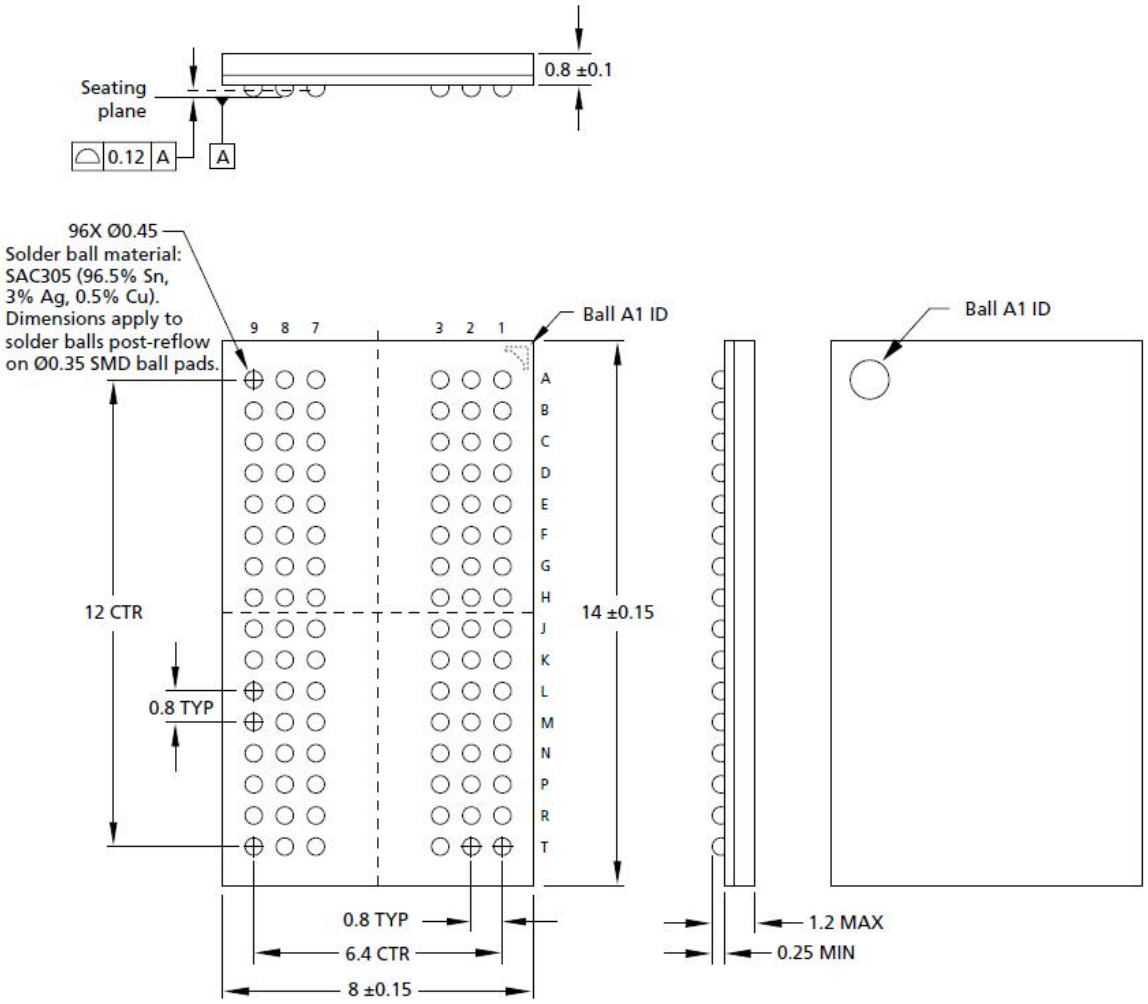
2.2. Pad Definition

Symbol	Type	Description
CK, CK#	Input	**Differential Clock:** CK and CK# are driven by the system clock. All SDRAM input signals are sampled on the crossing of positive edge of CK and negative edge of CK#. Output (Read) data is referenced to the crossings of CK and CK# (both directions of crossing).
CKE	Input	**Clock Enable:** CKE activates (HIGH) and deactivates (LOW) the CK signal. If CKE goes LOW synchronously with clock, the internal clock is suspended from the next clock cycle and the state of output and burst address is frozen as long as the CKE remains LOW. When all banks are in the idle state, deactivating the clock controls the entry to the Power Down and Self Refresh modes.
BA0-BA2	Input	**Bank Address:** BA0-BA2 define to which bank the BankActivate, Read, Write, or Bank Precharge command is being applied.
A0-A13	Input	**Address Inputs:** Provide the row address (A0-13) for Active commands and the column address (A0-9) for Read/Write commands to select one location out of the memory array in the respective bank. (A10/AP and A12/BC# have additional functions). The address inputs also provide the op-code during Mode Register Set commands.
A10/AP	Input	**Auto-Precharge:** A10 is sampled during Read/Write commands to determine whether Auto precharge should be performed to the accessed bank afterthe Read/Write operation. (HIGH: Autoprecharge; LOW: no Autoprecharge). A10 is sampled during a Precharge command to determine whether the Precharge applies to one bank (A10 LOW) or all banks (A10 HIGH).
A12/BC#	Input	**Burst Chop:** A12/BC# is sampled during Read and Write commands to determine if burst chop (on the fly) will be performed. (HIGH - no burst chop; LOW - burst chopped).
CS#	Input	**Chip Select:** CS# enables (sampled LOW) and disables (sampled HIGH) the command decoder. All commands are masked when CS# is sampled HIGH. It is considered part of the command code.
RAS#	Input	**Row Address Strobe:** The RAS# signal defines the operation commands in conjunction with the CAS# and WE# signals and is latched at the crossing of positive edges of CK and negative edge of CK#. When RAS# and CS# are asserted "LOW" and CAS# is asserted "HIGH" either the BankActivate command or the Precharge command is selected by the WE# signal. When the WE# is asserted "HIGH" the BankActivate command is selected and the bank designated by BA is turned on to the active state. When the WE# is asserted "LOW" the Precharge command is selected and the bank designated by BA is switched to the idle state after the precharge operation.

Symbol	Type	Description
CAS#	Input	**Column Address Strobe:** The CAS# signal defines the operation commands in conjunction with the RAS# and WE# signals and is latched at the crossing of positive edges of CK and negative edge of CK#. When RAS# is held "HIGH" and CS# is asserted "LOW" the column access is started by asserting CAS# "LOW". Then, the Read or Write command is selected by asserting WE# “HIGH" or “LOW".
WE#	Input	**Write Enable:** The WE# signal defines the operation commands in conjunction with the RAS# and CAS# signals and is latched at the crossing of positive edges of CK and negative edge of CK#. The WE# input is used to select the BankActivate or Precharge command and Read or Write command.
LDQS, LDQS# UDQS, UDQS#	Input/Output	**Bidirectional Data Strobe:** Specifies timing for Input and Output data. Read Data Strobe is edge triggered. Write Data Strobe provides a setup and hold time for data and DQM. LDQS is for DQ0~7, UDQS is for DQ8~15. The data strobes LDOS and UDQS are paired with LDQS# and UDQS# to provide differential pair signaling to the system during both reads and writes.
LDM, UDM	Input	**Data Input Mask:** Input data is masked when DM is sampled HIGH during a write cycle. LDM masks DQ0-DQ7, UDM masks DQ8-DQ15.
DQ0-DQ15	Input/Output	**Data I/O:** The DQ0-DQ15 input and output data are synchronized with positive and negative edges of DQS and DQS#. The I/Os are byte-maskable during Writes.
ODT	Input	**On Die Termination:** ODT (registered HIGH) enables termination resistance internal to the DDR3 SDRAM. When enabled, ODT is applied to each DQ, DQS, DQS#. The ODT pin will be ignored if Mode-registers, MR1and MR2, are programmed to disable RTT.
RESET#	Input	**Active Low Asynchronous Reset:** Reset is active when RESET# is LOW, and inactive when RESET# is HIGH. RESET# must be HIGH during normal operation. RESET# is a CMOS rail to rail signal with DC high and low at 80% and 20% of VDD.
VDD	Supply	**Power Supply:** +1.5V±0.075V.
VSS	Supply	**Ground**
VDDQ	Supply	**DQ Power:** +1.5V±0.075V.
VSSQ	Supply	**DQ Ground**
VREFCA	Supply	**Reference voltage for CA**
VREFDQ	Supply	**Reference voltage for DQ**
ZQ	Supply	**Reference pin for ZQ calibration.**
NC	-	**No Connect:** These pins should be left unconnected.

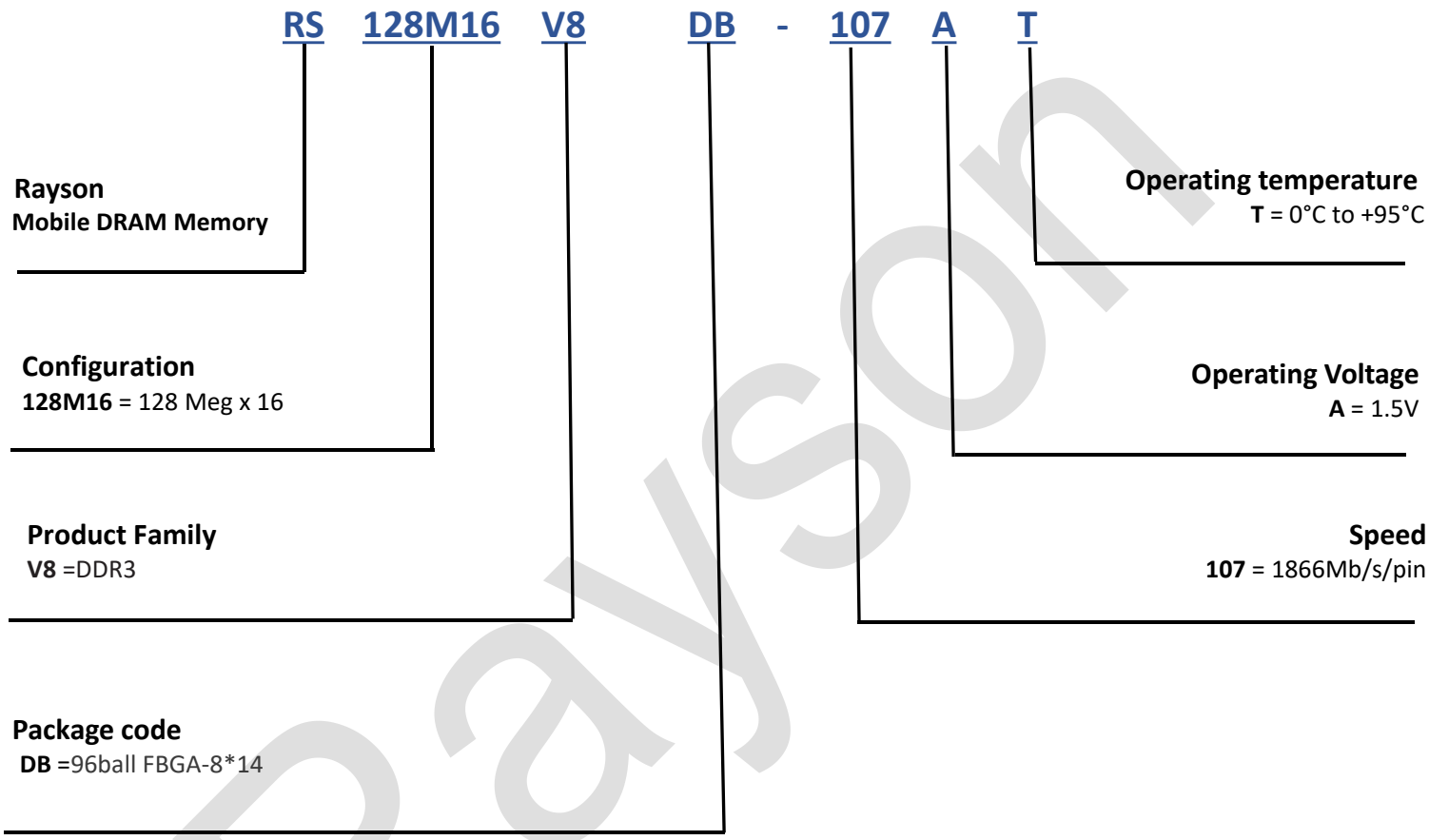
2.3. Discrete Package Dimension

8mm X 14mm



3. Core Specifications

3.1. Part Number Decoding



3.2. Ordering Options

Table 1: Key Timing Parameters

Speed	DDR3-1866	Unit
	13-13-13	
tCK (min)	1.07	ns
CAS Latency	13	nCK
tRCD (min)	13.91	ns
tRP (min)	13.91	ns
tRAS (min)	34	ns
tRC (min)	48.91	ns

Table 2: Part Number List

Part Number	Organization	Data Rate	CL-^{t}RCD-^{t}RP
RS128M16V8DB-107AT	128Mb x 16	1866 Mb/s/pin	13-13-13

3.3. Die Addressing Table

Parameter	128 Meg × 16
Number of Bank Groups	2
Bank Group Address	BG0
Bank count per group	4
Bank Address per Bank Group	BA[1:0]
Row Address	16K (A[13:0])
Column Address	1K (A[9:0])
Page Size	2KB

Notes: 1、Page size is per bank, calculated as follows:
Page size = 2COLBITS x ORG/8, where COLBIT = the number of column address bits and ORG = the number of DQ bits.
2、Die revision dependent.