



LPDDR5/5X Datasheet

RS1G64LP5D4FGD-23BT

RS2G64LP5D8FGD-23BT

496-ball

Revision 1.2

May. 13. 2025

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Revision History

Version	Date	Changes
V1.0	2023-6-28	Basic spec and architecture
V1.1	2024-10-21	1) Add some content 2) Change discrete package dimension
V1.2	2025-5-13	1) Add IDD parameters 2) Change discrete package dimension

Notes: This data sheet contains minimum and maximum limits specified over the power supply and temperature range set forth herein. Although considered final, these specifications are subject to change at any time without notice, as further product development and data characterization sometimes occur.

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1. Product Overview

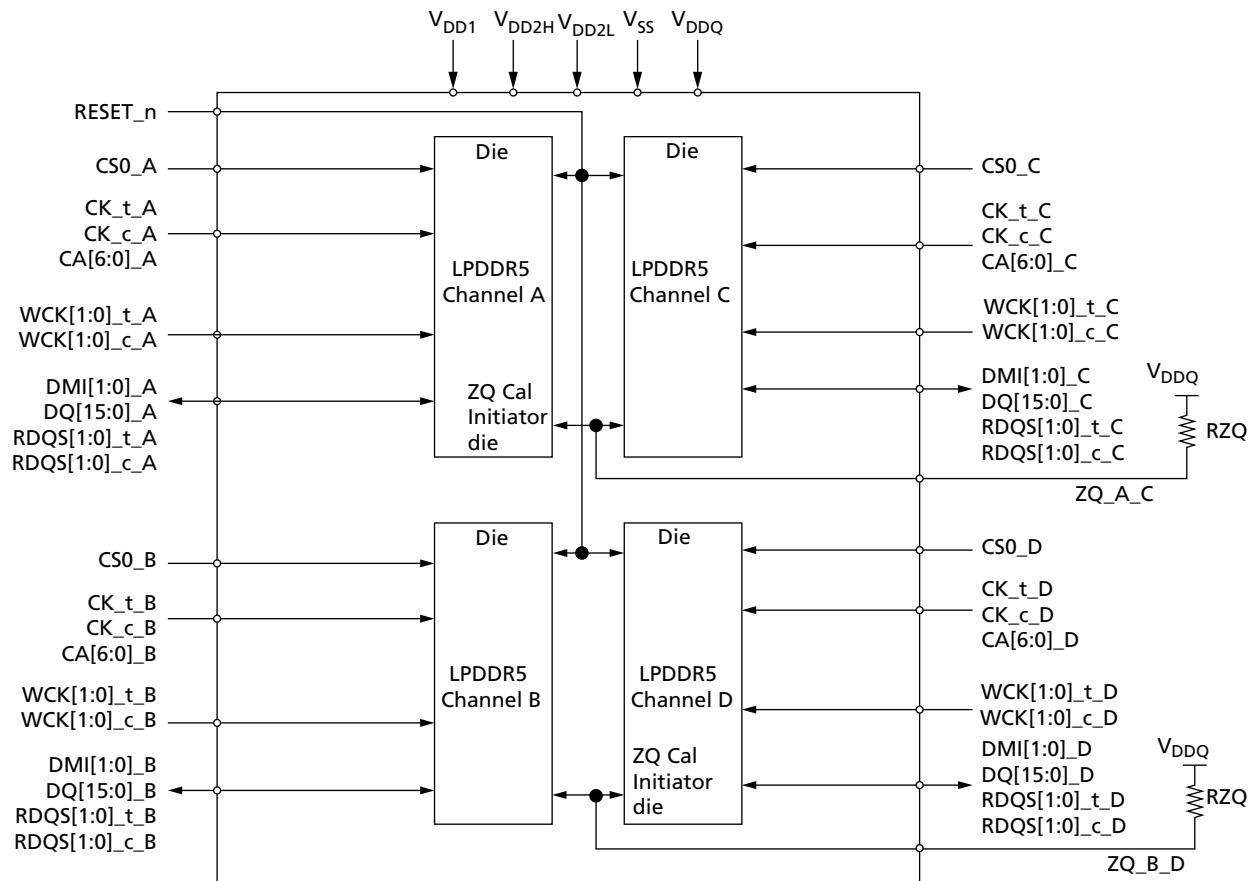
1.1. Feature Overview

- Architecture
 - 17.1 GB/s maximum bandwidth per channel
 - Frequency range: 1067–5 MHz (data rate range per pin: 8533–40 Mbp/s with WCK:CK = 4:1)
 - Selectable CKR (WCK:CK = 2:1 or 4:1)
- LPDDR5 data interface
 - Single x16 channel/die
 - Double-data-rate command/address entry
 - Differential command clocks (CK_t/CK_c) for high-speed operation
 - Differential data clocks (WCK_t/WCK_c)
 - Optional differential read strobe (RDQS_t/ RDQS_c)
 - 16n-bit or 32n-bit prefetch architecture
 - 2KB page size with bank group (BG mode), or 16-bank (16B mode) operation
 - Command-selectable burst lengths (BL = 16 or 32) in bank group or 16-bank modes
 - Background ZQ calibration/command-based ZQ calibration- Optional link protection (link ECC)
 - Optional link protection (link ECC)
 - Partial-array self refresh (PASR) and partial-array auto refresh (PAAR) with segment mask
- Ultra-low-voltage core and I/O power supplies
 - $V_{DD1} = 1.70\text{--}1.95\text{V}$; 1.8V NOM
 - $V_{DD2H} = 1.01\text{--}1.12\text{V}$; 1.05V NOM
 - $V_{DD2L} = V_{DD2H}$ or $0.87\text{--}0.97\text{V}$; 0.9V NOM
 - $V_{DDQ} = 0.5\text{V NOM}$ or 0.3V NOM (ODT off)
- I/O characteristics
 - Interface-LVSTL 0.5/0.3
 - I/O type: Low-swing single-ended, V_{SS} terminated
 - V_{OH} -compensated output drive

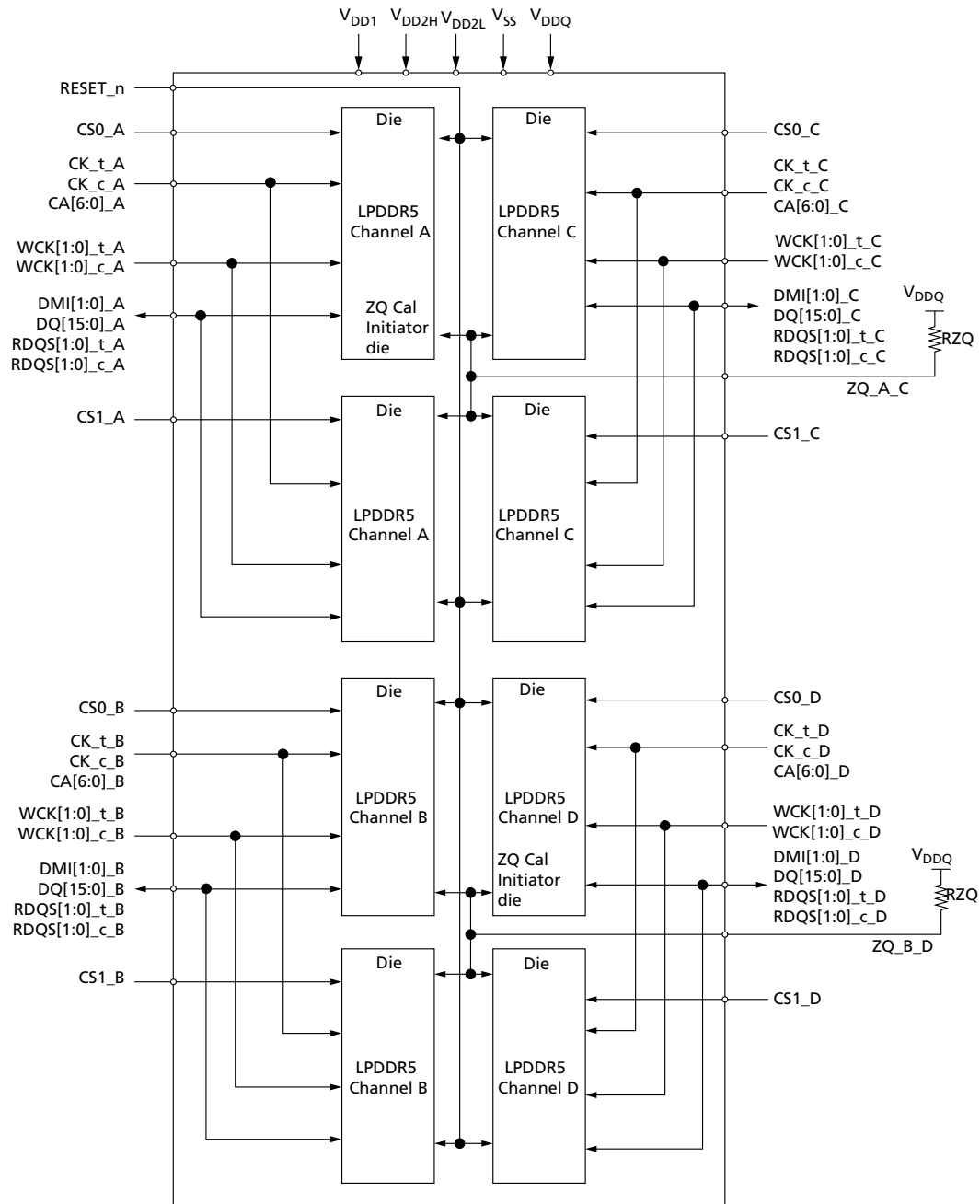
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- Programmable V_{SS} on-die termination (ODT)
 - Non target ODT support
 - DVFSQ support
 - Low power features
 - DVFSC: Dynamic voltage frequency scaling core
 - Single-ended CK, single-ended WCK, and single-ended RDQS
 - $V_{DD1}/V_{DD2H}/V_{DD2L}/V_{DDQ}$ (ODT on)/ (ODT off): 1.8V/1.05V/0.9V/0.5V/0.3V
 - Array configuration
 - 1 Gig × 64 (4 channels × 16 I/O)
 - 2 Gig × 64 (4 channels × 16 I/O)
 - Device configuration
 - 1G16 × 4 die in package
 - 1G16 × 8 die in package
 - FBGA "green" package
 - 496-ball FBGA (14mm × 12.4mm Seated height: 0.763mm MAX)
 - Speed grade, cycle time(t_{WCK})
 - 8533 Mb/s
 - Operating temperature range
 - -25°C to + 85 °C

2. Physical Specifications

2.1. Function Block Diagram



Quad-Die, Quad-Channel Package, Single-Rank Block Diagram



Eight-Die, Quad-Channel Package, Dual-Rank Block Diagram

2.2. Package ballout & Addressing

496-Ball Quad-Channel POP FBGA

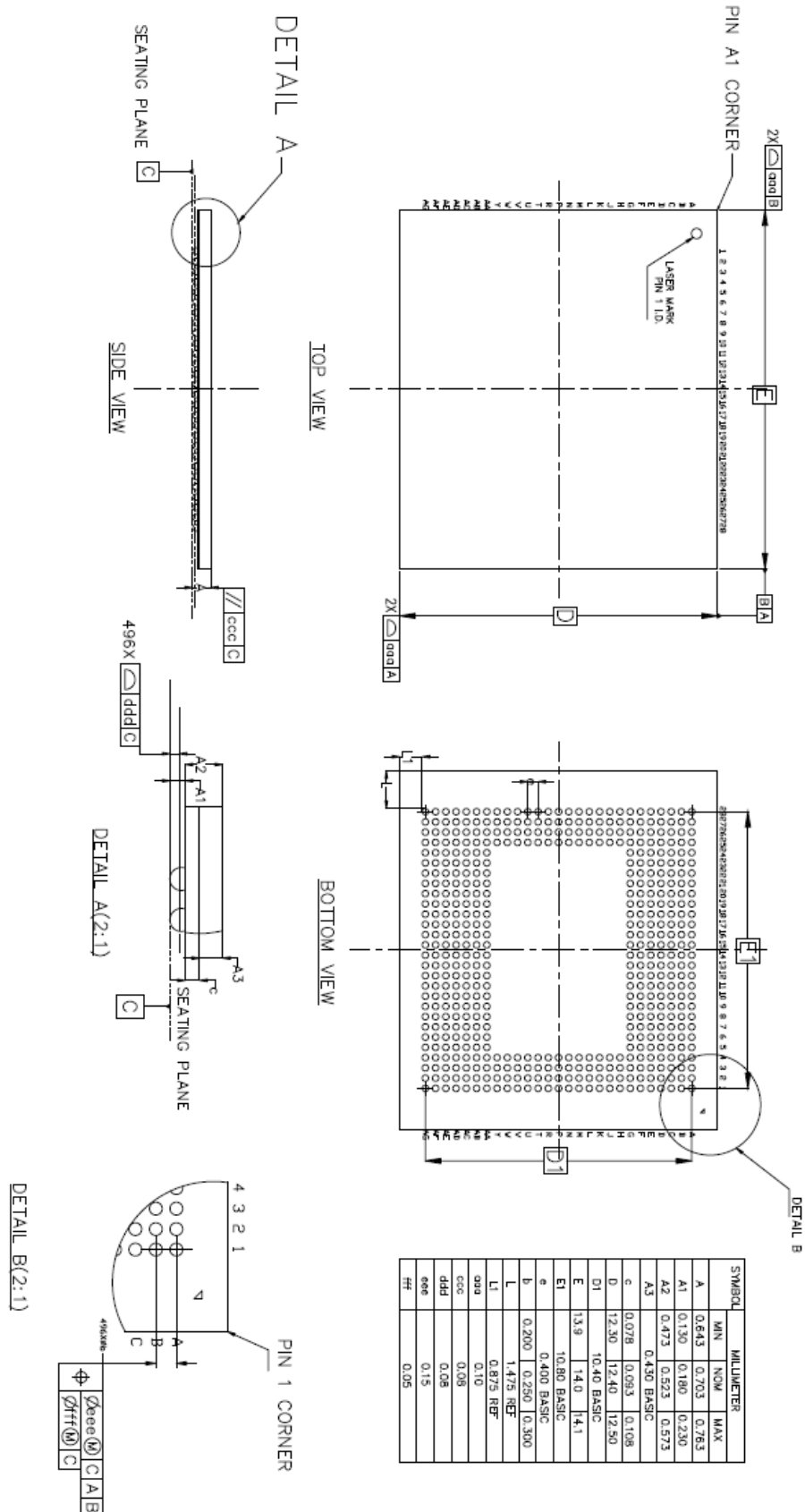
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	
A	NC	NC	V _{DD1}	V _{DD2H}	V _{DD2L}	V _{DDQ}	V _{SS}	V _{DD2H}	V _{DD2L}	V _{DD2H}	V _{DD2H}	V _{DDQ}	V _{DD1}	V _{DD2L}	V _{DD2L}	V _{DD1}	V _{DDQ}	V _{DD2H}	V _{DD2H}	V _{SS}	V _{DD2H}	V _{DD2L}	V _{DDQ}	V _{DD2L}	V _{DD2H}	V _{DD1}	NC	NC	A
B	NC	DQ3_A	RDQS0_t_A	V _{SS}	DQ5_A	V _{SS}	CS1_A	V _{SS}	V _{SS}	DQ13_A	V _{SS}	RDQS1_t_A	V _{SS}	DQ9_A	DQ1_C	V _{SS}	RDQS0_t_C	V _{SS}	DQ5_C	V _{SS}	CS1_C	V _{SS}	V _{SS}	DQ13_C	V _{SS}	RDQS1_t_C	DQ11_C	NC	B
C	DQ1_A	V _{SS}	RDQS0_c_A	DMI0_A	V _{DDQ}	CA0_A	CS0_A	CA4_A	CA6_A	V _{DDQ}	DMI1_A	RDQS1_c_A	DQ11_A	V _{DDQ}	V _{DDQ}	DQ3_C	RDQS0_c_C	DMI0_C	V _{DDQ}	CA0_C	CS0_C	CA4_C	CA6_C	V _{DDQ}	DMI1_C	RDQS1_c_C	V _{SS}	DQ9_C	C
D	V _{DDQ}	DQ2_A	V _{DDQ}	V _{SS}	DQ6_A	V _{SS}	CA2_A	CA3_A	V _{SS}	DQ14_A	V _{SS}	V _{DDQ}	V _{SS}	DQ8_A	DQ0_C	V _{SS}	V _{DDQ}	V _{SS}	DQ6_C	V _{SS}	CA2_C	CA3_C	V _{SS}	DQ14_C	V _{SS}	V _{DDQ}	DQ10_C	V _{DDQ}	D
E	DQ0_A	V _{DDQ}	WCK0_c_A	DQ4_A	V _{DDQ}	CA1_A	V _{DD2H}	V _{DD2L}	CA5_A	V _{DDQ}	DQ12_A	WCK1_c_A	DQ10_A	V _{DDQ}	V _{DDQ}	DQ2_C	WCK0_c_C	DQ4_C	V _{DDQ}	CA1_C	V _{DD2H}	V _{DD2L}	CA5_C	V _{DDQ}	DQ12_C	WCK1_c_C	V _{DDQ}	DQ8_C	E
F	V _{SS}	V _{SS}	WCK0_t_A	V _{SS}	DQ7_A	V _{SS}	CK_t_A	CK_c_A	V _{SS}	DQ15_A	V _{SS}	WCK1_t_A	V _{SS}	ZQ_A_C	RESET_n	V _{SS}	WCK0_t_C	V _{SS}	DQ7_C	V _{SS}	CK_t_C	CK_c_C	V _{SS}	DQ15_C	V _{SS}	WCK1_t_C	V _{SS}	V _{SS}	F
G	V _{DD2H}	V _{DD1}	V _{DD2L}	V _{DDQ}	V _{DD2H}	V _{DD2L}	V _{SS}	V _{SS}	V _{DD2H}	V _{DD2L}	V _{DD2H}	V _{SS}	V _{DD2L}	V _{DD2H}	V _{DD2H}	V _{DD2L}	V _{SS}	V _{DD2H}	V _{DD2H}	V _{DD2L}	V _{SS}	V _{SS}	V _{DD2H}	V _{DD2L}	V _{DDQ}	V _{DD2L}	V _{DD1}	V _{DD2H}	G
H	V _{DD2H}	V _{DD1}	V _{DD2H}	V _{DD2H}																				V _{DD2H}	V _{DD2H}	V _{DD1}	V _{DD2H}	H	
J	V _{SS}	V _{SS}	V _{SS}	V _{SS}																				V _{SS}	V _{SS}	V _{SS}	V _{SS}	J	
K	V _{SS}	V _{SS}	V _{SS}	V _{SS}																				V _{SS}	V _{SS}	V _{SS}	V _{SS}	K	
L	V _{SS}	V _{SS}	V _{SS}	V _{SS}																				V _{SS}	V _{SS}	V _{SS}	V _{SS}	L	
M	V _{SS}	V _{SS}	V _{SS}	V _{SS}																				V _{SS}	V _{SS}	V _{SS}	V _{SS}	M	
N	V _{SS}	V _{SS}	V _{SS}	V _{SS}																				V _{SS}	V _{SS}	V _{SS}	V _{SS}	N	
P	V _{SS}	V _{SS}	V _{SS}	V _{SS}																				V _{SS}	V _{SS}	V _{SS}	V _{SS}	P	
R	V _{SS}	V _{SS}	V _{SS}	V _{SS}																				V _{SS}	V _{SS}	V _{SS}	V _{SS}	R	
T	V _{SS}	V _{SS}	V _{SS}	V _{SS}																				V _{SS}	V _{SS}	V _{SS}	V _{SS}	T	
U	V _{SS}	V _{SS}	V _{SS}	V _{SS}																				V _{SS}	V _{SS}	V _{SS}	V _{SS}	U	
V	V _{SS}	V _{SS}	V _{SS}	V _{SS}																				V _{SS}	V _{SS}	V _{SS}	V _{SS}	V	
W	V _{SS}	V _{SS}	V _{SS}	V _{SS}																				V _{SS}	V _{SS}	V _{SS}	V _{SS}	W	
Y	V _{DD2H}	V _{DD1}	V _{DD2H}	V _{DD2H}																				V _{DD2H}	V _{DD2H}	V _{DD1}	V _{DD2H}	Y	
AA	V _{DD2H}	V _{DD1}	V _{DD2L}	V _{DDQ}	V _{DD2H}	V _{DD2L}	V _{SS}	V _{SS}	V _{DD2H}	V _{DD2L}	V _{DD2H}	V _{SS}	V _{DD2L}	V _{DD2H}	V _{DD2H}	V _{DD2L}	V _{SS}	V _{DD2H}	V _{DD2H}	V _{DD2L}	V _{SS}	V _{SS}	V _{DD2H}	V _{DD2L}	V _{DDQ}	V _{DD2L}	V _{DD1}	V _{DD2H}	AA
AB	V _{SS}	V _{SS}	WCK1_t_B	V _{SS}	DQ15_B	V _{SS}	CK_c_B	CK_t_B	V _{SS}	DQ7_B	V _{SS}	WCK0_t_B	V _{SS}	NC	ZQ_B_D	V _{SS}	WCK1_t_D	V _{SS}	DQ15_D	V _{SS}	CK_c_D	CK_t_D	V _{SS}	DQ7_D	V _{SS}	WCK0_t_D	V _{SS}	V _{SS}	AB
AC	DQ8_B	V _{DDQ}	WCK1_c_B	DQ12_B	V _{DDQ}	CA5_B	V _{DD2L}	V _{DD2H}	CA1_B	V _{DDQ}	DQ4_B	WCK0_c_B	DQ2_B	V _{DDQ}	V _{DDQ}	DQ10_D	WCK1_c_D	DQ12_D	V _{DDQ}	CA5_D	V _{DD2L}	V _{DD2H}	CA1_D	V _{DDQ}	DQ4_D	WCK0_c_D	V _{DDQ}	DQ0_D	AC
AD	V _{DDQ}	DQ10_B	V _{DDQ}	V _{SS}	DQ14_B	V _{SS}	CA3_B	CA2_B	V _{SS}	DQ6_B	V _{SS}	V _{DDQ}	V _{SS}	DQ0_B	DQ8_D	V _{SS}	V _{DDQ}	V _{SS}	DQ14_D	V _{SS}	CA3_D	CA2_D	V _{SS}	DQ6_D	V _{SS}	V _{DDQ}	DQ2_D	V _{DDQ}	AD
AE	DQ9_B	V _{SS}	RDQS1_c_B	DMI1_B	V _{DDQ}	CA6_B	CA4_B	CS0_B	CA0_B	V _{DDQ}	DMI0_B	RDQS0_c_B	DQ3_B	V _{DDQ}	V _{DDQ}	DQ11_D	RDQS1_c_D	DMI1_D	V _{DDQ}	CA6_D	CA4_D	CS0_D	CA0_D	V _{DDQ}	DMI0_D	RDQS0_c_D	V _{SS}	DQ1_D	AE
AF	NC	DQ11_B	RDQS1_t_B	V _{SS}	DQ13_B	V _{SS}	V _{SS}	CS1_B	V _{SS}	DQ5_B	V _{SS}	RDQS1_t_B	V _{SS}	DQ1_B	DQ9_D	V _{SS}	RDQS1_t_D	V _{SS}	DQ13_D	V _{SS}	V _{SS}	CS1_D	V _{SS}	DQ5_D	V _{SS}	RDQS0_t_D	DQ3_D	NC	AF
AG	NC	NC	V _{DD1}	V _{DD2H}	V _{DD2L}	V _{DDQ}	V _{SS}	V _{DD2H}	V _{DD2L}	V _{DD2H}	V _{DD2H}	V _{DDQ}	V _{DD1}	V _{DD2L}	V _{DD2L}	V _{DD1}	V _{DDQ}	V _{DD2H}	V _{DD2H}	V _{DD2L}	V _{DD2H}	V _{SS}	V _{DDQ}	V _{DD2L}	V _{DD2H}	V _{DD1}	NC	NC	AG
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	
Top View (ball down)																													
V_{SS} V_{DD1} V_{DD2H} V_{DD2L} V_{DDQ} CK RDQS WCK DQ,DMI CA, CS, ZQ, RESET NC																													

2.3. Pad Definition

Symbol	Type	Description
CK_t_[A:D] CK_c_[A:D]	Input	Clock: CK_t and CK_c are differential clock inputs. All double data rate (DDR) command/address inputs are sampled on both crossing points of CK_t and CK_c. The first crossing point is the rising (falling) edge of CK_t (CK_c) and second crossing point is falling (rising) edge of CK_t (CK_c). Single data rate (SDR) inputs, CS is sampled on the crossing point that is the rising (falling) edge of CK_t (CK_c).
CS0_[A:D], CS1_[A:D]	Input	Chip select: CS is part of the command code, and is sampled on the rising (falling) edge of CK_t (CK_c) unless the device is in power-down or deep sleep mode where it becomes an asynchronous signal. Each rank (0, 1) has its own CS signals. CS1_[A:B] be- come NC pins in a single-rank package.
CA[6:0]_[A:D]	Input	Command/address inputs: Provide the command and address inputs according to the command truth table.
WCK[1:0]_t_[A:D], WCK[1:0]_c_[A:D]	Input	Data clock: WCK_t and WCK_c are differential clock inputs used for write data capture and read data output.
DQ[15:0]_[A:D]	I/O	Data input/output: Bidirectional databus.
RDQS[1:0]_t_[A:D], RDQS[1:0]_c_[A:D]	I/O Output	Read data strobe: RDQS_t and RDQS_c are differential output clock signals used to strobe data during a READ operation. RDQS_t is also used as a parity pin during write link protection enabled. Each byte of data has RDQS_t and RDQS_c signals.
DMI[1:0]_[A:D]	I/O	Data mask inversion: DMI serves multiple functions such as data mask (DM), data bus inversion (DBI), and parity at READ with ECC operation by setting the mode register. DMI is a bidirectional signal and each byte of data has a DMI signal.
ZQ_A_C, ZQ_B_D	Reference	ZQ calibration reference: Used to calibrate the output drive strength and the termination resistance. The ZQ pin should be connected to VDDQ through a 240Ω ±1% resistor.
V _{DDQ} , V _{DD1} , V _{DD2H} , V _{DD2L}	Supply	Power supplies: Isolated on the die for improved noise immunity.
V _{SS}	Supply	Ground reference: Power supply ground reference.
RESET_n	Input	RESET: When asserted LOW, the RESET pin resets all channels of the die. Reset is an asynchronous signal.
NC	–	No connect: Not internally connected.

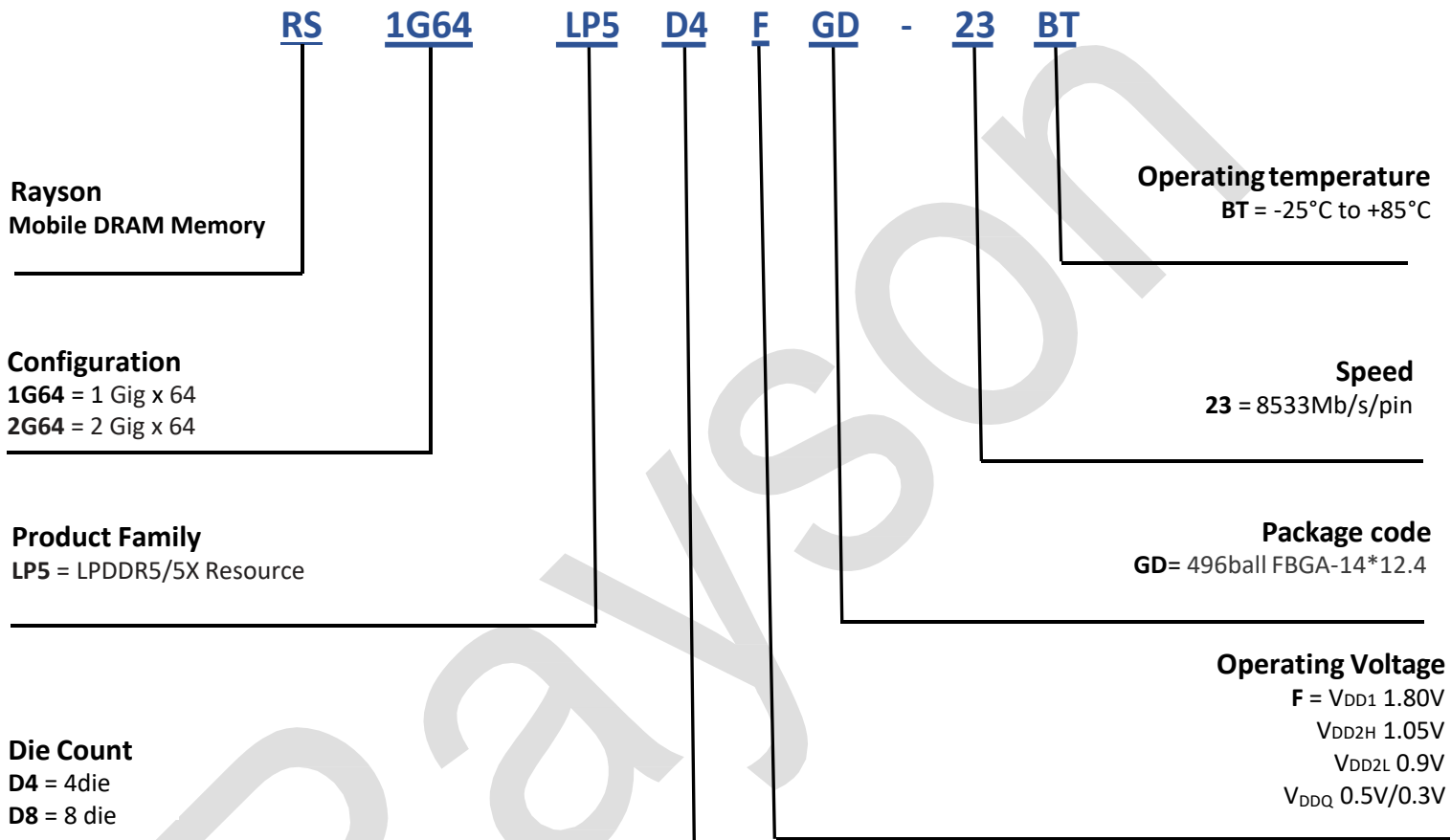
2.4. Discrete Package Dimension

14mm X12.4mm



3. Core Specifications

3.1. Part Number Decoding



3.2. Ordering Options

Table 1: Part Number List

Part Number	Total Density	Data Rate	Operating temperature
RS1G64LP5D4FGD-23BT	8GB(64Gb)	8533 Mb/s/pin	-25°C to + 85°C
RS2G64LP5D8FGD-23BT	16GB(128Gb)	8533 Mb/s/pin	-25°C to + 85°C

Table 2: Refresh Requirement Parameters

Parameter	Symbol	16Gb	unit
		BG and 16B Mode	
REFRESH cycle time (all banks)	t_{RFCab}	280	ns
REFRESH cycle time (per bank)	t_{RFCpb}	140	ns
Per bank refresh to per bank refresh time (different bank)	$t_{PBR2PBR}$	90	ns
Per bank refresh to ACTIVATE command time (different bank)	$t_{PBR2ACT}$	7.5	ns

3.3. Die Addressing Table

Configuration		1G64 (64Gb/package)	2G64 (128Gb/package)
Die Configuration	Channel A, rank 0 Channel B, rank 0	× 16 mode × 1 die × 16 mode × 1 die	× 16 mode × 1 die × 16 mode × 1 die
	Channel C, rank 0 Channel D, rank 0	× 16 mode × 1 die × 16 mode × 1 die	× 16 mode × 1 die × 16 mode × 1 die
	Channel A, rank 1 Channel B, rank 1	-	× 16 mode × 1 die × 16 mode × 1 die
	Channel C, rank 1 Channel D, rank 1	-	× 16 mode × 1 die × 16 mode × 1 die
Die Addressing	Bits	17,179,869,184	
	Bank mode	BG mode	16B mode
	Configuration	64Mb × 16 DQ × 4 Banks × 4 BG	64Mb × 16 DQ × 16 Banks
	Number of banks	4	16
	Number of banks groups	4	1
	Array prefetch bits	256	
	Rows per bank	65,536	
	Columns	64	
	Page size (bytes)	2048	
	Native burst length	16	
	Number of I/Os	16	
	Bank address	BA[1:0]	BA[3:0]
	Bank group address	BG[1:0]	-
	Row address	R[15:0]	
	Column address	C[5:0]	
	Burst address	B[3:0]	
	Burst starting address boundar	128-bit	

3.4. Mode Register Contents

MR0			MR1		
OP7	Per-pin DFE	OP[0] = 1b: Device supports different NT ODT latency for DQ and RDQS OP[1] = 0b: Device supports x16 mode OP[2] = 1b: Device supports enhanced WCK always-on mode. OP[3] = 1b: Device supports optimized refresh mode OP[4] = 1b: Device supports both DMI behavior mode 1 and 2 and mode selection OP[5] = 1b: The NT ODT behavior follows the unified NT ODT behavior OP[6] = 1b: Device supports Pre Emphasis mode OP[7] = 0b: Device does not support Per Pin DFE	OP7		OP[0] = 0b: Device does not support CS ODT behavior OP OP[1] = 1b: Device supports ARFM
OP6	Pre Emphasis		OP6		
OP5	Unified NT ODT behavior mode		OP5		
OP4	DMI output behavior mode		OP4		
OP3	Optimized refresh mode		OP3		
OP2	Enhanced WCK always-on mode		OP2		
OP1	Latency Mode		OP1	ARFM support	
OP0	NT ODT timing mode		OP0	CS ODT OP support	

MR3			MR5		
OP7			OP7	Manufacturer ID	1111 1111b : Micron
OP6			OP6		
OP5			OP5		
OP4			OP4		
OP3	BK/BG Org	OP[4:3] = 00b: BG; 10b: 16B Mode Supported	OP3		
OP2			OP2		
OP1			OP1		
OP0			OP0		

MR6		
OP7	Revision ID1	0000 1000b
OP6		
OP5		
OP4		
OP3		
OP2		
OP1		
OP0		

MR8		
OP7	I/O width	OP[7:6] = 00b: x16/channel
OP6		
OP5	Density	OP[5:2] = 0110b: 16Gb
OP4		
OP3		
OP2		
OP1	Type	OP[1:0] = 01b: LPDDR5X SDRAM
OP0		

MR13		
OP7		OP[2]=0b: Normal operation (default) 1b: Output the VREF(CA) value on DQ7 and VREF(DQ) value on DQ6
OP6		
OP5		
OP4		
OP3		
OP2		
OP1		
OP0	VR0	

MR19		
OP7		OP[5] = 1b: WCK2DQ Osc FM supported
OP6		
OP5	WCK2DQ Osc FM support	
OP4		
OP3		
OP2		
OP1		
OP0		

MR21		
OP7	WXS	OP[0] = 1b: WRITE DATA COPY function supported OP[1] = 1b: READ DATA COPY function supported OP[2] = 1b: WRITE X function supported OP[3] = 1b: Device ODTD-CS is supported OP[7] = 1b: Data to be written can be selected with 0 and 1
OP6		
OP5		
OP4		
OP3	ODTD-CSFS	
OP2	WXFS	
OP1	RDCFS	
OP0	WDCFS	

MR22		
OP7	RECC	OP[5:4] = 00b: Write link ECC disabled (default) 01b: Write link ECC enabled OP[7:6] = 00b: Read link ECC disabled (default) 01b: Read link ECC enabled
OP6		
OP5	WECC	
OP4		
OP3		
OP2		
OP1		
OP0		

MR24		
OP7	DFES	OP[3] = 1b: Device supports Read DCA OP[7] = 1b: Devices supports DFE
OP6		
OP5		
OP4		
OP3	Read DCA	
OP2		
OP1		
OP0		

MR26		
OP7		OP[6] = 1b: Read/write-based RDQS_t TRAINING function supported
OP6	RDQSTFS	
OP5		
OP4		
OP3		
OP2		
OP1		
OP0		

MR27		
OP7	RAAMULT	OP[0] = 1b: RFM is required OP[5:1] = 00101b: 40 OP[7:6]=01b: 4X
OP6		
OP5	RAAIMT	
OP4		
OP3		
OP2		
OP1		
OP0	RFM	

MR43		
OP7		OP[6] = 1b: Simultaneous SBE on each DQ byte and DMI are independently counted
OP6	SBEC Rule	
OP5		
OP4		
OP3		
OP2		
OP1		
OP0		

MR57		
OP7		OP[1:0] = 10b: 2 x RAAIMT OP[3:2] = 00b: 1=Does not support single-bank mode
OP6		
OP5		
OP4		
OP3	RFMSB	
OP2		
OP1	RAADEC	
OP0		

- Notes:** 1、 *The contents of Product Specific Mode Register definition will reflect information specific to each die in these packages.*
- 2、 *Refer to General LPDDR5 Specifications 1 for mode registers not described here.*
- 3、 *Write link ECC and read link ECC are supported.*

4. Parameters

Table 1: I_{DD} Parameters – Single Die

Symbol	Supply	Speed Grade		Unit	Note
		7500 Mb/s	8533 Mb/s		
I _{DD01}	V _{DD1}	3.80	3.80	mA	2
I _{DD02H}	V _{DD2H}	53.00	53.00		
I _{DD02L}	V _{DD2L}	0.20	0.20		
I _{DD0Q}	V _{DDQ}	0.60	0.60		
I _{DD2P1}	V _{DD1}	1.50	1.50	mA	2
I _{DD2P2H}	V _{DD2H}	3.90	3.90		
I _{DD2P2L}	V _{DD2L}	0.20	0.20		
I _{DD2PQ}	V _{DDQ}	0.60	0.60		
I _{DD2PS1}	V _{DD1}	1.50	1.50	mA	2
I _{DD2PS2H}	V _{DD2H}	3.90	3.90		
I _{DD2PS2L}	V _{DD2L}	0.20	0.20		
I _{DD2PSQ}	V _{DDQ}	0.60	0.60		
I _{DD2N1}	V _{DD1}	1.50	1.50	mA	2
I _{DD2N2H}	V _{DD2H}	32.50	32.50		
I _{DD2N2L}	V _{DD2L}	0.20	0.20		
I _{DD2NQ}	V _{DDQ}	0.60	0.60		
I _{DD2NS1}	V _{DD1}	1.50	1.50	mA	2
I _{DD2NS2H}	V _{DD2H}	32.50	32.50		
I _{DD2NS2L}	V _{DD2L}	0.20	0.20		
I _{DD2NSQ}	V _{DDQ}	0.60	0.60		
I _{DD3P1}	V _{DD1}	2.50	2.50	mA	2
I _{DD3P2H}	V _{DD2H}	12.50	12.50		
I _{DD3P2L}	V _{DD2L}	0.20	0.20		
I _{DD3PQ}	V _{DDQ}	0.60	0.60		
I _{DD3PS1}	V _{DD1}	2.50	2.50	mA	2
I _{DD3PS2H}	V _{DD2H}	12.50	12.50		
I _{DD3PS2L}	V _{DD2L}	0.20	0.20		
I _{DD3PSQ}	V _{DDQ}	0.60	0.60		

Table 1: I_{DD} Parameters – Single Die

Symbol	Supply	Speed Grade		Unit	Note
		7500 Mb/s	8533 Mb/s		
I _{DD3N1}	V _{DD1}	2.80	2.80	mA	2
I _{DD3N2H}	V _{DD2H}	40.00	40.00		
I _{DD3N2L}	V _{DD2L}	0.20	0.20		
I _{DD3NQ}	V _{DDQ}	0.60	0.60		
I _{DD4R1}	V _{DD1}	18.00	20.50	mA	2, 3, 4
I _{DD4R2H}	V _{DD2H}	390.00	430.00		
I _{DD4R2L}	V _{DD2L}	0.20	0.20		
I _{DD4RQ}	V _{DDQ}	111.90	121.00		
I _{DD4RDVFSC1}	V _{DD1}	10.00	10.00	mA	3, 4, 6
I _{DD4RDVFSC2H}	V _{DD2H}	32.00	32.00		
I _{DD4RDVFSC2L}	V _{DD2L}	115.00	115.00		
I _{DD4RDVFSCQ}	V _{DDQ}	74.70	74.70		
I _{DD4W1}	V _{DD1}	16.50	18.50	mA	2, 3
I _{DD4W2H}	V _{DD2H}	265.00	280.00		
I _{DD4W2L}	V _{DD2L}	0.20	0.20		
I _{DD4WQ}	V _{DDQ}	0.60	0.60		
I _{DD4WDVFSC1}	V _{DD1}	9.00	9.00	mA	3, 6
I _{DD4WDVFSC2H}	V _{DD2H}	29.00	29.00		
I _{DD4WDVFSC2L}	V _{DD2L}	80.00	80.00		
I _{DD4WDVFSCQ}	V _{DDQ}	0.60	0.60		
I _{DD51}	V _{DD1}	24.00	24.00	mA	2
I _{DD52H}	V _{DD2H}	205.00	205.00		
I _{DD52L}	V _{DD2L}	0.20	0.20		
I _{DD5Q}	V _{DDQ}	0.60	0.60		
I _{DD5ED1}	V _{DD1}	21.00	21.00	mA	6
I _{DD5ED2H}	V _{DD2H}	160.00	160.00		
I _{DD5ED2L}	V _{DD2L}	26.50	26.50		
I _{DD5EDQ}	V _{DDQ}	0.60	0.60		
I _{DD5AB1}	V _{DD1}	3.60	3.60	mA	2
I _{DD5AB2H}	V _{DD2H}	47.00	47.00		
I _{DD5AB2L}	V _{DD2L}	0.20	0.20		
I _{DD5ABQ}	V _{DDQ}	0.60	0.60		

Table 1: I_{DD} Parameters – Single Die

Symbol	Supply	Speed Grade		Unit	Note
		7500 Mb/s	8533 Mb/s		
I _{DD5ABED1}	V _{DD1}	3.40	3.40	mA	6
I _{DD5ABED2H}	V _{DD2H}	24.00	24.00		
I _{DD5ABED2L}	V _{DD2L}	22.00	22.00		
I _{DD5ABEDQ}	V _{DDQ}	0.60	0.60		
I _{DD5PB1}	V _{DD1}	3.60	3.60	mA	2
I _{DD5PB2H}	V _{DD2H}	47.00	47.00		
I _{DD5PB2L}	V _{DD2L}	0.20	0.20		
I _{DD5PBQ}	V _{DDQ}	0.60	0.60		
I _{DD5PBED1}	V _{DD1}	3.40	3.40	mA	6
I _{DD5PBED2H}	V _{DD2H}	24.00	24.00		
I _{DD5PBED2L}	V _{DD2L}	22.00	22.00		
I _{DD5PBEDQ}	V _{DDQ}	0.60	0.60		

- Notes: 1. Published I_{DD} values except I_{DD4RQ} are the maximum I_{DD} values considering the worst-case conditions of process, temperature, and voltage.
2. BG mode. Enhanced DVFS and DVFSQ disabled.
3. BL = 16, DBI disabled.
4. I_{DD4RQ} value is reference only. Typical value. Output load = 5pF; R_{ON} = 40 ohms; T_C = 25°C
5. V_{DD1} = 1.70–1.95V; V_{DD2H} = 1.01–1.12V; V_{DD2L} = 0.87–0.97V; V_{DDQ} = 0.47–0.57V (DVFS disabled)/0.27–0.37V (DVFSQ enabled); T_C = –25°C to +85°C
6. Enhanced DVFS enabled, DVFSQ enabled, 3200 Mb/s, 16B Mode
7. Notes 1 and 5 apply to entire table.

Table 2: Full-Array Power-Down Self Refresh Current – Single Die

Temperature	Symbol	Supply	Value	Unit
25°C	I _{DD61}	V _{DD1}	0.27	mA
	I _{DD62H}	V _{DD2H}	1.00	
	I _{DD62L}	V _{DD2L}	– (See Note 4)	
	I _{DD6Q}	V _{DDQ}	– (See Note 4)	
85°C	I _{DD61}	V _{DD1}	3.70	
	I _{DD62H}	V _{DD2H}	21.00	
	I _{DD62L}	V _{DD2L}	0.20	
	I _{DD6Q}	V _{DDQ}	0.60	

- Notes: 1. I_{DD625°C} is the typical value in the distribution with nominal V_{DD} and a reference-only value. I_{DD685°C} is the maximum I_{DD} guaranteed value considering the worst-case conditions of process, temperature, and voltage.
2. Enhanced DVFS and DVFSQ disabled.
3. V_{DD1} = 1.70–1.95V; V_{DD2H} = 1.01–1.12V; V_{DD2L} = 0.87–0.97V; V_{DDQ} = 0.47–0.57V; T_C = –25°C to +85°C
4. V_{DD2L} and V_{DDQ} power rail are not used during power-down self refresh.