

Features

700V normally-OFF GaN power switch
 High $V_{GS(TH)}$, no need for negative gate drive, and high gate drive tolerance of $\pm 20V$
 Low Q_G and simple gate drive
 Fast switching speed for reduced cross-over loss
 Lowest V_F in reverse conduction among all SiC and GaN FETs for low dead-time loss
 Negligible Q_{RR} for high-efficiency hard-switching bridge-configuration topologies
 RoHS, Pb-free -

Applications

AC-DC converters, DC-DC converters
 QR flyback, ACF, boost PFC, totem pole PFC
 LLC, AHB, HFB
 High efficiency power supplies
 Fast chargers
 Power adaptors
 LED lighting drivers
 Wireless power transfer
 Laser drivers
 TV display

Table 1 Key Performance Parameters at $T_J = 25^\circ C$

Parameters	Values	Units
V_{DSS}	700	V
V_{TDSS}	800	V
$R_{DS(on), typ}$	125	m Ω
Q_G	16	nC
$Q_{OSS} @ 400 V$	42	nC

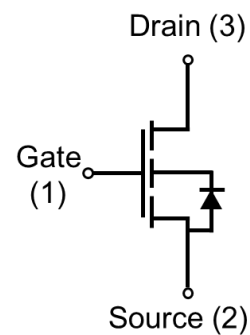
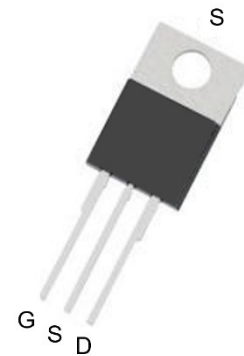


Table 2 Ordering Information

Ordering Code	Package	Marking	Packing
CID15N70C3	TO220-3L	CID15N70	Tube

1 Maximum ratings

at $T_j = 25\text{ °C}$ unless otherwise specified. Continuous application of maximum ratings can deteriorate transistor lifetime.

Table 3 Maximum ratings

Parameters	Sym.	Values			Units	Notes/Test Conditions
		Min.	Typ.	Max.		
Drain-source voltage	V_{DS}	-	-	700	V	$V_{GS} = 0\text{ V}; I_D = 10\text{ }\mu\text{A}$
Drain-source voltage transient ¹	V_{TDSS}	-	-	800	V	$V_{GS} = 0\text{ V}; V_{DS} = 800\text{ V}$
Continuous current, drain-source	I_D	-	-	15.8	A	$T_c = 25\text{ °C}$
		-	-	10	A	$T_c = 100\text{ °C}$
Pulsed current, drain-source ²	$I_{D, \text{ pulse}}$	-	-	49	A	$T_c = 25\text{ °C}$
		-	-	37	A	$T_c = 150\text{ °C}$
Gate-source voltage, continuous	V_{GS}	-20	-	+20	V	$T_j = -55\text{ °C to }150\text{ °C}$
Gate-source voltage, pulsed	$V_{GS, \text{ pulse}}$	-30	-	+30	V	$T_j = -55\text{ °C to }150\text{ °C};$ $t_{\text{Pulse}} = 50\text{ ns}; f > 1\text{ kHz}$
Power dissipation	P_{tot}	-	-	66	W	$T_c = 25\text{ °C}$
Operating temperature	T_j	-55	-	+150	°C	
Storage temperature	T_{stg}	-55	-	+150	°C	

1. Off-state spike duty cycle < 0.01 , spike duration $< 2\text{ }\mu\text{s}$.

2. Pulse width = $100\text{ }\mu\text{s}$.

2 Thermal characteristics

Table 4 Thermal characteristics

Parameters	Sym.	Values			Units	Notes/Test Conditions
		Min.	Typ.	Max.		
Thermal resistance, junction-case	R_{thJC}	-	1.9	-	°C/W	
Thermal resistance, junction-ambient ¹	R_{thJA}	-	50	-	°C/W	
Reflow soldering temperature	T_{sold}	-	-	260	°C	MSL3

1. Device mounted on 1.6 mm PCB thickness FR4, 4-layer PCB with 2 oz copper on each layer. The recommendation for thermal vias under the thermal pad is 0.3 mm diameter (12mil) with 0.889 mm pitch (35mil). The copper layers under the thermal pad and drain pad are $25 \times 25\text{ mm}^2$ each. The PCB is mounted in horizontal position without air stream cooling.

3 Electrical characteristics

at $T_j = 25\text{ }^{\circ}\text{C}$, unless otherwise specified.

Table 5 Static characteristics

Parameters	Sym.	Values			Units	Notes/Test Conditions
		Min.	Typ.	Max.		
Gate threshold voltage	$V_{GS(TH)}$	3.0	4.0	5.0	V	$I_D = 0.5\text{ mA}$; $V_{DS} = V_{GS}$; $T_j = 25\text{ }^{\circ}\text{C}$
$V_{GS(TH)}$ temperature coefficient	$\Delta V_{GS(TH)}/T_j$		-10.7		mV/ $^{\circ}\text{C}$	$I_D = 0.5\text{ mA}$; $V_{DS} = V_{GS}$
Drain-source leakage current	I_{DSS}	-	8	20	μA	$V_{DS} = 700\text{ V}$; $V_{GS} = 0\text{ V}$; $T_j = 25\text{ }^{\circ}\text{C}$
		-	50	-		$V_{DS} = 700\text{ V}$; $V_{GS} = 0\text{ V}$; $T_j = 150\text{ }^{\circ}\text{C}$
Gate-source leakage current	I_{GSS}	-	-	150	nA	$V_{GS} = 20\text{ V}$; $V_{DS} = 0\text{ V}$
Reverse Gate leakage current	I_{RGL}	-	-	-150	nA	$V_{GS} = -20\text{ V}$; $V_{DS} = 0\text{ V}$
Drain-source on-state resistance ¹	$R_{DS(on)}$	-	125	160	m Ω	$V_{GS} = 12\text{ V}$; $I_D = 4\text{ A}$; $T_j = 25\text{ }^{\circ}\text{C}$
		-	250	-	m Ω	$V_{GS} = 12\text{ V}$; $I_D = 4\text{ A}$; $T_j = 150\text{ }^{\circ}\text{C}$

1. Dynamic on-resistance

Table 6 Dynamic characteristics

Parameters	Sym.	Values			Units	Notes/Test Conditions
		Min.	Typ.	Max.		
Input capacitance	C_{iss}	-	505	-	pF	$V_{GS} = 0\text{ V}$; $V_{DS} = 400\text{ V}$; $f = 1\text{ MHz}$
Output capacitance	C_{oss}	-	30	-	pF	$V_{GS} = 0\text{ V}$; $V_{DS} = 400\text{ V}$; $f = 1\text{ MHz}$
Reverse transfer capacitance	C_{rss}	-	0.8	-	pF	$V_{GS} = 0\text{ V}$; $V_{DS} = 400\text{ V}$; $f = 1\text{ MHz}$
Effective output capacitance, energy related ¹	$C_{o(er)}$	-	48	-	pF	$V_{GS} = 0\text{ V}$; $V_{DS} = 0\text{ to }400\text{ V}$
Effective output capacitance, time related ²	$C_{o(tr)}$	-	106	-	pF	$V_{GS} = 0\text{ V}$; $V_{DS} = 0\text{ to }400\text{ V}$
Output charge	Q_{oss}	-	42	-	nC	$V_{GS} = 0\text{ V}$; $V_{DS} = 400\text{ V}$; $f = 1\text{ MHz}$
Output capacitance stored energy	E_{oss}	-	3.8	-	μJ	
Turn-on delay time	$t_{d(on)}$	-	44	-	ns	$V_{DS} = 400\text{ V}$; $I_D = 10\text{ A}$; $L = 120\text{ }\mu\text{H}$; $V_{GS} = 12\text{ V}$; $R_G = 40\text{ }\Omega$
Turn-off delay time	$t_{d(off)}$	-	40	-	ns	
Rise time	t_r	-	16	-	ns	
Fall time	t_f	-	12	-	ns	

1. $C_{o(er)}$ is the fixed capacitance that gives the same stored energy as C_{oss} while V_{DS} is rising from 0 to 400 V.

2. $C_{o(tr)}$ is the fixed capacitance that gives the same charging time as C_{oss} while V_{DS} is rising from 0 to 400 V.

Table 7 Gate charge characteristics

Parameters	Sym.	Values			Units	Notes/Test Conditions
		Min.	Typ.	Max.		
Gate charge	Q_G	-	16	-	nC	$V_{GS} = 0$ to 12 V; $V_{DS} = 400$ V; $I_D = 6$ A
Gate-source charge	Q_{GS}	-	4.8	-	nC	
Gate-drain charge	Q_{GD}	-	4.4	-	nC	
Gate plateau voltage	V_{plat}	-	5.0	-	V	$V_{DS} = 400$ V; $I_D = 9$ A

Table 8 Reverse conduction characteristics

Parameters	Sym.	Values			Units	Notes/Test Conditions
		Min.	Typ.	Max.		
Source-drain reverse voltage	V_{SD}	-	1.4	-	V	$V_{GS} = 0$ V; $I_{SD} = 5$ A; $T_J = 25$ °C
		-	2	-	V	$V_{GS} = 0$ V; $I_{SD} = 10$ A; $T_J = 25$ °C
		-	2.8	-	V	$V_{GS} = 0$ V; $I_{SD} = 10$ A; $T_J = 150$ °C
Reverse recovery time	t_{rr}	-	21	-	ns	$I_S = 9$ A, $V_{GS} = 0$ V, $di/dt = 1000$ A/ μ s, $V_{DS} = 400$ V
Reverse recovery charge ¹	Q_{rr}	-	0	-	nC	

1. Excluding Q_{OSS}

4 Electrical characteristics diagrams

at $T_j = 25\text{ }^{\circ}\text{C}$, unless otherwise specified.

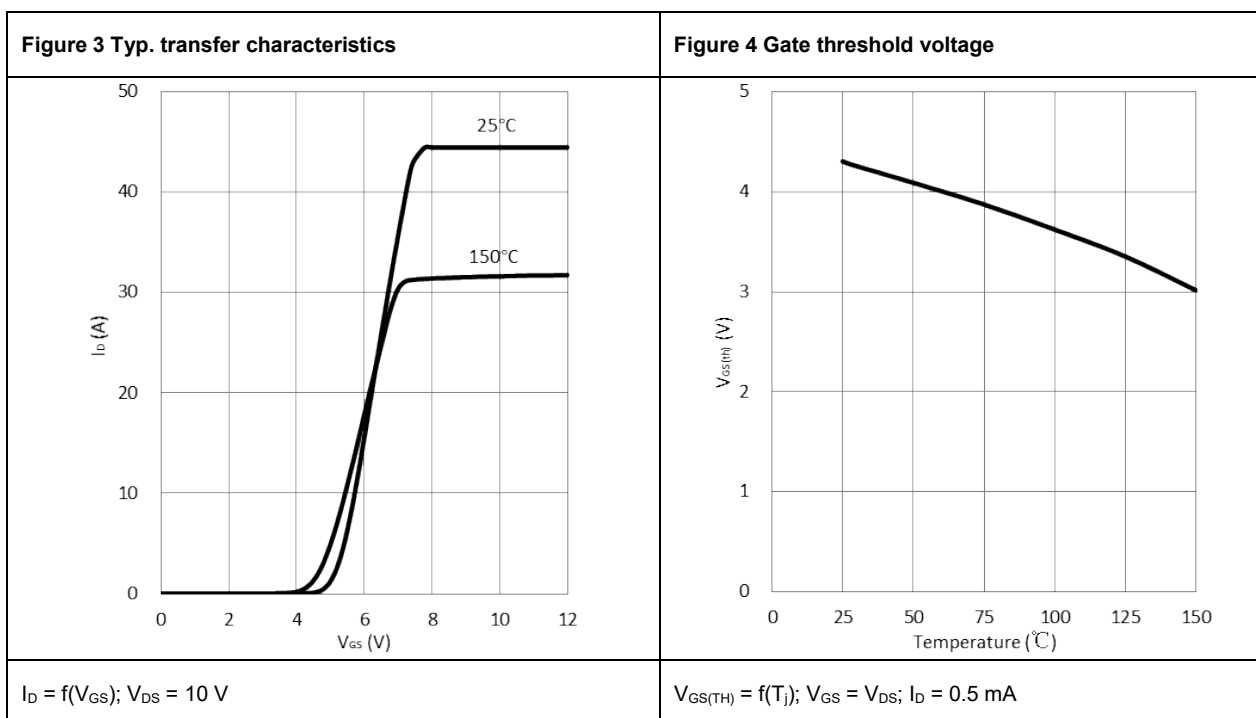
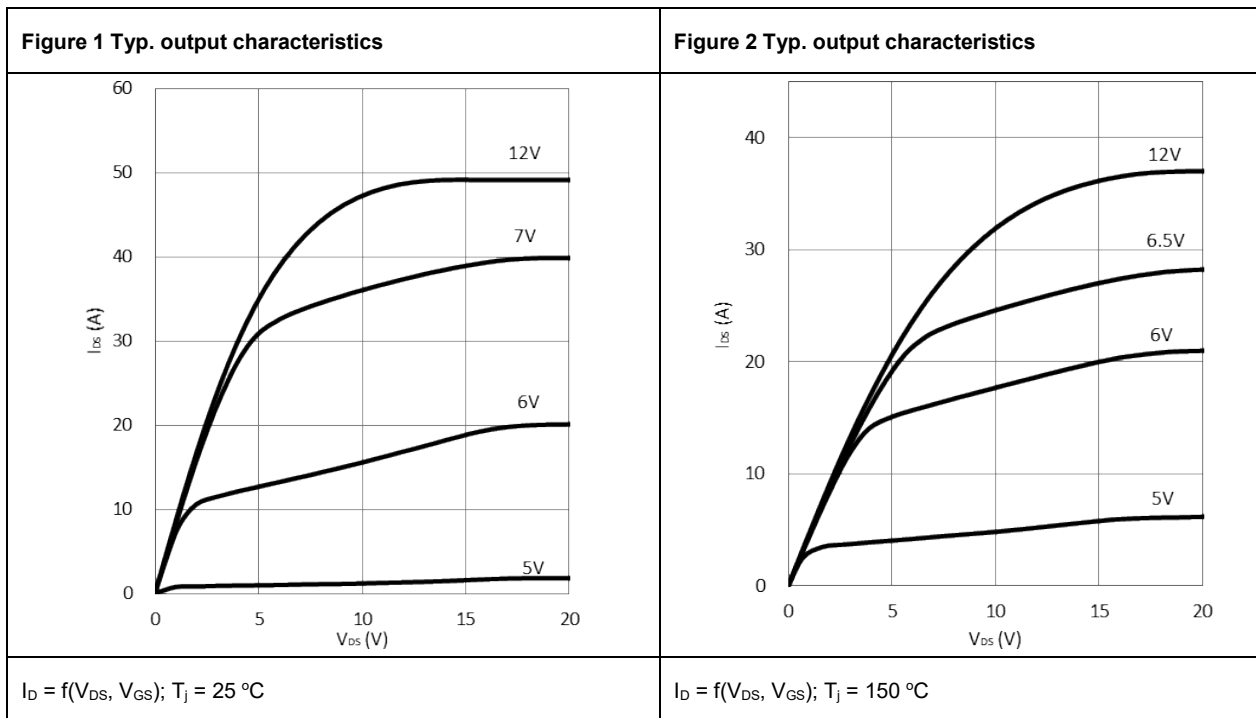
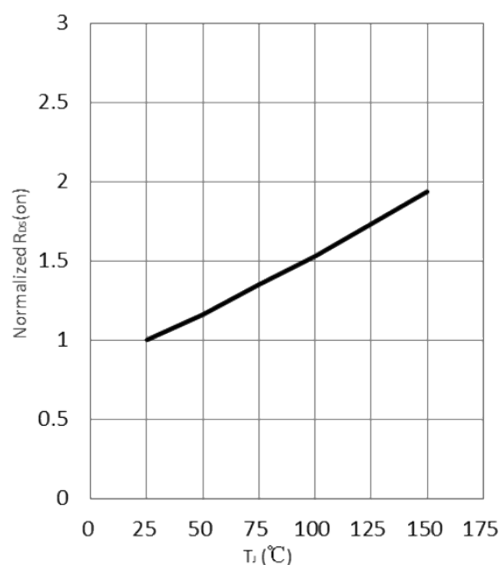
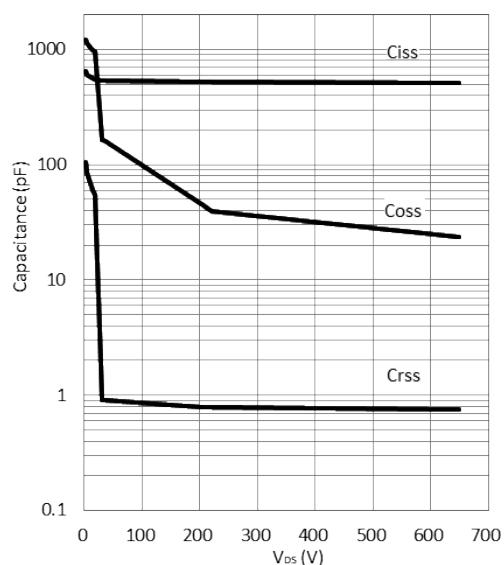


Figure 5 Drain-source on-state resistance



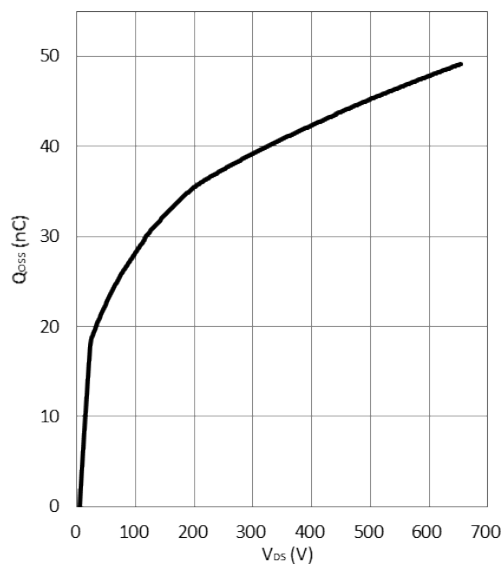
$$R_{DS(on)} = f(T_J); I_D = 4 \text{ A}; V_{GS} = 12 \text{ V}$$

Figure 6 Typ. capacitances



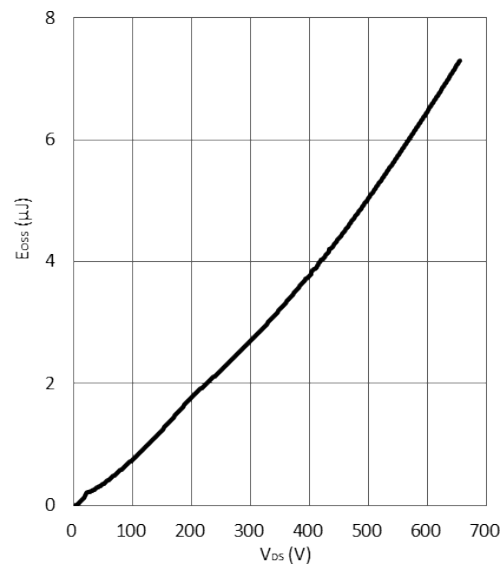
$$C_{XSS} = f(V_{DS}); \text{Freq.} = 1 \text{ MHz}$$

Figure 7 Typ. output charge



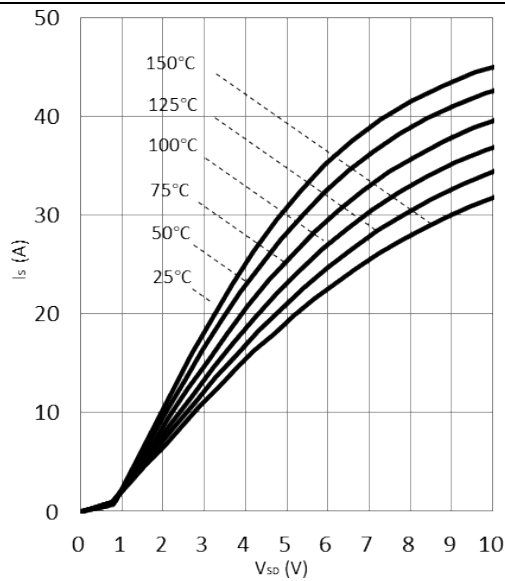
$$Q_{OSS} = f(V_{DS}); \text{Freq.} = 1 \text{ MHz}$$

Figure 8 C_oss stored energy



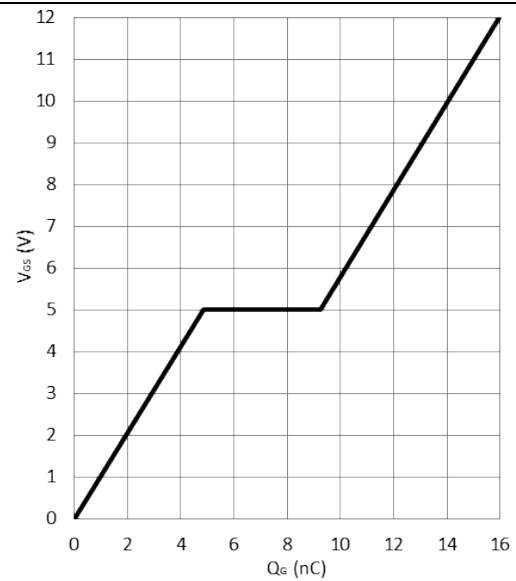
$$E_{OSS} = f(V_{DS}); \text{Freq.} = 1 \text{ MHz}$$

Figure 9 Reverse conduction characteristics



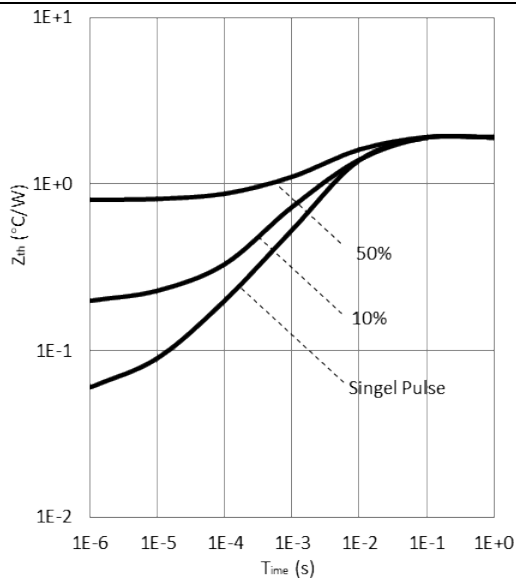
$$I_S = f(V_{SD})$$

Figure 10 Typ. gate charge



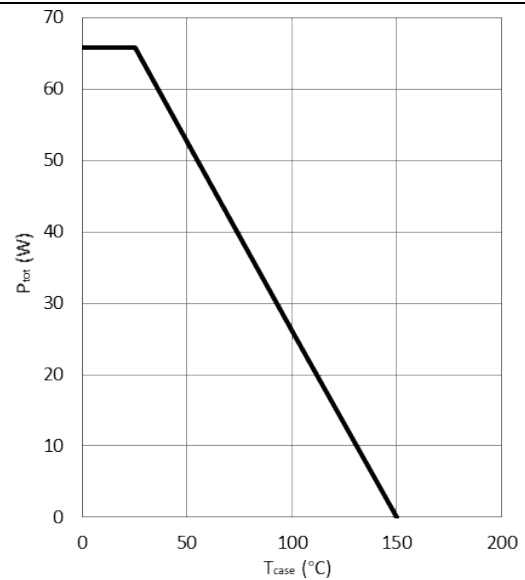
$$V_{GS} = f(Q_G); V_{DS} = 400 \text{ V}; I_D = 9 \text{ A}$$

Figure 11 Max. transient thermal impedance



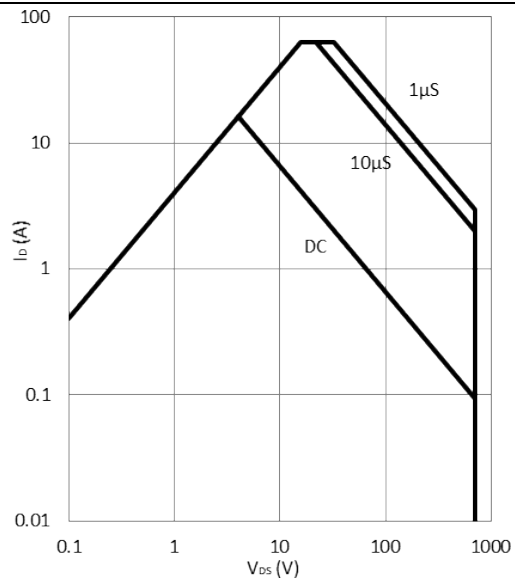
$$Z_{thJC} = f(t_p, D)$$

Figure 12 Power dissipation



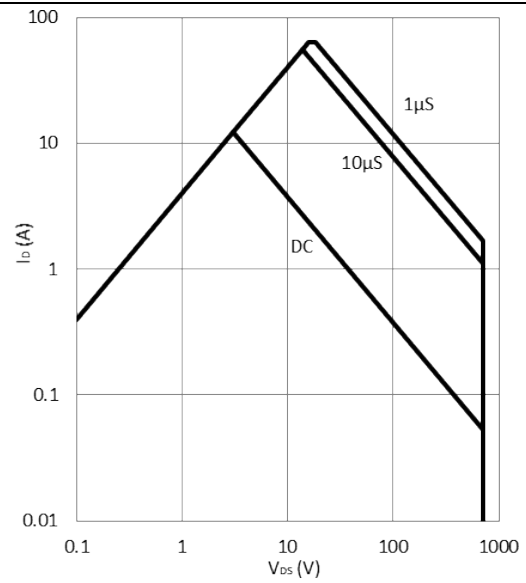
$$P_{tot} = f(T_C)$$

Figure 13 Safe operating area



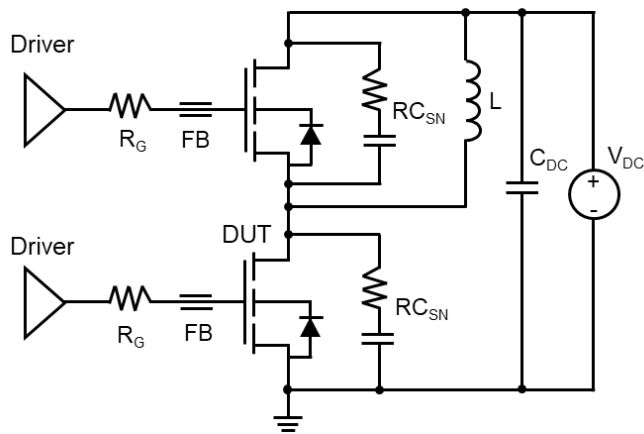
$$Z_{thJC} = f(t_P, D), T_C = 25\text{ }^{\circ}\text{C}$$

Figure 14 Safe operating area



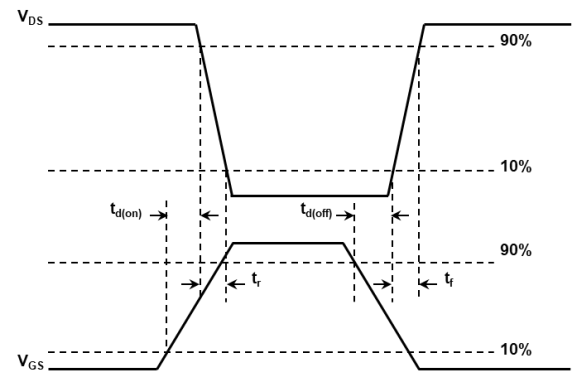
$$Z_{thJC} = f(t_P, D), T_C = 80\text{ }^{\circ}\text{C}$$

Figure 15 Switching time test circuit



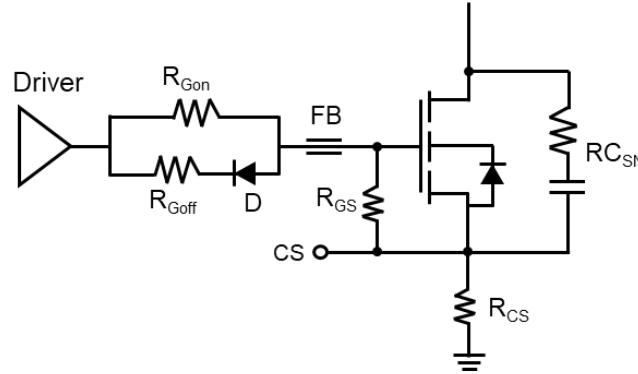
$$V_{DS} = 400\text{ V}, I_D = 10\text{ A}, L = 120\text{ }\mu\text{H}, V_{GS} = 0\text{ to }12\text{ V}, R_G = 40\text{ }\Omega$$

Figure 16 Typ. switching time waveform



5 Circuit implementations

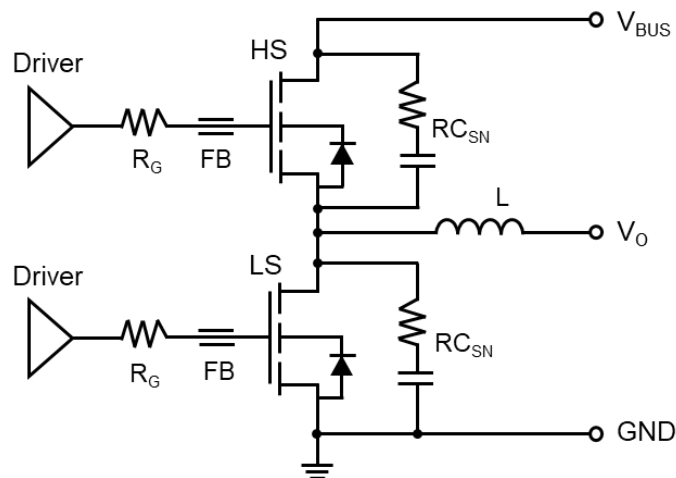
(1) Mostly used in flyback, forward and push-pull converters:



Recommended gate drive: (0 V, 12 V) with $R_{Gon} = 300 - 500 \Omega$, $R_{Goff} = 10 \Omega$

Gate ferrite bead (FB)	Gate-source resistance (R _{GS})	Gate diode (D)
300 - 600 Ω @ 100MHz	10 k Ω	1N4148

(2) Mostly used in half bridge and full bridge topologies:



Recommended gate drive: (0 V, 8 V) with $R_{G(tot)} = 40 \Omega$, where $R_{G(tot)} = R_G + R_{driver}$

Gate ferrite bead (FB)	Gate resistance (R _G)	RC snubber (R _{CSN})
MPZ1608S471ATA00	33 Ω	69 pF + 15 Ω

Notes:

- R_{CSN} should be placed as close as possible to the drain pin
- The layout and wiring of the drive circuit should be as short as possible

6 Package outlines

Symbol	Values (mm)	
	MIN	MAX
A	4.30	4.80
A1	1.20	1.45
A2	2.20	2.90
b	0.69	0.95
b2	1.00	1.60
c	0.33	0.65
D	14.70	16.20
D1	8.59	9.65
D2	11.75	13.60
e	2.54BSC	
E	9.60	10.60
E1	7.00	8.46
H1	6.20	7.00
L	12.60	14.80
L1	2.70	3.80
L2	12.13	16.50
Q	2.40	3.10
P	3.50	3.90

7 Tube information

