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Nyfea product specification

PRODUCT SPECIFICATION

Customer : _____

Product Name : 8-Bit I/O Expander for 12C Bus

Part NO : FCA8574

Issue Date : _____

Prepared	Checked	Customer Check
ChenTT	Zelig	

NYFEA

1 Features

- Alternative to xCF8574
- Supply Range: 1.6V to 5.5V
- Temperature Range: - 40°C to + 85°C
- Standby Current: 0.5μA
- High-Current Drive Capability
- Open-Drain Active-Low Interrupt Output

2 Applications

- Servers
- Routers
- Communication Cabinet
- Industrial Automation
- Products with GPIO-Limited Processors

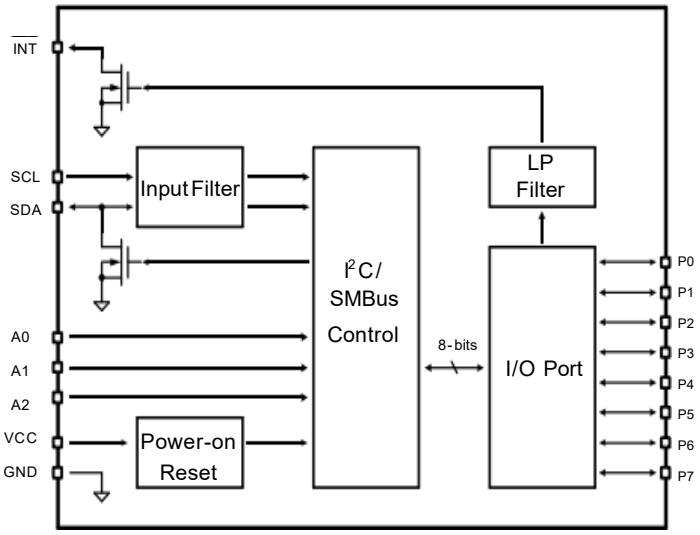
3 Description

FCA8574 provides general purpose parallel input and output (GPIO) expansion. Port data is transmitted through the standard two-wire I²C protocol, and can support a communication rate of up to 1MHz (up to 2MHz after turning on the high-speed mode).

FCA8574 features 8-bit quasi-bidirectional GPIO ports that can directly drive LEDs. Each GPIO port can be used as an input or output port independently without any direction control signal.

4 Package Information

PART NUMBER	PACKAGE	BODY SIZE
FCA8574T	TSSOP (20)	6.50 mm x 4.40
FCA8574Q	WQFN (16)	3.00 mm x 3.00
FCA8574S	SOW (16)	10.30 mm x 7.50



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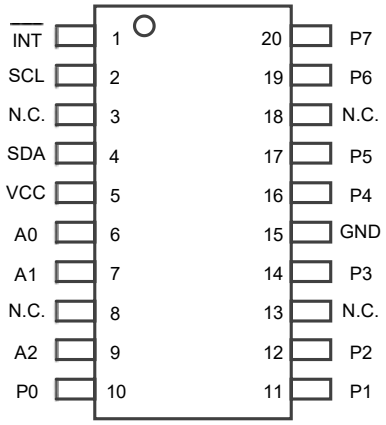
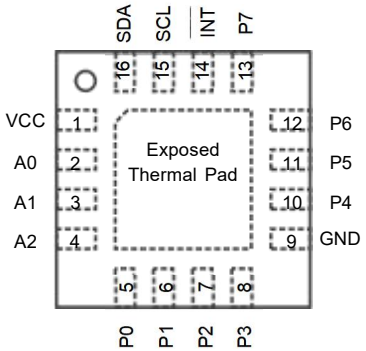
Contents

5 Pin Configuration

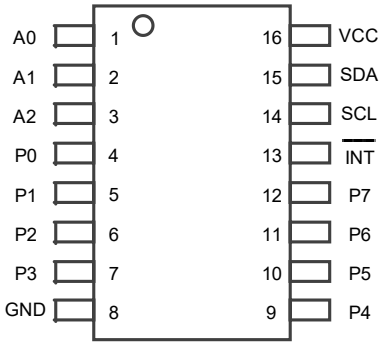
FCA8574T
Top View
TSSOP-20



FCA8574Q
Top View
WQFN-16



FCA8574S
Top View
SOW-16



PIN				DESCRIPTION
NAME	TSSOP-20	WQFN-16	SOW-16	
A0	6	2	1	Address input 0. Connect directly to VCC or GND.
A1	7	3	2	Address input 1. Connect directly to VCC or GND.
A2	9	4	3	Address input 2. Connect directly to VCC or GND.
GND	15	9	8	Ground.
INT	1	14	13	Interrupt open-drain output. Connect to VCC through a pull-up
N.C.	3, 8, 13, 18	-	-	No connection.
P0	10	5	4	P-port I/O.
P1	11	6	5	P-port I/O.
P2	12	7	6	P-port I/O.
P3	14	8	7	P-port I/O.
P4	16	10		P-port I/O.
P5	17	11		P-port I/O.
P6	19	12		P-port I/O.
P7	20	13		P-port I/O.
SCL	2	15		Serial clock bus. Connect to VCC through a pull-up resistor.
SDA	4	16		Serial data bus. Connect to VCC through a pull-up resistor.
VCC	5	1		Supply voltage. Recommended to add an 1uF filter capacitor.

6 Specifications

6.1 Absolute Maximum Ratings

Over operating free-air temperature range (unless otherwise noted)

	MIN	MAX	UNIT
Input Voltage	- 0.5	+ 6	V
Storage Temperature	- 65	+ 150	°C
Input/output Clamp Current		±20	mA
Continuous Output Low Current		+ 50	mA
Continuous Output High Current		- 4	mA
Continuous Current Flowing Through VCC or GND		± 100	mA

Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device.

6.2 ESD Ratings

		VALUE	UNIT
Electrostatic Discharge	Human Body Mode (HBM), per ANSI/ESDA/JEDEC JS-001	±8000	V

6.3 Electrical Characteristics

Over temperature range of -40~+85°C and supply range of 1.6~5.5V, unless otherwise noted. Typical values at +25°C and 3.3V.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Supply Voltage, V_{CC}		1.6	3.3	5.5	V
Operating Temperature, T_A		- 40		85	°C
Quiescent Current, I_{CC}			0.5	5	μA
P-port pullup current, I_{OH}	V_{OH} = GND, V_{CC} = 2.5V~5.5V	30	50	300	μA
P-port transient pullup current, I_{OHT}	V_{OH} = GND, during ACK		1		mA
P-port pulldown current, I_{OL}	V_{OL} = 1.0V, V_{CC} = 5.0V	10	25		mA
SDA pulldown current, I_{OL}	V_{OL} = 0.4V, V_{CC} = 2.5V~5.5V	3			mA
INT pulldown current, I_{OL}	V_{OL} = 0.4V, V_{CC} = 2.5V~5.5V	3			mA
Input current, I_I	V_I = V_{CC} or GND			± 1	μA

6.4 Switching Characteristics

Over temperature range of -40~+125°C and supply range of 1.6~5.5V, unless otherwise noted. Typical values at +25°C and 3.3V.

PARAMETER	FROM	TO	MIN	TYP	MAX	UINIT
Output data valid time, t_{pv}	SCL	P port			4	μs
Input data setup time, t_{su}	P port	SCL		0		μs
Input data hold time, t_h	P port	SCL		4		μs
Interrupt effective time, t_{iv}	P port	INT			4	μs
Interrupt reset delay, t_{ir}	SCL	INT			4	μs

7 Detailed Description

7.1 Port Structure

The simplified circuit of the general purpose input/output (GPIO) is shown in Figure 1, which consists of a weak pull current path (100uA) and a strong sink current path (25mA). This structure can be used as an input or output port without any direction control signal. If used as an input, the port must be written with data 1.

When writing data 0 to the I/O port through the I²C interface, transistor Q2 is turned on, while Q1 and Q3 are turned off. At this time, the pull-down path is turned on and provides sufficient sink current to drive LED. When writing data 1 to the I/O port through the I²C interface, transistor Q2 is turned off while Q1 and Q3 are turned on. Q3 is an additional auxiliary for strong current path (1mA) to provide a fast-rising edge when driving heavy loads. Transistor Q3 is turned on only during the Ack period of I²C writing sequence.

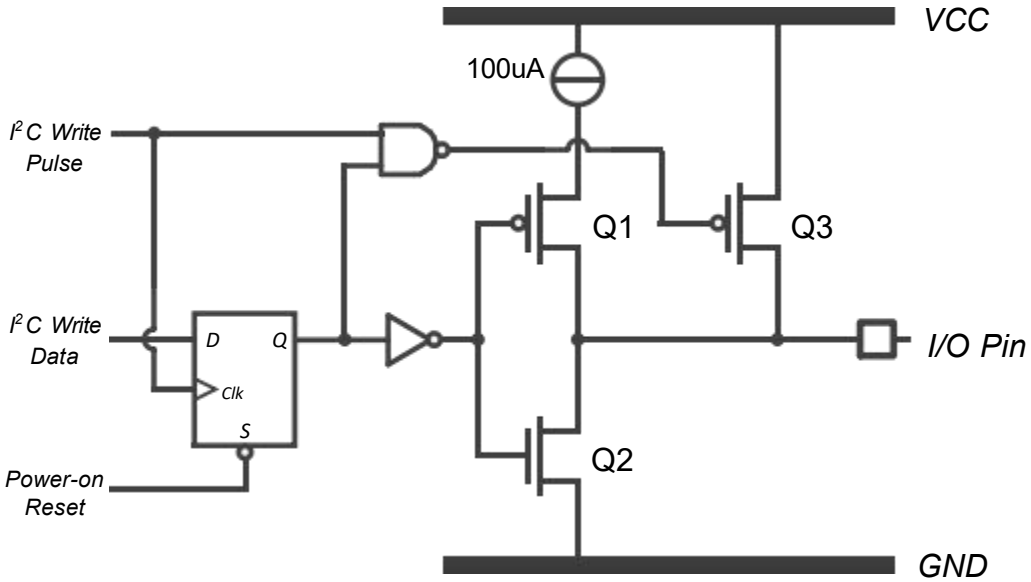


Figure 1. Simplified Circuit Diagram of General Purpose Input/Output (GPIO)

7.2 Serial Interface

7.2.1 Bus Overview

I2C/SMBus is a two-wire serial communication interface supporting multi-master and multi-slave. The device that initiates the communication is called the *master*, and the device controlled by the master is called the *slave*. The master is responsible for generating the serial clock (SCL) and controlling the bus access.

Data transfer is sent over eight clock pulses followed by an acknowledge bit. During data transfer, SDA must remain stable when SCL is high because any change in SDA while SCL is high is interpreted as a START or STOP conditions. Parameters for Figure 2 are defined in Table 1.

Table 1. Timing Diagram Requirements

SYMBOL	PARAMETER	FAST MODE		HIGH-SPEED MODE		UNIT
		MIN	MAX	MIN	MAX	
f_{SCL}	SCL operating frequency	1	400	1	2000	kHz
$t_{SU:STA}$	Repeated START condition setup time	0.6	-	0.26	-	us
$t_{HD:STA}$	Repeated START condition hold time	0.6	-	0.26	-	us
$t_{SU:STO}$	STOP condition setup time	0.6	-	0.26	-	us
t_{BUF}	Bus free time between STOP and START	1.3	-	0.5	-	us
$t_{SU:DAT}$	Data setup time	0.1	-	0.05	-	us
$t_{HD:DAT}$	Data hold time	0	-	0	-	us
t_{HIG}	SCL clock high period	0.6	-	0.26	-	us
t_{LOW}	SCL clock low period	1.3	-	0.5	-	us
t_R	Clock and data rise time	-	300	-	120	ns
t_F	Clock and data fall time	-	300	-	120	ns

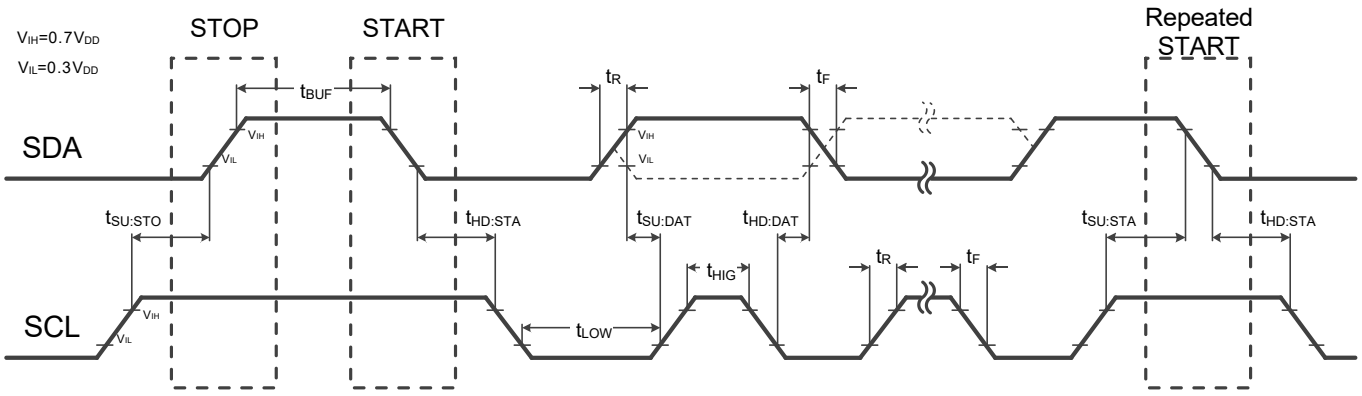


Figure 2. Two-Wire Timing Diagram

7.2.2 Slave Address

FCA8574 has 3 hardware address pins (A2/A1/A0), which allow users to select the slave address of the chip. The corresponding reference is shown in Table 2. The logic level of the pin must always remain unchanged during a communication process, otherwise it may cause communication failure. The address pin must be connected to VCC or GND and cannot be in a float state, otherwise it will cause communication failure and the chip will show an abnormal standby current more than 1uA.

The slave address byte consists of 7 address bits and 1 read/write flag bit. The read/write flag bit indicates the data transmission direction. 0b represents write operation; 1b represents read operation. The transmission of communication data starts from the highest bit of the byte.

Table 2. Slave Address Reference

A2	A1	A0	Slave Address
GND	GND	GND	0x40 (write), 0x41 (read)
GND	GND	VCC	0x42 (write), 0x43 (read)
GND	VCC	GND	0x44 (write), 0x45 (read)
GND	VCC	VCC	0x46 (write), 0x47 (read)
VCC	GND	GND	0x48 (write), 0x49 (read)
VCC	GND	VCC	0x4A (write), 0x4B (read)
VCC	VCC	GND	0x4C (write), 0x4D (read)
VCC	VCC	VCC	0x4E (write), 0x4F (read)

7.2.3 Read and Write Operations

GPIO output can be achieved by writing data to FCA8574. Starting from the slave address byte with the R/$\overline{W}$ bit low, each subsequent byte represents the data to be output to the GPIO port. FCA8574 refreshes the received data byte to the GPIO port at the rising edge of SCL of the Ack bit of each data byte, and samples the GPIO port at the falling edge of SCL immediately following it to ensure that the write data does not trigger an interrupt signal. Taking the continuous writing of two bytes as an example, the specific timing is shown in Figure 3, and the shaded part represents that the slave is controlling the SDA bus.

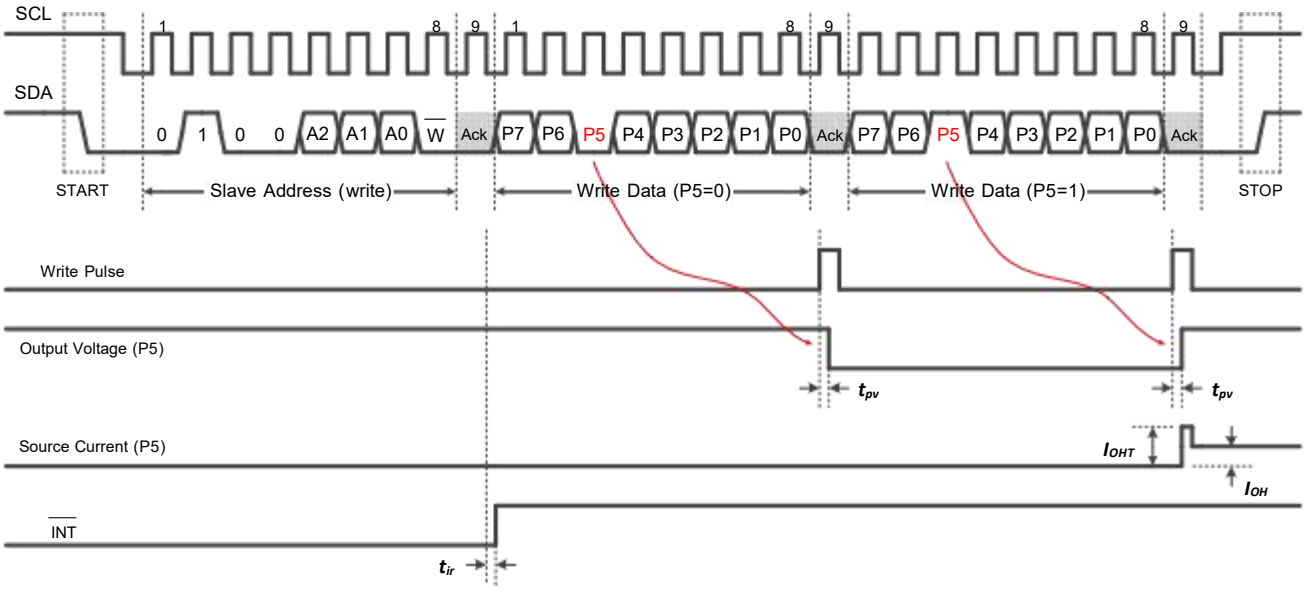


Figure 3. Timing Diagram of Write Sequence

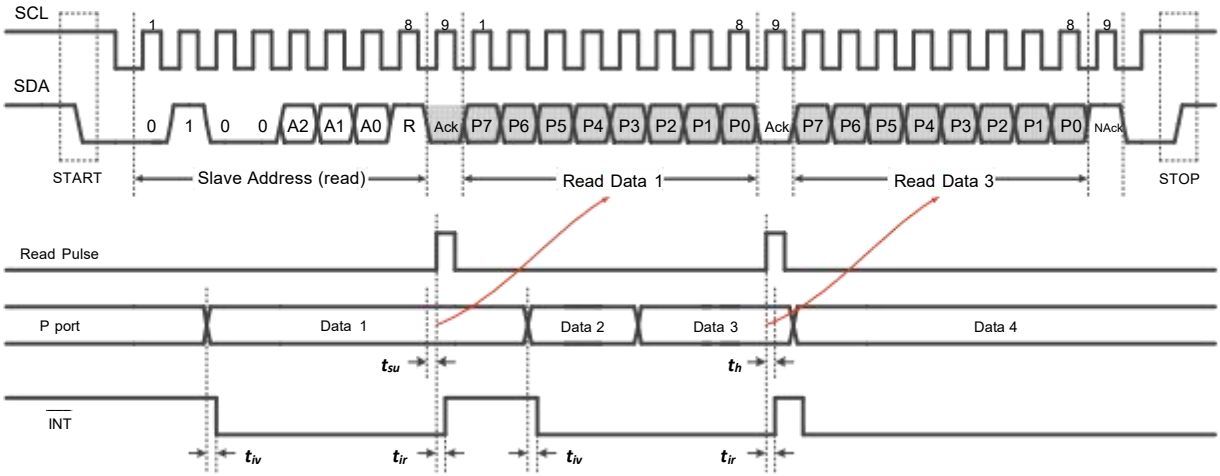


Figure 4. Timing Diagram of Read Sequence

GPIO input can be achieved by reading data from FCA8574. Starting from the slave address byte with the R/$\overline{W}$ bit high, each subsequent byte represents the data sampled from the GPIO port. FCA8574 samples the GPIO port at the rising edge of SCL of the address byte and the Ack bit of each data byte, thereby clearing the interrupt signal. However, it should be noted that when the host sends the NAck bit, FCA8574 will not sample the GPIO port, so the interrupt signal will not be cleared. Taking the continuous reading of two bytes as an example, the specific timing is shown in Figure 4, and the shaded part represents that the slave is controlling the SDA bus.

Note: When a GPIO port is used as an input port, data 1 must be written to the port first.

7.2.4 High-Speed Mode

If the host sends a high-speed mode code (0000 1xxxb) after the start condition, the chip will not answer the byte, but will switch the input and output filters of the SDA and SCL pins to high-speed mode, allowing the bus to transmit data at a communication frequency of up to 2MHz. The chip will continue to operate in high-speed mode until STOP appears on the bus. Once STOP is received, the chip will switch the input and output filters back to standard mode.

7.3 Interrupt Output

FCA8574 provides an open-drain interrupt pin that can be directly connected to the interrupt input of a microprocessor. By sending an interrupt signal, the chip can actively notify the microprocessor if the logic level of the remote I/O pin has changed.

There are three key points to note about setting and clearing interrupt signals:

- Only external changes will cause the interrupt signal to be set, that is, writing data will not cause an interrupt;
- The interrupt signal will not be latched. If the I/O pin logic level returns to the state at the last sampling moment, the interrupt signal will be cleared immediately;
- Interrupt signal assertions that occur close to the Ack bit may be lost.

8 Application and Implementation

NOTE

The following contents are notes and suggestions for the use of FCA8574, and NYFEA does not warrant its accuracy or completeness. Customers are responsible for determing suitability of components for their purpose, as well as validating and testing their design implementation to confirm system functionality.

8.1 Quick Feature Guide

Table 5. Selection Table

DEVICE	TYPE	I/O	ADDRESS	BUILT-IN PULLUP	RESET INPUT
FCA8574	Quasi bi-dir.	8	0100 xxxb		
FCA9534	Totem-pole	8	0100 xxxb		
FCA9538	Totem-pole	8	1110 0xxb		√
FCA9554	Totem-pole	8	0100 xxxb	√	
FCA9535	Totem-pole	16	0100 xxxb		
FCA9539	Totem-pole	16	1110 1xxb		√
FCA9555	Totem-pole	16	0100 xxxb	√	

8.2 High Current-Drive Load Application

The I/O pins of the FCA8574 are capable of driving with a minimum perfusion current of 10 mA. Additionally, it is possible to connect multiple I/O pins together through short-wiring in order to enhance the current-driven capability. As illustrated in Figure 5, individual current limiting resistors are necessary for each I/O pin and proper synchronization of switches is required to prevent any potential damage to the chip.

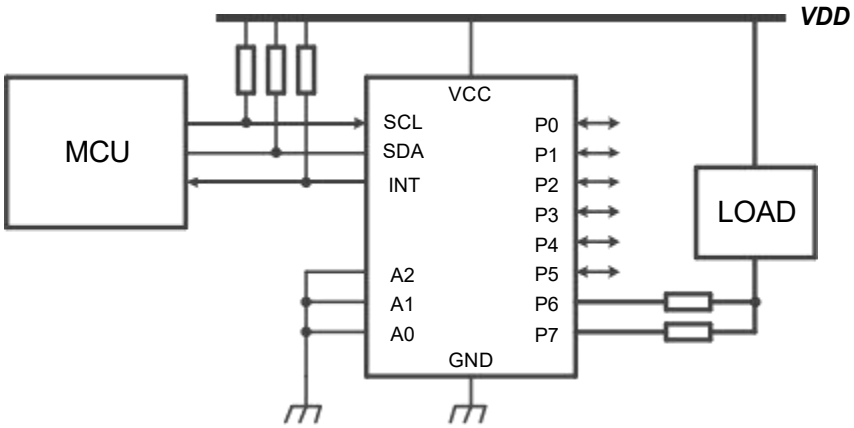
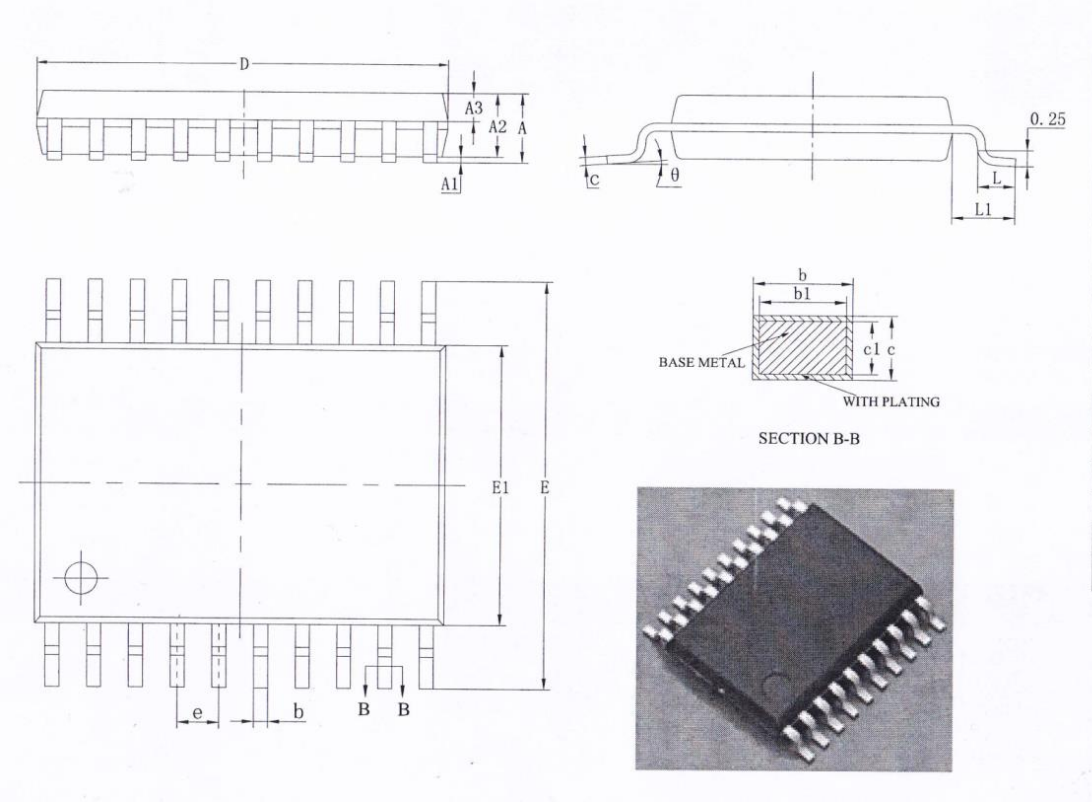


Figure 5. High Current-Drive Load Application

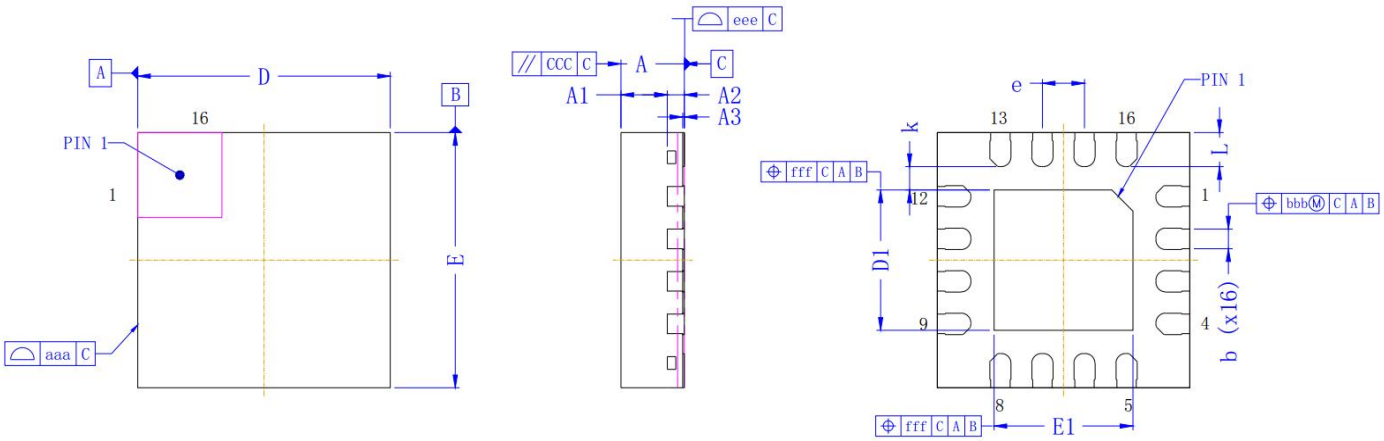
9 Packaging Information

9.1 Package Size (TSSOP-20)



SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	—	—	1.20
A1	0.05	—	0.15
A2	0.80	1.00	1.05
A3	0.39	0.44	0.49
b	0.20	—	0.28
b1	0.19	0.22	0.25
c	0.13	—	0.17
c1	0.12	0.13	0.14
D	6.40	6.50	6.60
E1	4.30	4.40	4.50
E	6.20	6.40	6.60
e	0.65BSC		
L	0.45	0.60	0.75
L1	1.00REF		
θ	0	—	8°

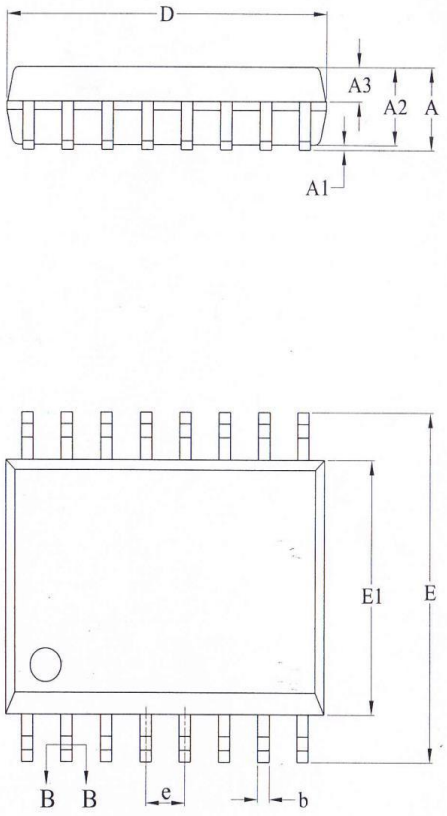
9.2 Package size (WQFN-16)

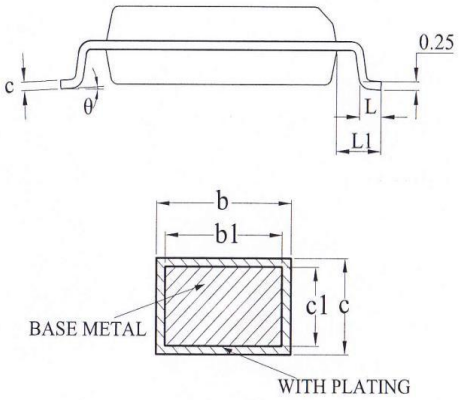


TOP VIEW SIDE VIEW BOTTOM VIEW

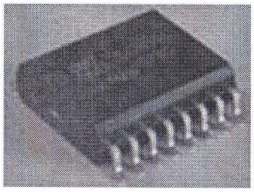
Item		Symbol	Minimum	Normal	Maximum
Body Size	X	D		3.0 BSC	
	Y	E		3.0 BSC	
Exposed Pad Size	X	D1	1.55	1.65	1.75
	Y	E1	1.55	1.65	1.75
Total Thickness		A	0.7	0.75	0.8
Molding Thickness		A1		0.55	
LF Thickness		A2		0.203 REF	
Stand Off		A3	0	0.02	0.05
Lead Width		b	0.20	0.25	0.30
Lead Length		L	0.3	0.4	0.5
Lead Pitch		e		0.5 BSC	
The space from terminals of lead to exposed pad		k		0.2 MIN	
Package Edge Tolerance		aaa		0.1	
Lead Offset		bbb		0.07	
Molding Flatness		ccc		0.1	
Coplanarity		eee		0.08	
Exposed Pad Offset		fff		0.1	

9.3 Package Size (SOW-16)



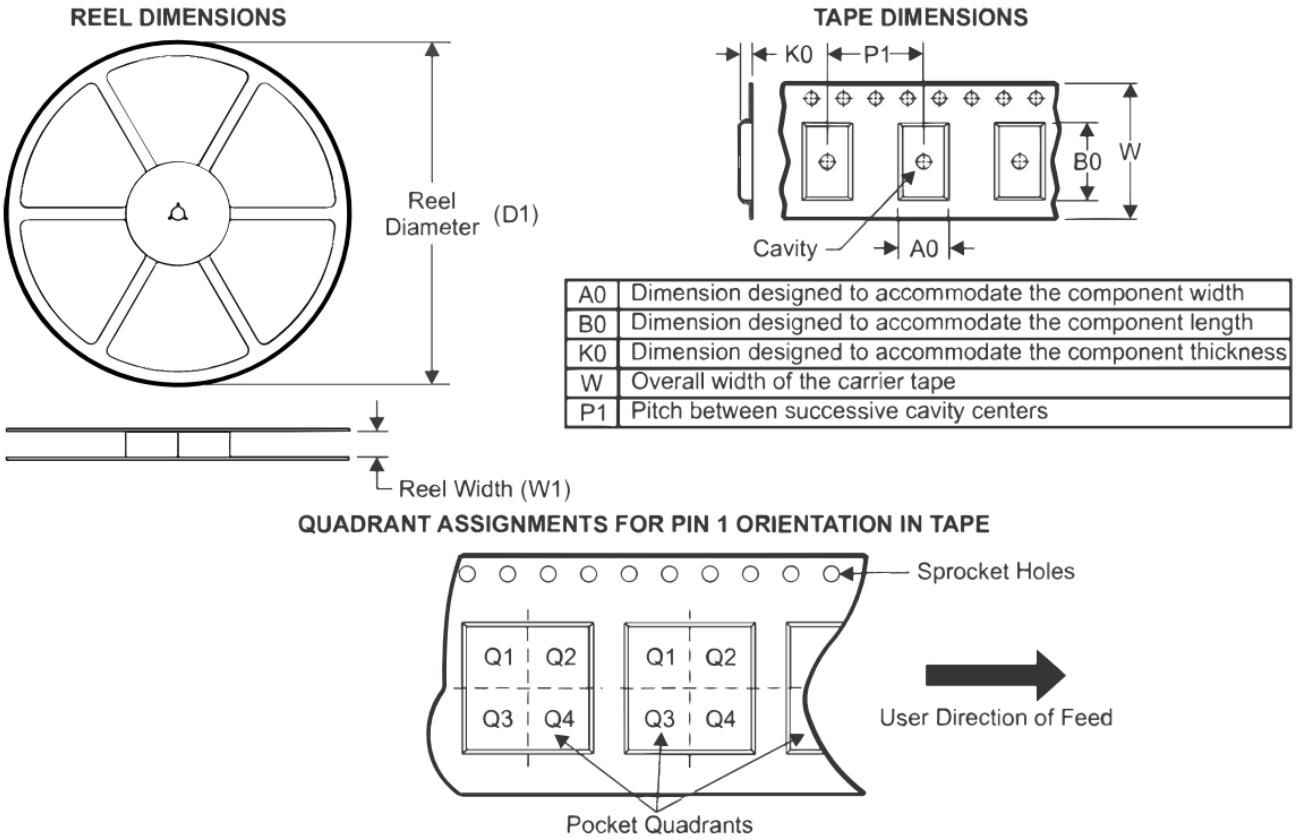


SECTION B-B



SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	—	—	2.65
A1	0.10	—	0.30
A2	2.25	2.30	2.35
A3	0.97	1.02	1.07
b	0.35	—	0.43
b1	0.34	0.37	0.40
c	0.25	—	0.29
c1	0.24	0.25	0.26
D	10.20	10.30	10.40
E	10.10	10.30	10.50
E1	7.40	7.50	7.60
e	1.27BSC		
L	0.55	—	0.85
L1	1.40REF		
θ	0	—	8°

9.4 Reel and Tape Information



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

PACKAGE	D1 (mm)	W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1
TSSOP (20)	330	16.4	6.80	6.90	1.50	8.00	16.00	Q1
WQFN (16)	180	13.2	3.20	3.20	1.05	4.00	12.00	Q1
SOW (16)	330	16.4	10.90	10.80	3.00	12.00	16.00	Q1

Note: All the above dimensions are in millimeters.

10 Ordering Information

ORDER CODE	DEVICE	PACKAGE	QUANTITY	NOTES
FCA8574T-T&R	FCA8574T	TSSOP (20)	4500	Tape&Reel
FCA8574Q-T&R	FCA8574Q	WQFN (16)	3000	Tape&Reel
FCA8574S-T&R	FCA8574S	SOW (16)	1500	Tape&Reel