

General Description

The SQ27695TOD develops a high efficiency, peak current mode controlled, asynchronous step-down DC/DC converter capable of delivering 5A output current. The SQ27695TOD operates over a wide input voltage range from 4.5V to 60V and integrates a main switch with very low $R_{DS(ON)}$ to minimize the conduction loss.

The switching frequency is adjustable from 100kHz to 2.5MHz using an external resistor. And the SQ27695TOD features cycle by cycle peak current limit, UVLO, UVP, OVP and OTP protection.

The SQ27695TOD is available in DFN4×4-10 package.

Features

- Wide Input Voltage Range: 4.5V ~ 60V
- Output Current Capability: 5A
- Low $R_{DS(ON)}$ for Internal N-Channel Power FET (TOP): 95mΩ
- Accurate Feedback Set Point: 0.8V $\pm$ 1% from -40°C to 125°C
- Adjustable Switching Frequency: 100kHz to 2500kHz
- High Efficiency at Light Loads with Pulse Skipping Mode
- Cycle by Cycle Peak Current Limit Protection
- Automatic Recovery for UVLO, OVP and OTP Conditions
- Hiccup Mode for UVP Condition
- Internal and Adjustable Soft-Start Limits Inrush Current
- Power Good Output Monitor for Under-Voltage and Over-Voltage
- Compact Package: DFN4×4-10

Applications

- 5G AAU/RRU
- Industrial
- High-Voltage DC-DC Converters

Typical Applications

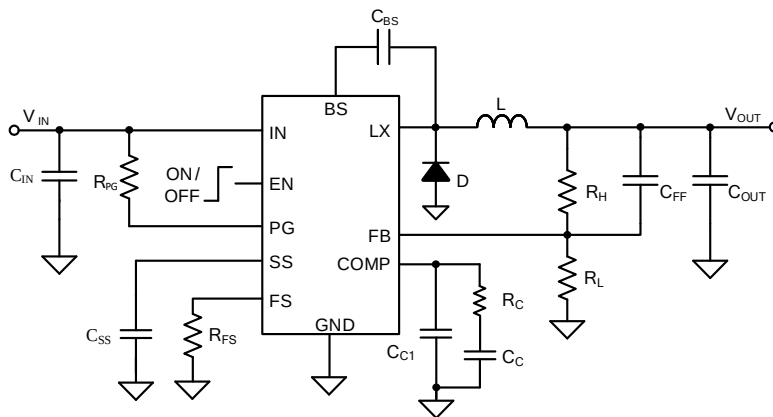


Figure1. Schematic Diagram

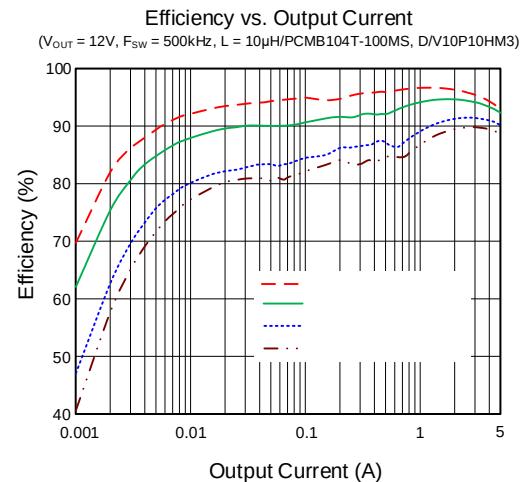


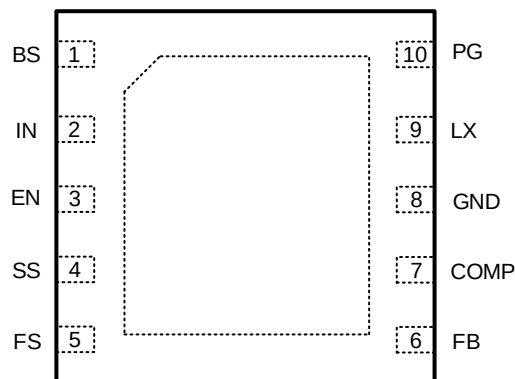
Figure2. Efficiency vs. Output Current

Ordering Information

Ordering Number	Package type	Top Mark
SQ27695TOD	DFN4×4-10 RoHS Compliant and Halogen Free	FNRxyz

x = year code, y = week code, z = lot number code

Pinout (top view)



Pin Description

Pin Number	Pin Name	Pin Description
1	BS	Bootstrap pin. Supply high side gate driver. Connect a 0.1μF ceramic capacitor between the BS and the LX pin.
2	IN	Input pin. Decouple this pin to GND pin with at least a 4.7μF ceramic capacitor.
3	EN	Enable pin, with internal pull-up current source. Pull below 1.2V to disable. Float to enable. Adjust the input under-voltage lockout with two resistors.
4	SS	External soft-start setting pin. Optional adjust the soft-start time by adding an appropriate external capacitor between this pin and the GND pin.
5	FS	Frequency programming pin. Connect a resistor to ground to program a switching frequency from 100kHz to 2.5MHz. The switching frequency(kHz) equals to: $10^5/R_{FS}(k\Omega)$
6	FB	Output feedback pin. Connect this pin to the center point of the output resistor divider (as shown in Figure 1) to program the output voltage: $V_{OUT}=0.8 \times (1+R_H/R_L)$
7	COMP	Error amplifier output. Connect frequency compensation components to this pin.
8	GND	Ground.
9	LX	Inductor pin. Connect this pin to the switching node of inductor.
10	PG	Power good indicator. Open drain output when the output voltage is within 93% to 120% of the regulation set point.
/	Thermal Pad	GND pin must be electrically connected to the exposed pad on the printed circuit board for proper operation.



Block Diagram

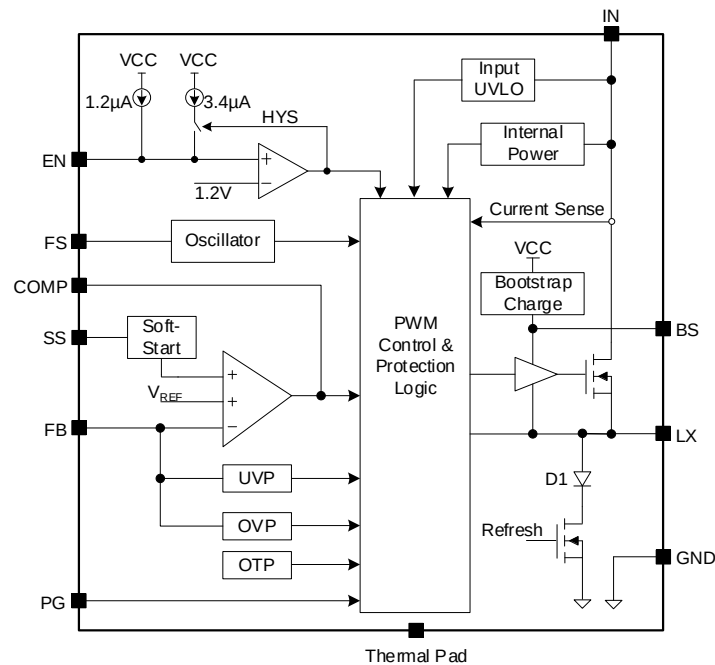


Figure3. Block Diagram

Absolute Maximum Ratings

Parameter (Note1)	Min	Max	Unit
IN, EN, PG	-0.3	65	V
LX	-0.6	65	
LX, 25ns duration	GND - 5	VIN + 5	
BS-LX	-0.3	6	
FB, COMP, SS, FS	-0.3	4	
Junction Temperature, Operating	-40	150	°C
Lead Temperature (Soldering, 10s.)		260	
Storage Temperature	-65	150	

Thermal Information

Parameter (Note2)	Typ	Unit
θ_{JA} Junction-to-Ambient Thermal Resistance	30	°C/W
θ_{JC} Junction-to-Case Thermal Resistance	14	
θ_{JB} Junction-to-Board Thermal Resistance	9	
P_D Power Dissipation $T_A = 25^\circ\text{C}$	3.3	W

Recommended Operating Conditions

Parameter (Note3)	Min	Max	Unit
Input Voltage	4.5	60	V
Output Voltage	0.8	40	
Junction Temperature	-40	125	°C

Electrical Characteristics

($V_{IN} = 48V$, $T_J = -40^{\circ}C$ to $+125^{\circ}C$. Typical values are at $T_J = 25^{\circ}C$, unless otherwise specified. The values are guaranteed by test, design or statistical correlation.)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Input Voltage Range	V_{IN}		4.5		60	V
Input UVLO Rising Threshold	$V_{UVLO,RISING}$		4.1	4.3	4.48	
Input UVLO Hysteresis	$V_{UVLO,HYS}$			0.325		
Shutdown Current	I_{SD}	$V_{EN} = 0V$		2.25	4.5	μA
Quiescent Current	I_Q	$V_{FB} = V_{REF} \times 105\%$		152	210	
EN Rising Threshold	V_{EN}	No voltage hysteresis, rising and falling	1.1	1.2	1.3	V
EN Input Current	I_{EN}	Enable threshold +50 mV		-4.6		μA
		Enable threshold -50 mV	-0.58	-1.2	-1.8	
EN Hysteresis Current	$I_{EN,HYS}$		-2	-3.4	-4.5	μA
Feedback Reference Voltage	V_{REF}	CCM	0.792	0.8	0.808	V
FB Leakage Current	$I_{FB,LKG}$	EN ON, $V_{FB} = 1V$		50		nA
Top FET R_{ON}	$R_{DS(ON)}$			95		m Ω
Peak Current Limit Threshold	$I_{PK,LMT}$	DC value, $V_{IN} = 12V$, $V_{OUT_SET} = 12V$	6.3	7.5	8.8	A
Peak Current Limit Delay	$t_{PK,DLY}$	(Note 4)		60		ns
Switching Frequency Program Range	$F_{SW,RNG}$		100		2500	kHz
Switching Frequency	F_{SW}	$R_{FS} = 200k\Omega$	450	500	550	
SS Charge Current	I_{SS}	$V_{SS} = 0.4V$		1.7		μA
SS Discharge Current	$I_{SS,RISING}$	$V_{FB} = 0V$, $V_{SS} = 0.4V$		277		
Power Good Threshold	V_{PG}	FB falling, PG from high to low		90%		V_{REF}
		FB rising, PG from low to high		93%		
		FB rising, PG from high to low		120%		
		FB falling, PG from low to high		115%		
PG Delay	$t_{PG,FALLING}$	PG falling edge		20		μs
	$t_{PG,RISING}$	PG rising edge		150		
Power Good Output Low Voltage	$V_{PG,LOW}$	$I_{PG,LOW} = 10mA$		0.45	0.7	V
PG High Leakage Current	I_{PG}	$V_{PWRGD} = 5.5V$, $T_A = 25^{\circ}C$		10		nA
Error Amplifier Transconductance	g_m	$-2\mu A < I_{COMP} < 2\mu A$, $V_{COMP} = 1V$		350		$\mu A/V$
Error Amplifier DC Gain	Gain	(Note 4)		10000		V/V
Error Amplifier Min Unity Gain Bandwidth	BW	(Note 4)		2500		kHz
Error Amplifier Source/Sink Current	$I_{EA,MAX}$	$V_{COMP} = 1V$, 100 mV overdrive		± 30		μA
Error Amplifier COMP to HS Current Transconductance	G_{PK}			17		A/V
Min t_{ON} Time	$t_{ON,MIN}$			100		ns
Max Duty	D_{MAX}			95		%
Thermal Shutdown Temperature	T_{SD}			160		$^{\circ}C$
Thermal Shutdown Hysteresis	T_{HYS}			15		

Note 1: Stresses beyond the "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

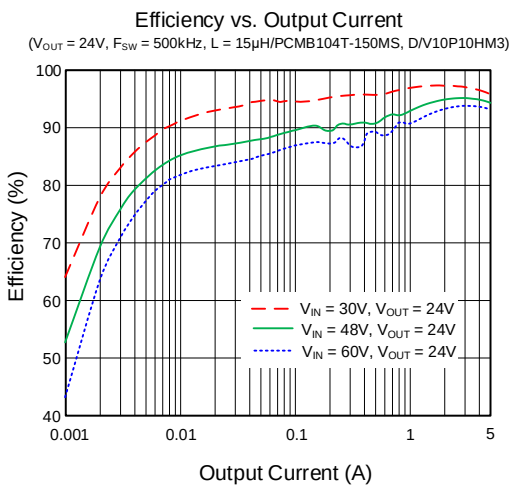
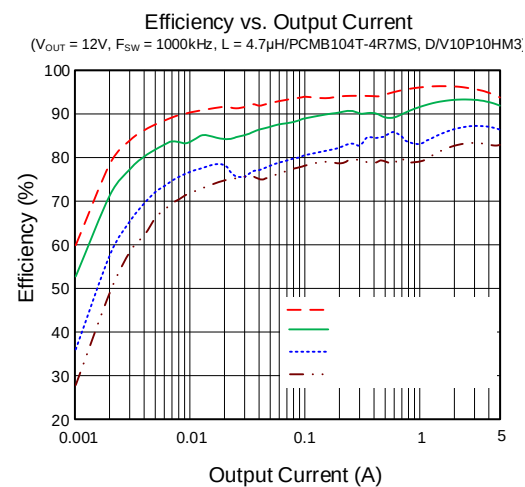
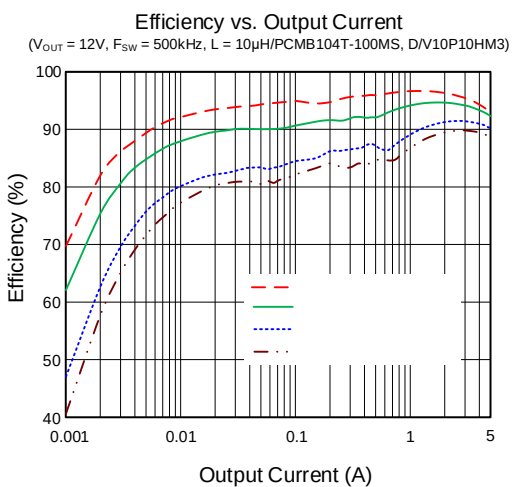
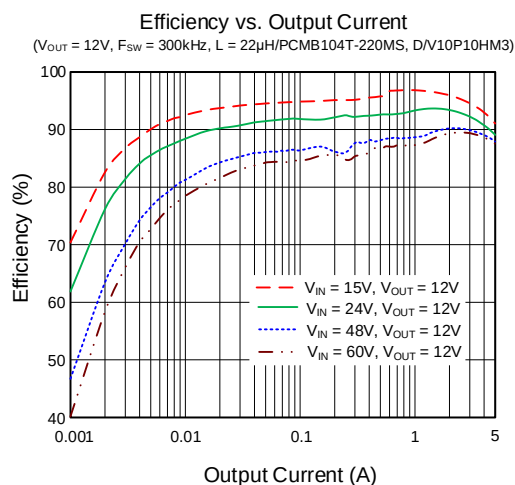
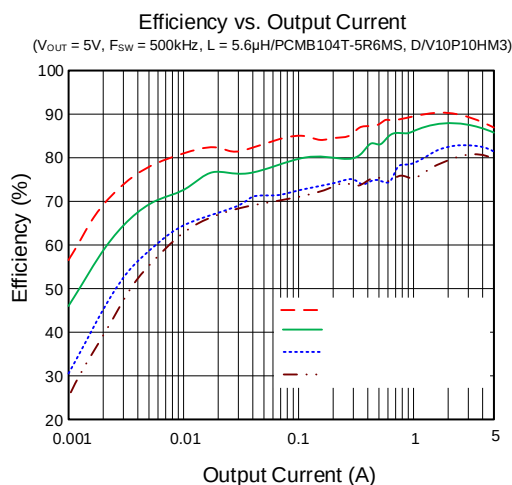
Note 2: θ_{JA} is measured in the natural convection at $T_A = 25^{\circ}C$ on a 2oz four-layer Silergy evaluation board.

Note 3: The device is not guaranteed to function outside its operating conditions.

Note 4: Guaranteed by design.

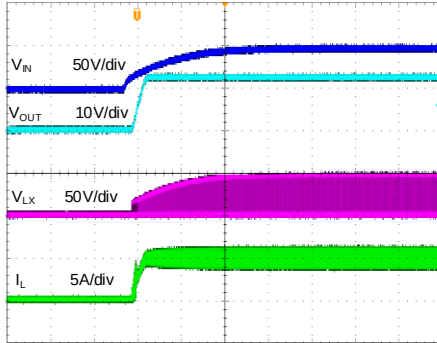
Typical Performance Characteristics

($T_A = 25^\circ\text{C}$, $V_{IN} = 48\text{V}$, $V_{OUT} = 12\text{V}$, $L = 10\mu\text{H}$, $C_{OUT} = 66\mu\text{F}$, $F_{SW} = 500\text{kHz}$, unless otherwise noted)



Startup from V_{IN}

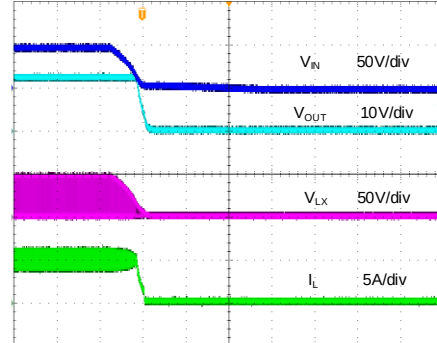
($V_{IN} = 48V$, $V_{OUT} = 12V$, $I_{OUT} = 5A$)



Time (4ms/div)

Shutdown from V_{IN}

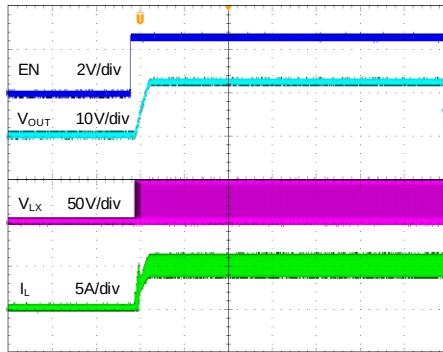
($V_{IN} = 48V$, $V_{OUT} = 12V$, $I_{OUT} = 5A$)



Time (4ms/div)

Startup from EN

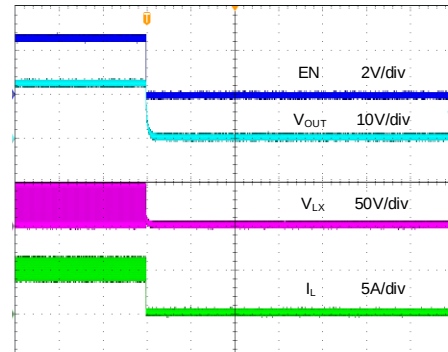
($V_{IN} = 48V$, $V_{OUT} = 12V$, $I_{OUT} = 5A$)



Time (4ms/div)

Shutdown from EN

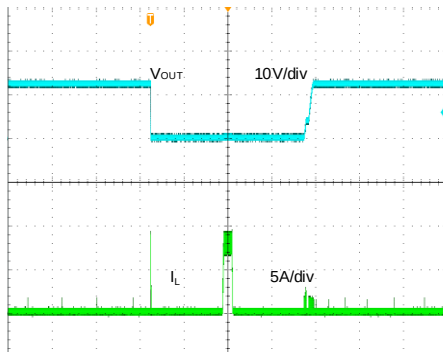
($V_{IN} = 48V$, $V_{OUT} = 12V$, $I_{OUT} = 5A$)



Time (4ms/div)

Short Circuit Protection

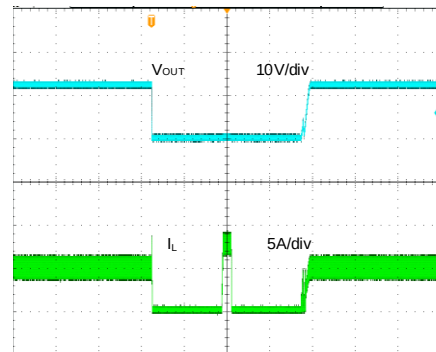
($V_{IN} = 48V$, $V_{OUT} = 12V$, $I_{OUT} = 0A \sim \text{short}$)



Time (10ms/div)

Short Circuit Protection

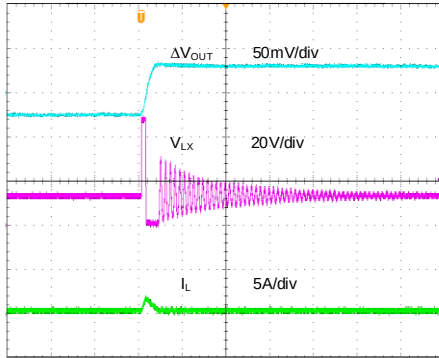
($V_{IN} = 48V$, $V_{OUT} = 12V$, $I_{OUT} = 5A \sim \text{short}$)



Time (10ms/div)

Output Ripple

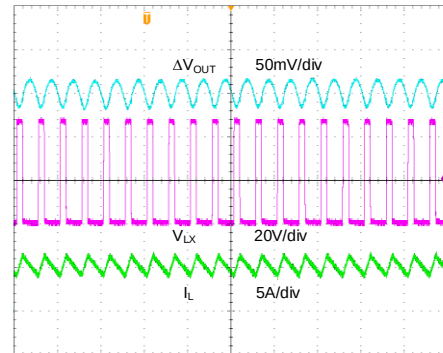
($V_{IN} = 48V$, $V_{OUT} = 12V$, $I_{OUT} = 0A$)



Time (4 μ s/div)

Output Ripple

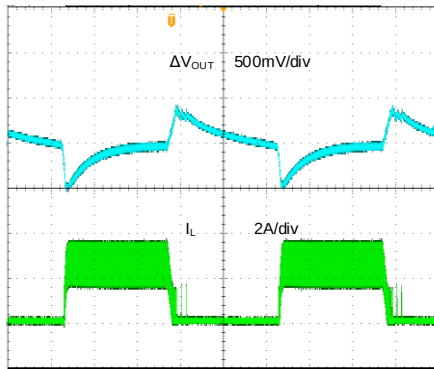
($V_{IN} = 48V$, $V_{OUT} = 12V$, $I_{OUT} = 5A$)



Time (4 μ s/div)

Load Transient

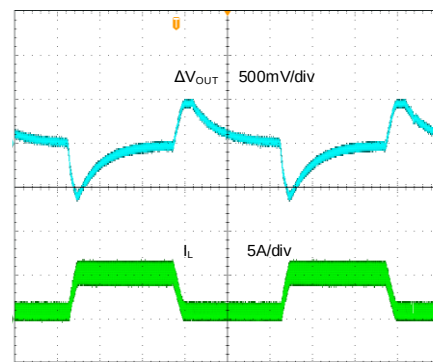
($V_{IN} = 48V$, $V_{OUT} = 12V$, $I_{OUT} = 0 \sim 2.5A$)



Time (200 μ s/div)

Load Transient

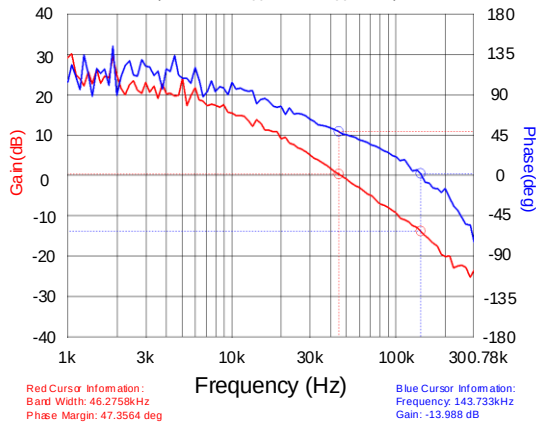
($V_{IN} = 48V$, $V_{OUT} = 12V$, $I_{OUT} = 0.5 \sim 5A$)



Time (200 μ s/div)

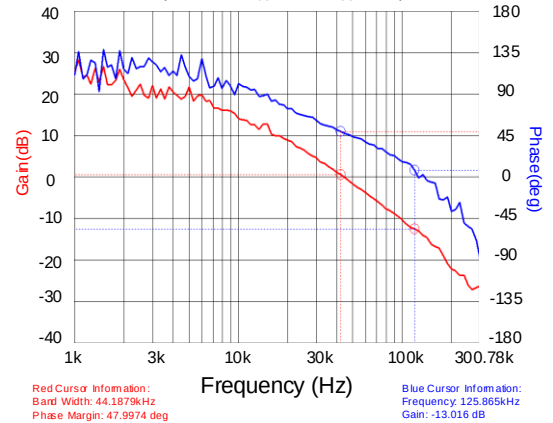
Bode Plot

($V_{IN} = 48V$, $V_{OUT} = 12V$, $I_{OUT} = 5A$)



Bode Plot

($V_{IN} = 60V$, $V_{OUT} = 12V$, $I_{OUT} = 5A$)



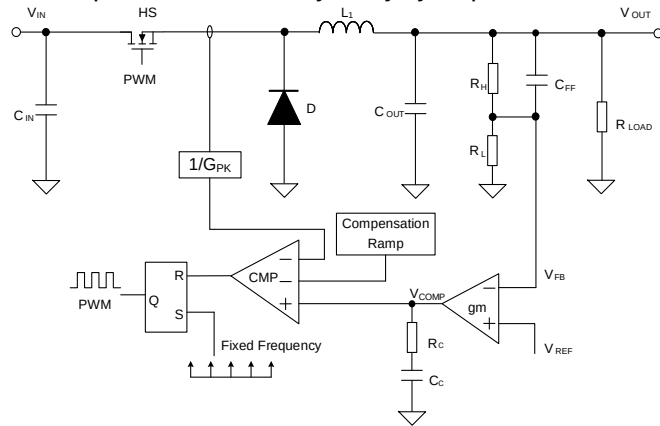
Detailed Description

General Features

Fixed Frequency and Peak Current Mode Control Strategy

The device adopts fixed frequency and peak current mode control strategy. The output voltage is fed back to the error amplifier through an external resistor divider connected to the FB pin, and compared with the internal reference voltage V_{REF} . The output of the error amplifier (V_{COMP}) controls the peak current level and the output voltage.

When fixed frequency clock comes, the internal high-side N-channel power FET will turn on. The high side power FET current is translated into a ramp voltage signal by a coefficient of $1/G_{PK}$. When the ramp voltage plus the compensation ramp reaches the V_{COMP} , the high side power FET will turn off. Besides, the peak current mode control provides inherent cycle by cycle peak current limit.



Light Load Operation

Under light load conditions, the output of the error amplifier (V_{COMP}) naturally decreases and reduces the peak current. When the V_{COMP} further goes down with the load decreasing and reaches the pre-set low threshold, the device will stop switching to decrease the switching power loss and reduce quiescent current to further improve light-load efficiency. Switching resumes once V_{COMP} rises above the low threshold.

Programmable Soft-start Time

The soft-start time can be programmed by SS pin. A capacitor is placed between SS pin and GND pin to program the soft-start time. The soft-start time equation is:

$$t_{SS}(ms) = \frac{C_{SS}(nF) \times V_{REF}(V)}{I_{SS}(\mu A)}$$

The typical value of SS's charging current I_{SS} is 1.7 μA . To guarantee the programmable soft-start time is not too

short when using smaller SS capacitor, there is a minimum soft-start time limitation, the minimum soft-start time is 0.5ms.

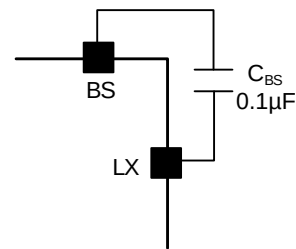
Power Good Indicator

The power good indicator is an open drain output controlled by a window comparator connected to the feedback signal. If V_{FB} is greater than 93% V_{REF} and less than 120% V_{REF} , then after at least the power good delay time (150 μs), PG will be high-impedance.

PG should be connected to V_{IN} or another voltage source through a resistor (e.g. 10k Ω ~ 100k Ω).

External Bootstrap Capacitor

This device integrates a floating power supply for the gate driver that operates the internal high-side N-channel power FET. Proper operation requires a 0.1 μF low ESR ceramic capacitor to be connected between BS and LX.



Adjustable Switching Frequency

The switching frequency is adjustable from 100kHz to 2.5MHz by connecting a resistor between FS and GND. The switching frequency can be calculated as follows:

$$F_{sw}(kHz) = \frac{10^5}{R_{FS}(k\Omega)}$$

Note that switching frequency will be limited if the on time is close to the minimum on time. Table 1 shows the proper switching frequency and R_{FS} for typical applications.

Table 1

F_{sw}/kHz	$R_{FS}/k\Omega$	V_{OUT}/V ($V_{IN}=48V$)		
		5	12	24
300	330	√	√	√
500	200	√	√	√
1000	100	×	√	√
1200	82	×	√	√

Minimum Duty Cycle and Maximum Duty Cycle

The switching frequency is not only affected by component tolerance but also minimum on and off time limit. Therefore, the minimum duty cycle is around 7.5% at 500kHz switching frequency considering ~150ns minimum on time. Benefiting by the device's on time

stretch function, the maximum duty cycle is up to 95% under -40°C ~ 125°C condition.

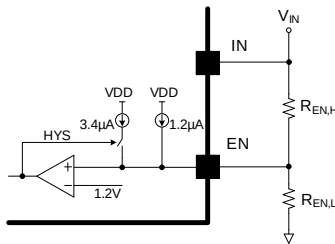
Enable and Adjustable Input Under Voltage Lock-out

The EN pin provides electrical on/off control of the device. Once the EN pin voltage exceeds the 1.2V threshold voltage, the device will start to switch. If the EN pin voltage is pulled below the 1.2V threshold voltage, the device will stop switching and enter shutdown state. An external set-point voltage divider from VIN to GND can be used to adjust the input under voltage lock-out. The $R_{EN,H}$ and $R_{EN,L}$ equation is as follows:

$$R_{EN,H}(k\Omega) = \frac{V_{IN,UVLO,Rising} - V_{IN,UVLO,Falling}}{3.4\mu A \times 10^3}$$

$$R_{EN,L}(k\Omega) = \frac{1.2V \times R_{EN,H}}{V_{IN,UVLO,Rising} - 1.2V + 1.2\mu A \times R_{EN,H} \times 10^3}$$

For example, setting $R_{EN,H} = 500k\Omega$ and $R_{EN,L} = 100k\Omega$, the input UVLO rising and falling threshold will be 6.6V and 4.9V.



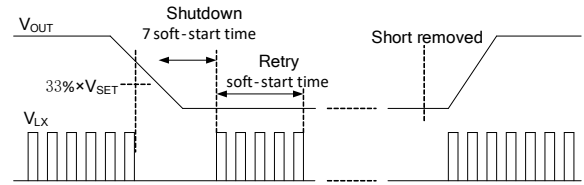
Fault Protection

Peak Current Limit Protection

Benefiting from the peak current mode control, the device provides inherent cycle by cycle peak current limit protection. During t_{ON} , and after $t_{ON,MIN}$, if the high side power FET current exceeds the peak current limit threshold, the high side power FET will turn off. If the device detects 128 consecutive cycles peak current limit protection, the device will be disabled for a hiccup off time. In addition, the switching frequency will be linearly folded back if the FB voltage is lower than 50% of the reference voltage. This will effectively increase the off time of the high side power FET, providing sufficient time to ramp down the high side power FET current.

Short Circuit Protection

If $V_{OUT} < 33\%$ and peak current limit is triggered, the short-circuit protection mode will be initiated, and the device will shut down for 7 soft-start time, after which the device will restart with a complete soft-start cycle. If the short circuit condition remains after a soft start time, this hiccup cycle will continue unless the junction temperature exceeds T_{SD} . If the fault condition is resolved, the device will resume normal operation.



Over Temperature Protection (OTP)

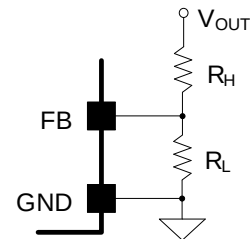
The over temperature protection (OTP) circuitry prevents overheating due to excessive power dissipation. This will shut down the device when the junction temperature exceeds T_{SD} . Once the junction temperature cools down by approximately 15°C, the device will resume normal operation after a complete soft-start cycle. For continuous operation, provide adequate cooling so that the junction temperature does not exceed the T_{SD} .

Design Procedure

Feedback Resistor Selection

Choose R_H and R_L to program the proper output voltage. To minimize the power consumption under light loads, it is desirable to choose large resistance values for both R_H and R_L . A value of between 10kΩ and 1MΩ is strongly recommended for R_H . If $V_{OUT} = 12V$, $R_H = 100k\Omega$ is chosen, then using following equation, R_L can be calculated to be 7.14kΩ.

$$R_L = \frac{0.8V}{V_{OUT} - 0.8V} \times R_H$$



Input Capacitor Selection

Input filter capacitors are needed to reduce the ripple voltage on the input, to filter the switched current drawn from the input supply and to reduce potential EMI. When selecting an input capacitor, be sure to select a voltage rating at least 20% greater than the maximum voltage of the input supply and a temperature rating above the system requirements. X5R or X7R series ceramic capacitors are most often selected due to their small size, low cost, surge current capability and high RMS current ratings over a wide temperature and voltage range. However, systems that are powered by a wall adapter or other long and therefore inductive cabling may be susceptible to significant inductive ringing at the input to the device. In these cases, consider adding some bulk

capacitance like electrolytic, tantalum or polymer type capacitors. Using a combination of bulk capacitors (to reduce overshoot or ringing) in parallel with ceramic capacitors (to meet the RMS current requirements) is helpful in these cases.

Consider the RMS current rating of the input capacitor, paralleling additional capacitors if required to meet the calculated RMS ripple current.

$$I_{CIN_RMS} = I_{OUT} \times \sqrt{D \times (1 - D)}$$

The worst-case condition occurs at $D = 0.5$, then

$$I_{CIN_RMS_MAX} = \frac{I_{OUT}}{2}$$

For simplification, choose an input capacitor with an RMS current rating greater than half of the maximum load current.

On the other hand, the input capacitor value determines the input voltage ripple of the converter. If there is an input voltage ripple requirement in the system, choose an appropriate input capacitor that meets the specification. Given the very low ESR and ESL of ceramic capacitors, the input voltage ripple can be estimated by

$$V_{CIN_RIPPLE_CAP} = \frac{I_{OUT}}{f_{SW} \times C_{IN}} \times D \times (1 - D)$$

The worst-case condition occurs at $D = 0.5$, then

$$V_{CIN_RIPPLE_MAX} = \frac{I_{OUT}}{4 \times f_{SW} \times C_{IN}}$$

The capacitance value is less important than the RMS current rating. In most applications three 2.2μF X5R capacitors are sufficient. Take care to locate the ceramic input capacitor as close to the device's IN and GND pin as possible.

Inductor Selection

The inductor is necessary to supply constant current to the output load while being driven by the switched input voltage. Selecting a low inductor value will help reduce size and cost and enhance transient response, but will increase peak inductor ripple current, reducing efficiency and increasing output voltage ripple. The low DC resistance (DCR) of these low value inductors may help reduce DC losses and increase efficiency. On the other hand, higher inductor values tend to have higher DCR and will slow transient response.

A reasonable compromise between size, efficiency, and transient response can be determined by selecting a ripple current (ΔI_L) about 20% ~ 50% of the desired full output load current. Start calculating the approximate inductor value by selecting the input and output voltages, the operating frequency (f_{SW}), the maximum output

current (I_{OUT_MAX}) and estimating a ΔI_L as some percentage of that current.

$$L_1 = \frac{V_{OUT} \times (V_{IN} - V_{OUT})}{V_{IN} \times f_{SW} \times \Delta I_L}$$

Use this inductance value to determine the actual inductor ripple current (ΔI_L) and required peak current inductor current I_{L_PEAK} .

$$\Delta I_L = \frac{V_{OUT} \times (V_{IN} - V_{OUT})}{V_{IN} \times f_{SW} \times L_1}$$

$$I_{L_PEAK} = I_{OUT_MAX} + \frac{\Delta I_L}{2}$$

Select an inductor with a saturation current and thermal rating in excess of I_{L_PEAK} .

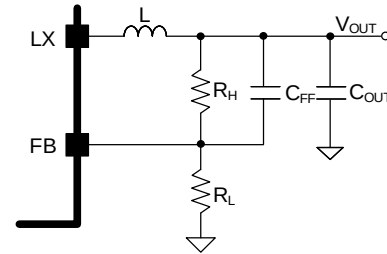
For highest efficiency, select an inductor with a low DCR that meets the inductance, size and cost targets. Low loss ferrite materials should be considered.

Output Capacitor Selection

The output capacitor is selected to handle the output ripple noise requirements. Both steady state ripple and transient requirements must be taken into consideration when selecting this capacitor. Ceramic and POS types are most often selected due to their small size and low cost. For the best performance, it is recommended to use an X5R or better grade ceramic capacitor greater than 22μF capacitance.

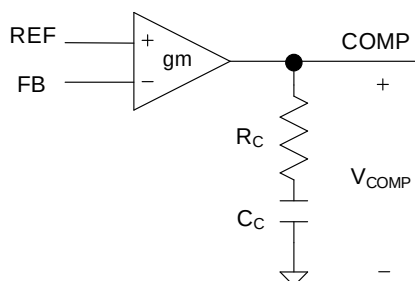
Load Transient Considerations

The device integrates the compensation components to achieve good stability and fast transient responses. Adding a small ceramic capacitor C_{FF} in parallel with R_H may further speed up the load transient responses and is thus highly recommended for applications with large load transient step requirements.



Loop Compensation Parameters Selection

The device uses a trans-conductance amplifier for the error amplifier and readily supports a commonly used frequency compensation circuit. The compensation circuit is shown as below, which is normally implemented in high bandwidth power supply designs using low ESR output capacitors.



The R_C and C_C introduce a zero to the loop compensation. Increasing R_C will increase the bandwidth and increasing C_C will decrease the bandwidth. With higher bandwidth, the IC will achieve faster dynamic response speed. However, the higher bandwidth will bring less stability margin. So it is a tradeoff for dynamic response and stability margin when selecting R_C and C_C . In addition, placing a capacitor (C_{C1} , which is much less than C_C) between COMP and GND is recommended to reject high frequency noise.

The design guidelines for the device loop compensation are as follows:

$$\frac{V_{COMP}}{I_{COMP}} = \frac{1 + s \times R_C \times C_C}{s \times C_C}$$

Thermal Design Considerations

Maximum power dissipation depends on the thermal resistance of the IC package, the PCB layout, the surrounding airflow, and the difference between the junction and ambient temperatures. The maximum power dissipation may be calculated by:

$$P_{D,MAX} = (T_{J,MAX} - T_A) / \theta_{JA}$$

Where, $T_{J,MAX}$ is the maximum junction temperature, T_A is the ambient temperature, and θ_{JA} is the junction to ambient thermal resistance.

To comply with the recommended operating conditions, the maximum junction temperature is 125°C. The junction to ambient thermal resistance θ_{JA} is layout dependent. For the DFN4×4-10 package the thermal resistance θ_{JA} is 30°C/W when measured on a standard Silergy four-layer thermal test board. These standard thermal test layouts have a very large area with long 2-oz. copper traces connected to each IC pin and very large, unbroken 1-oz. internal power and ground planes.

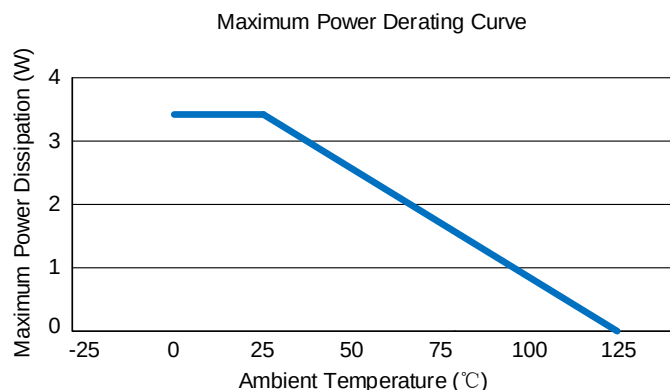
Meeting the performance of the standard thermal test board in a typical tiny evaluation board area requires wide copper traces well-connected to the IC's backside pads leading to exposed copper areas on the component side of the board as well as good thermal via from the exposed pad connecting to a wide middle-layer ground plane and,

perhaps, to an exposed copper area on the board's solder side.

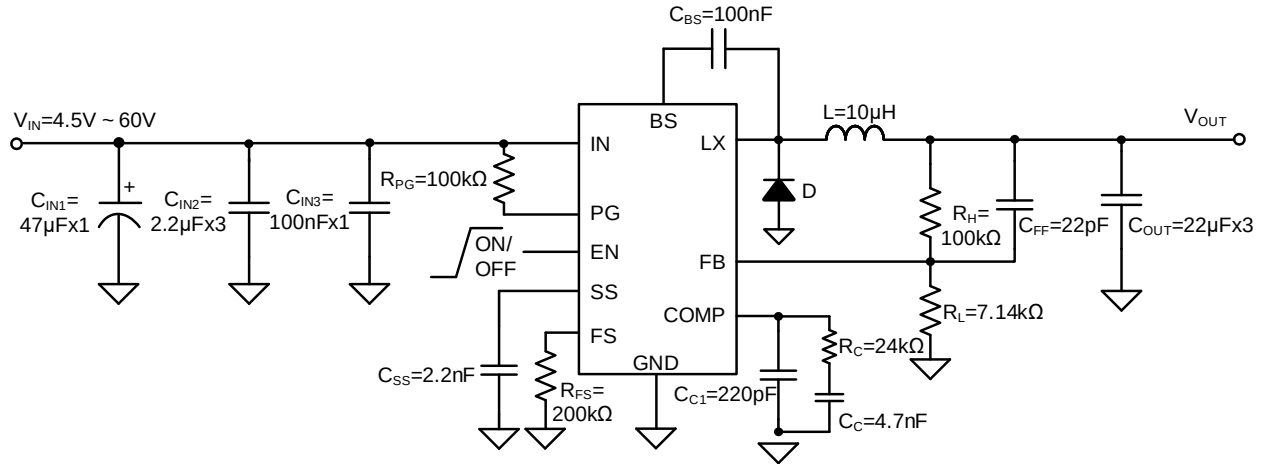
The maximum power dissipation at $T_A = 25^\circ\text{C}$ may be calculated by the following formula:

$$P_{D,MAX} = (125^\circ\text{C} - 25^\circ\text{C}) / (30^\circ\text{C}/\text{W}) = 3.33\text{W}$$

The maximum power dissipation depends on operating ambient temperature for fixed $T_{J,MAX}$ and thermal resistance θ_{JA} . Use the derating curve in figure below to calculate the effect of rising ambient temperature on the maximum power dissipation.



Application Schematic ($V_{OUT} = 12V$)



BOM List

Designator	Description	Part Number	Manufacturer
C _{IN1}	47µF/100V Electrolytic Cap		
C _{IN2}	2.2µF/100V/X7R, 1206	GRM31CR72A225KA73L	mpRata
C _{IN3}	100nF/100V/X7R, 0603	GRM188R72A104KA35D	mpRata
C _{OUT}	22µF/25V/X5R, 1206	GRM31CR61E226KE15L	mpRata
C _{BS}	100nF/50V/X7R, 0603	GRM188R71H104KA93D	mpRata
C _{SS}	2.2nF/50V/X7R, 0603	GRM188R71H222KA01D	mpRata
C _{C1}	220pF/50V/X7R, 0603	GRM188R71H221KA01D	mpRata
C _C	4.7nF/50V/X7R, 0603	GRM188R71H472KA01D	mpRata
C _{FF}	22pF/50V/C0G, 0603	GRM1885C1H220JA01D	mpRata
D	10A/100V	V10P10HM3	Vishay
L	10µH	PCMB104T-100MS	Susumu
R _H	100kΩ, 1%, 0603		
R _L	7.14kΩ, 1%, 0603		
R _{PG}	100kΩ, 1%, 0603		
R _{FS}	200kΩ, 1%, 0603		
R _C	24kΩ, 1%, 0603		

Recommend Components for Typical Applications

V _{OUT} (V)	F _{sw} (kHz)	R _H (kΩ)	R _L (kΩ)	R _C (kΩ)	C _C (nF)	C _{C1} (pF)	L/(Rated/Saturating Current)	C _{OUT}
5	500	100	19.05	12	1.5	56	5.6µH/ PCMB104T-5R6MS	22µF×3/ GRM31CR61E226KE15L
12	300	100	7.14	15	4.7	220	22µH/ PCMB104T-220MS	22µF×4/ GRM31CR61E226KE15L
12	500	100	7.14	24	4.7	220	10µH/ PCMB104T-100MS	22µF×3/ GRM31CR61E226KE15L
12	1000	100	7.14	27	4.7	100	4.7µH/ PCMB104T-4R7MS	22µF×3/ GRM31CR61E226KE15L
24	500	100	3.45	33	4.7	100	15µH/ PCMB104T-150MS	22µF×4/ GRM31CR61E226KE15L

Layout Design

Refer to Figure4 and follow these PCB layout guidelines for optimal performance.

- 1) Place the input capacitor very near IN and GND, minimizing the loop formed by these connections.
- 2) Keep the high current traces as short and wide as possible.
- 3) Make the feedback sampling point connect with C_{OUT} rather than the inductor output terminal.
- 4) Place the FB components (R_H , R_L and C_{FF}) as close to FB as possible. Avoid routing the FB trace near LX as it is noise sensitive.
- 5) Place the COMP components (R_C , C_C and C_{C1}) as close to COMP as possible. Avoid routing the COMP trace near LX as it is noise sensitive.
- 6) The LX connection has large voltage swings and fast edges and can easily radiate noise to adjacent components. Keep its area small to prevent excessive EMI, while providing wide copper traces to minimize parasitic resistance and inductance. Keep sensitive components away from the switching node or provide ground traces between for shielding, to prevent stray capacitive noise pickup.
- 7) Provide dedicated wide copper traces for the power path ground between the IC and the input and output capacitor grounds, rather than connecting each of these individually to an internal ground plane.
- 8) It is desirable to maximize the PCB copper area connecting to GND pin to achieve the best thermal and noise performance. If the board space allowed, a ground plane is highly desirable.
- 9) Place some vias in GND copper for heat sinking too.
- 10) A four-layer layout is strongly recommended to achieve better thermal performance.
- 11) Keep the BS voltage path (BS, LX and C_{BS}) as short as possible.

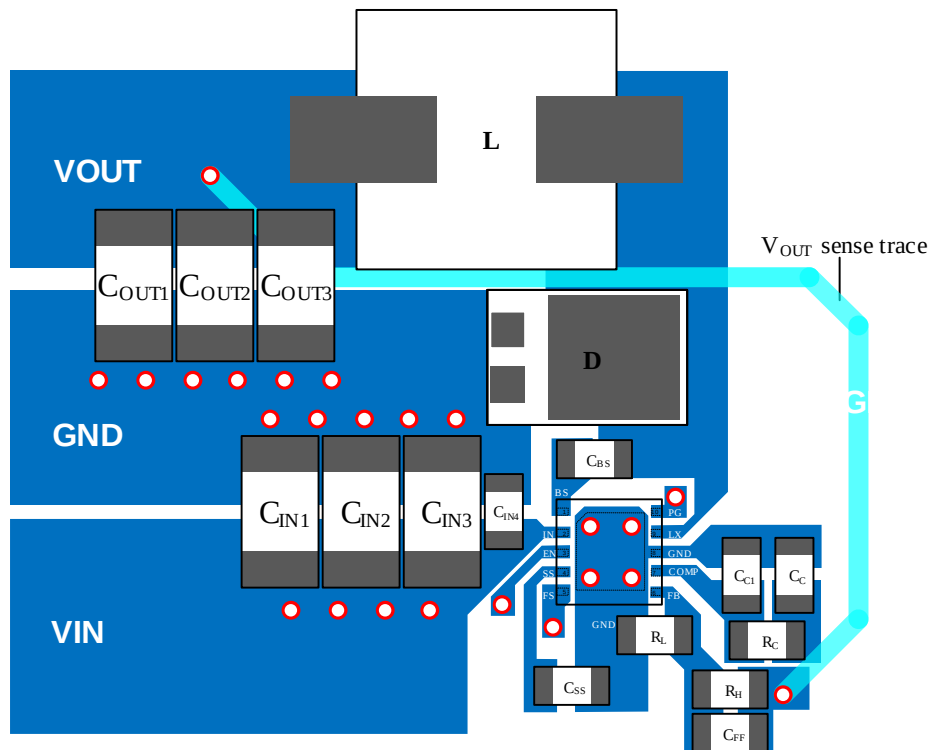
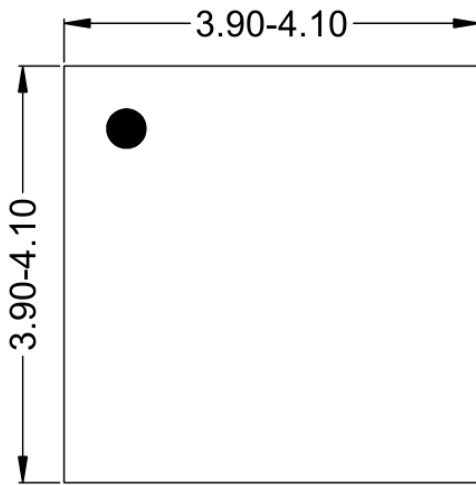
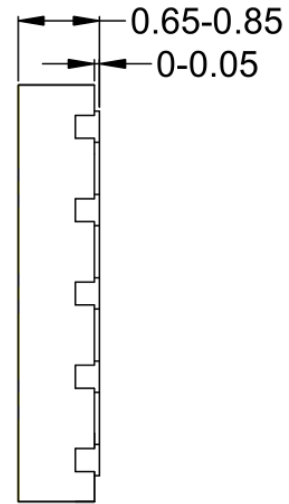


Figure4. PCB Layout Suggestion

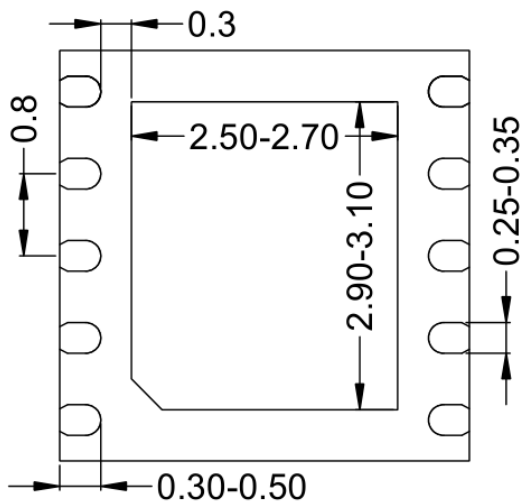
DFN4×4-10 Package Outline and PCB Layout



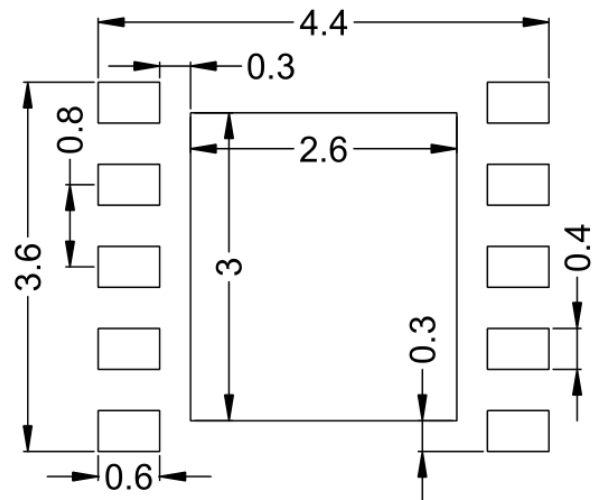
Top View



Side View



Bottom View



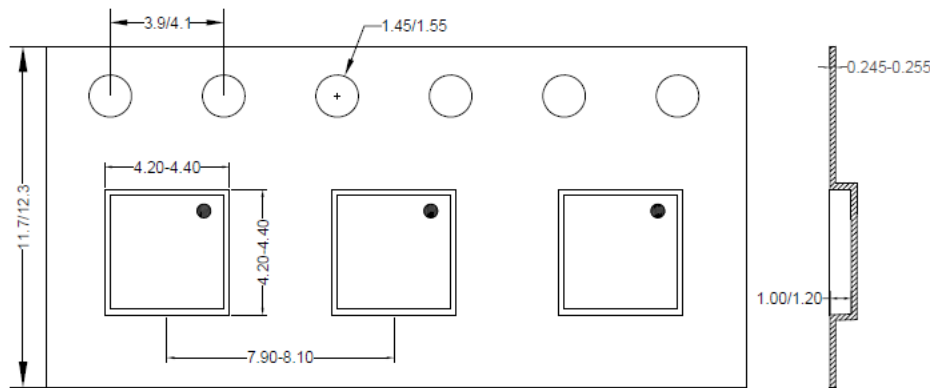
Recommended PCB layout
(only for reference)

Notes: All dimension in millimeter and exclude mold flash & metal burr.

Tape and Reel Information

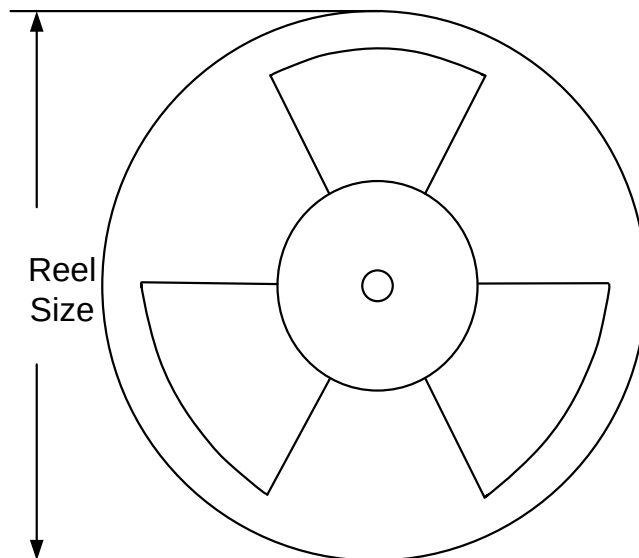
1. Tape Orientation

DFN4x4-10



Feeding Direction →

2. Carrier Tape and Reel specification for packages



Package types	Tape width (mm)	Pocket pitch(mm)	Reel size (Inch)	Trailer * length(mm)	Leader * length (mm)	Qty per reel
						(pcs)
DFN4x4-10	12	8	13"	400	400	5000

3. Others: NA

Revision History

The revision history provided is for informational purpose only and is believed to be accurate, however, not warranted. Please make sure that you have the latest revision.

Date	Revision	Change	Pages changed
May.7, 2024	1.0	Initial Release	-
October 9, 2024	1.0A	Modify EC Table NOTE2 and supplement the description of thermal resistance coefficient.	4

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