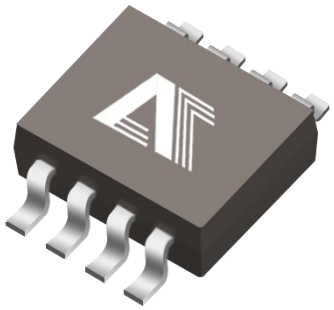
AOTE SEMICONDUCTOR



RS-485/RS-422CHIP

SN75176BDR

Product Data Sheet

AOTE DCC
RELEASE

◆ Summary ：

SN75176BDR/SN75LBC184DR is a transceiver chip used in RS-485 and RS-422 communication systems. The data transmission rate of HM485 for transmission and reception can reach up to 2.5Mbps. 485 is a half duplex type. In addition, 485 has driver enable (DE) and receiver enable (RE) pins, and when turned off, the driver and receiver outputs are high impedance. MAX485CSA has a fail safe function, and when in the receiving state, the input terminal is open or short circuited, and the receiver output is high level.

◆ Product features

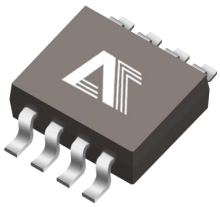
- Electrostatic Discharge (ESD): ± 1500V - Human Body Mode (HBM)
- Tri state output
- Half duplex
- The bus allows up to 128 transceivers

◆ Applications

- Low power RS-485 transceiver
- Low power RS-422 transceiver
- level shifting
- Electromagnetic interference (EMI) resistant transceiver
- Industrial control LAN

Applicable models: SN75176BDR,SN75LBC184DR Wait

◆ Product packaging



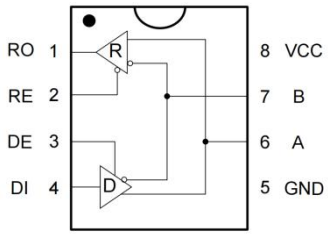


Figure 1. Packaging diagram

Pin number	Pin name	Pin Description
1	RO	Receiver output terminal: When the voltage at terminal A is 200mV higher than that at terminal B, RO is high; when the voltage at terminal A is 200mV lower than that at terminal B, RO is low
2	RE	Receiving enable terminal: Low level is effective, when RE is high, the receiving output is high impedance
3	DE	Sending Enable Terminal: High level is effective, and when DE is low, the sending output is high impedance. DE is at high level
4	DI	The chip operates in the transmitting state, and when DE is at a low level and RE is at a low level, the chip operates in the receiving state. Sending data input: When DI is low, A outputs a high level, B outputs a low level, and when DI is high, the opposite is true.
5	GND	Ground, negative terminal of power supply
6	A	Forward receiving input terminal, also known as forward sending output terminal
7	B	Reverse receiving input terminal, also known as reverse sending output terminal
8	V_{CC}	Positive end of power supply

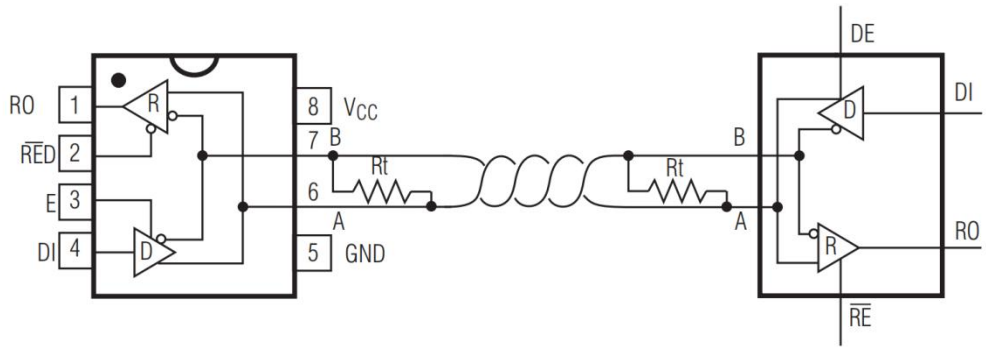


Figure 2 Schematic diagram of product application

◆ Product Function Table

(Table 1 Sending)

Input			Output	
RE	**DE**	**DI**	**A**	**B**
X	1	0	0	1
X	1	1	1	0
0	0	X	High-Z	High-Z
1	0	X	High-Z	High-Z

X=irrelevant
High-Z=high resistance

(Table 2 Reception)

Input			Output
RE	**DE**	**A-B**	**RO**
0	0	≥+0.2V	1
0	0	≤-0.2V	0
0	0	Input open circuit	1
1	0	X	High-Z

X=irrelevant
High-Z=high resistance

◆ Absolute maximum rated value of the product

power supply voltage(Vcc).....+5V

Control input voltage(RE,DE).....-0.5Vto+5V

Drive input voltage(DI)..... -0.5Vto+5V

Drive output voltage(A,B).....-0.5Vto+5V

Receive input voltage(A,B)..... -0.5Vto+5V

Receive output voltage(RO)..... -0.5Vto+5V

Continuous power spectrum(TA=+70℃)

8-foot plastic seal DIP(+70℃以上-9.08mW/℃).....725mW

8-foot SO (+70℃以上-5.85mW/℃)..... 470mW

Storage temperature range.....-65℃to+160℃

Working temperature range.....-40℃to+85℃

Soldering temperature (10 seconds).....+300℃

The maximum allowable rated value refers to the possibility that exceeding these values may cause irreparable damage to the device. Under these conditions, it is not conducive to the normal operation of the device. Continuous operation of the device at the maximum allowable rated value may affect its reliability, and the reference point for all voltages is ground.

◆ DC electrical characteristics of the product

(VDD=3.3V ± 5%, Ta=TMinto TMAx) (Note 1,2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Drive differential output (no load)	Vop1		2.7	3.3	5.5	V
Drive differential output (with load)	VoD2	R=30Ω,图3	1.5	1.8		V
The variation amplitude of differential output voltage driven by complementary output state degree	▵Vop				0.2	V
Drive common mode output voltage	Voc			1.6		V
The variation amplitude of common mode output voltage driven by complementary output state degree	▵Voc				0.2	V
Input high voltage	ViH	DE,RE	1.6			V
		DI	2			V
Input low voltage	ViL	DE,RE			0.8	V

		DI			1.2	
input current	IiN1	DE,RE,DI			±2	uA
Input current (A, B)	IN2	DE=0V; VCC=3.3V	ViN=3.3V	40	100	uA
			ViN=0V	120	300	
Receive differential threshold voltage	VTH		-0.2		-0.05	V
Received input lag	△VTH			70		mV
Receive output high voltage	VoH	I0=-3mA,VID=200mV	2.5	2.9		V
Receive output low voltage	VoL	I0=3mA, VID=-200mV		0.2	0.4	V
Receive tri state (high impedance) output current	lozR	0.4V≤VO≤2.4V			±1	uA
Receive input impedance	RIN			48		KS
No load supply current	Icc	RE、DI=0 or Vcc	DE=Vco	0.8	1.2	mA
			DE=0	0.7	1.2	
Drive short-circuit current (VO=High)	losp1	DE=RE=3.3V DI=0 Va=3.3V		60	100	mA
Drive short-circuit current (VO=Low)	losD2	DE=RE=3.3V DI=0Vg=0		60	100	mA
Receive short-circuit current	losR	OV≤VO≤VCC		20	60	mA
ESD Protect	A,B,Y and Z pins,tested using Human Body Model			±15		kV

(VDD=5V ± 5%, Ta=TMin to TMAx) (Note 3,4)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Drive differential output (no load)	Vop1		2.7	5	5.5	V
Drive differential output (with load)	Vop2	R=50Ω,Figure 3	2	3.6		V
The variation amplitude of differential output voltage driven by complementary output state	△Vop				0.2	V
Drive common mode output voltage	Voc				3	V
The variation amplitude of common mode output voltage driven by complementary output state	△Voc				0.2	V
Input high voltage	ViH	DE,RE	2			V
		DI	2.8			V
Input low voltage	ViL	DE,RE			0.8	V
		DI			1.6	

input current	liN1	DE,RE,DI				±2	uA
Input current (A, B)	liN2	DE=0V; VCC=5V	ViN=5V		60	150	uA
			ViN=0		180	400	
Receive differential threshold voltage	VTH			-0.2		0.2	V
Received input lag	△VTH				70		mV
Receive output high voltage	VoH	I0=-4mA, VID=200mV		3.5	4.5		V
Receive output low voltage	VoL	I0=4mA, VID=-200mV			0.2	0.4	V
Receive tri state (high resistance) output current	IozR	0.4V≤VO≤2.4V				±1	uA
Receive input impedance	RN				48		KΩ
No load supply current	Icc	RE、DI=0 or Vcc	DE=Vc		1.2	1.6	mA
			DE=0		1.1	1.5	
Drive short-circuit current(VO=High)	Iosp1	DE=RE=5V DI=0VA=5V			120	250	mA
Drive short-circuit current(VO=Low)	Iosp2	DE=RE=5V DI=0Vg=0			120	250	mA
Receive short-circuit current	IosR	OV≤VO≤VCC			60	100	mA
ESD Protect	A,B,Y and Z pins,tested using Human Body Model				±15		kV

◆ Switch characteristics

(VDD=3.3V ± 5%, Ta=TMINto TMAx) (Note 1,2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Drive input to output	tpLH	Fig 5,Fig 8,Rdiff=60Ω, CL1=Cl2=100pF,	30	60	90	ns
	tpHL		40	70	100	ns
Drive output pressure swing to output	tsKEW			10		ns
Drive up and down time	tR			70	100	ns
	tF			40	100	ns
Drive turned on until output is high	tzH	Fig6,Fig10,CL=100pF, S2 Close		90	120	ns
Driver turned on to output	tzL	Fig6,Fig10,CL=100pF,		100	120	ns

low		S1 Close				
Drive from low to off	tuz	Fig6,Fig10,CL=100pF, S1 Close		120	150	ns
Drive from high to off	tHz	Fig6,Fig10,CL=100pF S2 Close		120	150	ns
Receive input to output	tPLH	Fig5Fig9,Rdiff=60Ω, CL1=Cl2=100pF,	20	75	200	ns
	tpHL		20	80	200	ns
tPLH-tPHL| Differential receiving pressure swing	tsKD			10		ns
Receive enabled until output is low	tzL	Fig4,Fig11,CL=22pF, S2 Close		40	90	ns
Receive from enabled to output high	tzH	Fig4,Fig11,CL=22pF, S1 Close		60	90	ns
Receive from low to off	tLz	Fig4,Fig11,CL=22pF, S2 Close		80	120	ns
Receive from high to closed	tHz	Fig4,Fig11,CL=22pF, S1 Close		80	120	ns
Maximum data rate	fMAX		2.5			Mbps

(VDD=5V ± 5%, Ta=TMI into TMAx) (Note 3,4)

PARAMETER	SYMBOI	CONDITIONS	MIN	TYP	MAX	UNITS
Drive input to output	tpLH	Fig5,Fig8,Rdiff=50Ω, CL1=Cl2=100pF,	40	70	90	ns
	tPHL		10	40	60	ns
Drive output pressure swing to output	tsKEW			30		ns
Drive up and down time	tr			40	60	ns
	tF			40	60	ns
Drive turned on until output is high	tzH	Fig6,Fig10,CL=100pF, S2 Close		50	70	ns
Drive turned on until output is low	tzL	Fig6,Fig10,CL=100pF, S1 Close		50	70	ns
Drive from low to off	tz	Fig6,Fig10,CL=100pF, S1 Close		100	120	ns
Drive from high to off	tHz	Fig6,Fig10,CL=100pF, S2 Close	90	110		ns
Receive input to output	tpLH	Fig5,Fig9,Rdiff=50Ω, CL1=Cl2=100pF,	20	60	200	ns
	tpHL		20	40	200	ns
|tPLH-tPHL| Differential receiving pressure swing	tsKD			20		ns
Receive enabled until output is low	tzL	Fig4,Fig11,CL=15pF, S2 Close		50	80	ns

Receive from enabled to output high	tzH	Fig4,Fig11,CL=15pF, S1 Close		60	90	ns
Receive from low to off	tuz	Fig4,Fig11,CL=15pF, S2 Close		50	80	ns
Receive from high to closed	tHz	Fig4,Fig11,CL=15pF, S1 Close		60	90	ns
Maximum data rate	fMAX		2.5			Mbps

Note 1: All typical cases refer to vdd=3.3V, Ta=25 ℃;

Note 2: All currents input to the pins are positive, and all currents output from the pins are negative; Unless otherwise specified, voltage refers to the ground voltage;

Note 3: All typical cases refer to vdd=5V, Ta=25 ℃;

Note 4: All currents input to the pins are positive, and all currents output from the pins are negative; Unless otherwise specified, voltage refers to the ground voltage

◆ Product testing circuit

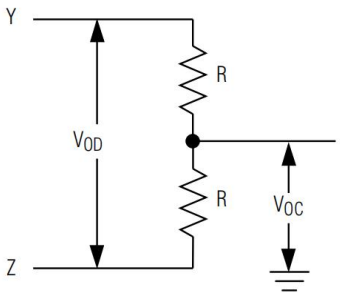


Figure 3. DC Drive Test Circuit

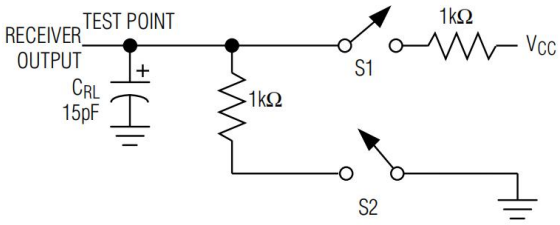


Figure 4. Receiving time test

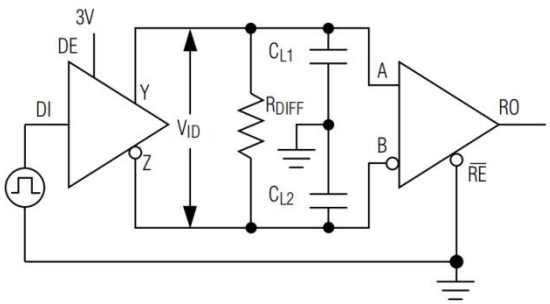


Figure 5. Driver receiving time test circuit

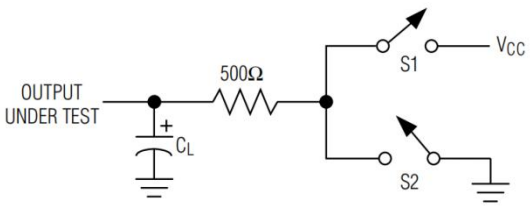


Figure 6. Driving time test circuit

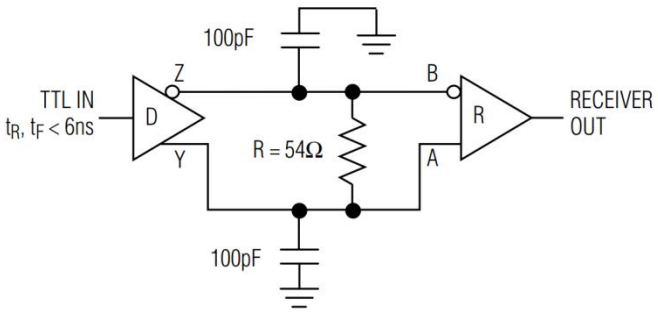


Figure 7. Reception and transmission delay test circuit

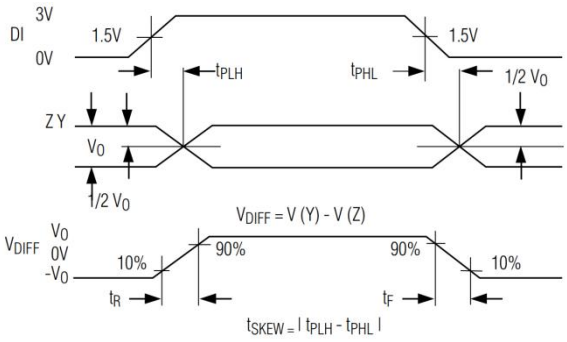


Figure 8. Driver transmission delay

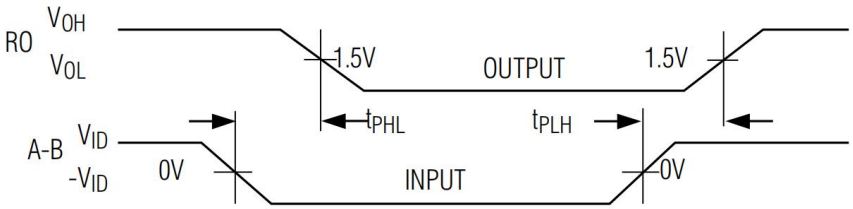


Figure 9. Receive transmission delay

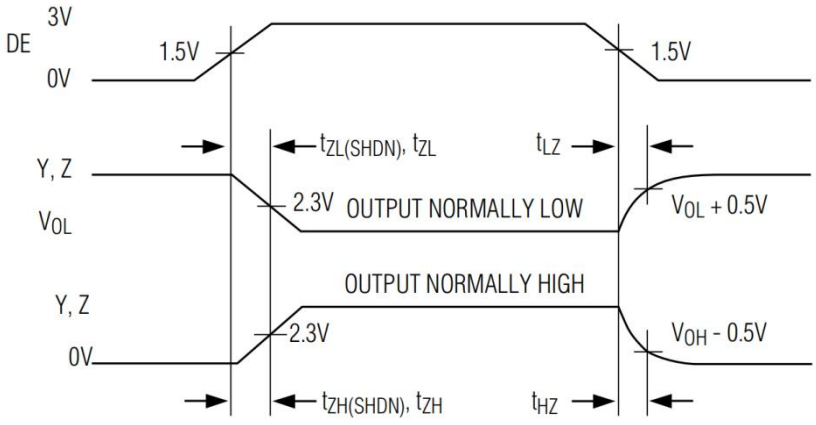


Figure 10. Drive on and off time

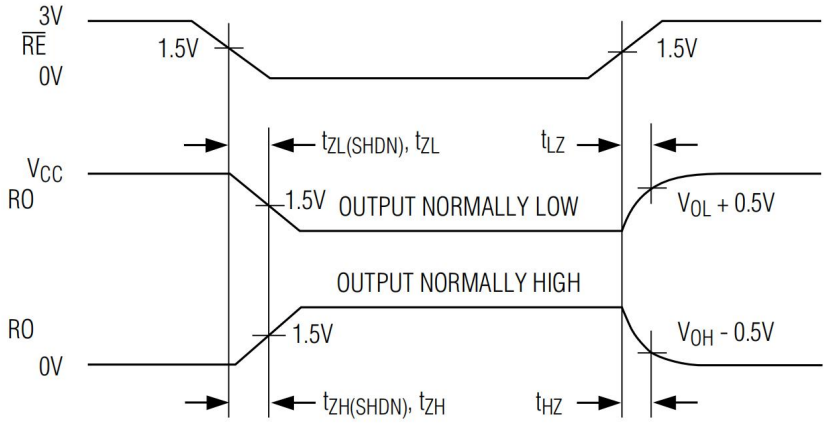


Figure 11. Receive opening and closing times

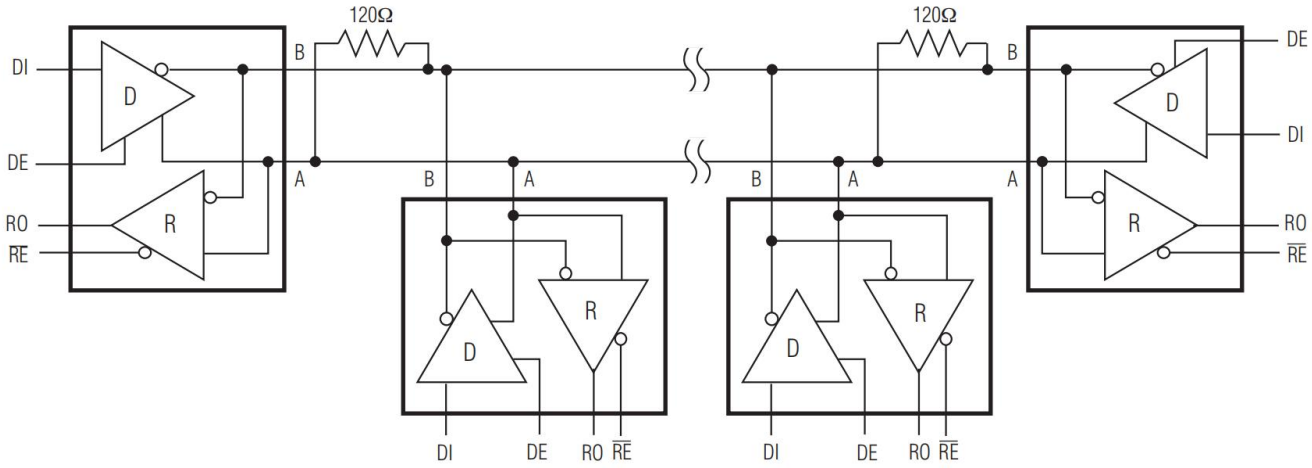


Figure 12. Typical Duplex RS-485 Network

◆ Attention

- AOTE implements dynamic technical updates. Specifications are subject to change. Refer to the official website for the latest version.
- Users must strictly adhere to specified conditions. Failures caused by misuse (overload, high temperature, incompatible circuits) are excluded from warranty.
- Contact technical support for customized validation in critical applications (medical devices, industrial control).
- This document is valid until December 31, 2026 Updates will be notified on the official website.
- For further clarification on technical specifications or application solutions, please contact us through official channels: