



钜地半导体
Tudi Semiconductor

Product Specification

TUDI-MAX491E

Low-Power, Slew-Rate-Limited RS-485/RS-422 Transceivers

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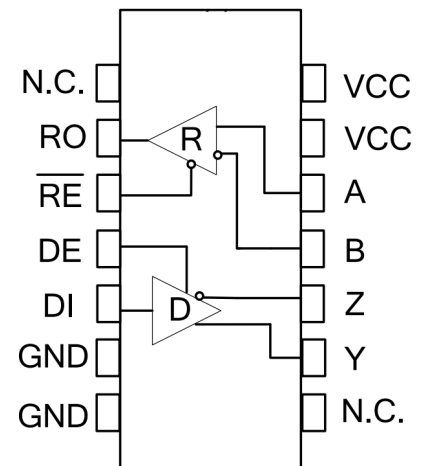
**semiconductor device
manufacturer**

- Design
- research and development
- production
- and sales



Features

- 4.5V~5.5V power supply, RS485/RS422 full-duplex communication;
- Fail-Safe function;
- 1/8 unit load, allowing up to 256 devices to be connected to the bus;
- Short-circuit output for the driver;
- Receiver open-circuit fail-safe protection;
- Strong anti-noise capability;
- Integrated transient voltage suppression function;
- Data rate in an electrical noise environment can reach 2.5Mbps;
- A, B port protection: HBM $\pm$ 15KV;



Pin diagram

Description

The MAX491E is a low-power, RS-485/RS-422 transceiver for harsh environments. Each output and receiver input is protected against $\pm 15\text{kV}$ electrostatic discharge (ESD) with no latch-up. These parts contain one driver and one receiver. The MAX491E's driver rise time is unconstrained, allowing them to transmit up to 2.5Mbps. These transceivers consume only 120μ of supply current with the drivers disabled and the line fully loaded. All parts operate from a single 5V supply. Short-circuit current is limited, and thermal shutdown circuit is protected, taking the outputs into a high-impedance state to prevent excessive power dissipation. The receiver input has a fail-safe feature that guarantees the output to be logic if it is open. The MAX491E is designed for full-duplex communication.

Applications

- Low-Power RS-485/RS-422 Transceivers
- Level Translators Transceivers for EMI-Sensitive Applications
- Industrial-Control Local Area Networks



Pin description

Pin number	Pin name	Pin function
1	NC	No internal connections required
2	RO	Receiver output.When RE is low,the RO output is high if A-B is $\geq -10\text{mV}$,and low if A-B is $\leq -200\text{mV}$.
3	/RE	Receiver output enable control.When /RE is low,the receiver output is enabled and RO is active;when /RE is high,the receiver output is disabled and RO is in high-impedance state.When RE is at a high level and DE is at a low level,the device enters low-power shutdown mode
4	DE	The driver output enables the control.When DE is at high level, the driver outputs effectively;when DE is low,it outputs high-impedance state.When /RE is high and DE is low,the device enters low-power shutdown mode.
5	DI	DI driver input.When DE is high,the low level on DI makes the in-phase output A of the driver low and the in-phase output B high;the high level on DI makes the in-phase output high and the in-phase output B low.
6	GND	Landing
7	GND	Landing
8	NC	No internal connections required
9	Y	Driver in-phase output terminal
10	Z	Driver inverting output
11	B	Receiver inverting input
12	A	Receiver in phase input
13	VCC	This pin can be connected to power or left unconnected
14	VCC	Power connection



Extreme parameter

Parameter	Symbol	Unit	size
Continuous power consumption	SOP14	mW	600
	DIP14	mW	700
Power supply voltage	VCC	V	+7
working temperature range		°C	-40~125
Storage temperature range		°C	-60~150
Welding temperature range		°C	300
Control port voltage	DI	V	-0.3~VCC+0.3
Bus side input voltage	A、B	V	-8~13
Receiver output voltage	RO	V	-0.3~VCC+0.3

The maximum limit parameters are values beyond which the device can be damaged in an irreversible manner. Operation of the device under these conditions is not intended to be normal and may affect the reliability of the device if operated continuously at the maximum rated limit. All voltages are referenced to ground.

ESD Protect						
Parameter	symbol	Test condition	Minimum	Typical case	Maximum	Unit
A、B、Y、Z		Human bodymodel		±15		KV
Other ports		Human bodymodel		±6		KV



Receiver Switching Characteristics

Parameter	symbol	Test condition	Minimum	Typical case	Maximum	Unit
Acceptor	tRPLH	See Figure 7 and Figure 8	20	60	90	ns
Input to output propagation delay from low to high		$V \geq 2.0V$; rising and falling edge time $V_{ID} \leq 15ns$				
The propagation delay from receiver input to output is from high to low	tRPHL		20	60	90	ns
tRPLH-tRPHL	tsKEW2			7	10	ns
Enable low time out	tRPZL	CL=15pF See Figures 7 and 8		20	50	ns
Enable to output high time	tRPZH	CL=15pF See Figures 7 and 8		20	50	ns
Time from output low to disable	tpRLZ	CL=15pF See Figures 7 and 8		20	45	ns
Time from output high to disable	tpRHZ	CL=15pF See Figures 7 and 8		20	45	ns
Off state Enable to output high time	tRPSH	CL=15pF See Figures 7 and 8		200	1400	ns
Off state Enable low time out	tRPSL	CL=15pF See Figures 7 and 8		200	1400	ns
Time to turn off	tsHDN	NOTE2	80		300	ns

(If not otherwise, VCC=3V~5.5V, Temp = TMIN ~ TMAX, typical value at Temp = 25) NOTE 1: V_{OD} and V_{OC} is the change in V_{OD} and V_{OC} amplitude caused when the DI state of the input signal changes, respectively.



DC electrical characteristics of the driver

Parameter	symbol	Test condition	Minimum	Typical case	Maximum	Unit
Driver differential output (non-loaded)	VoD ₁			4.5	VCC	V
Drive differential output	VoD ₂	graph 2,RL=27Ω	1.5	2.3	VCC	V
		graph 2,RL=50Ω	2	2.8	VCC	
Variation in the amplitude of the output voltage (NOTE1)	△VoD	graph 2,RL=27Ω			0.2	V
Output common mode voltage	Voc	graph 2,RL=27Ω			3	V
Amplitude Variation of Common Mode Output Voltage(NOTE1)	△Voc	graph 2,RL=27Ω			0.2	V
High-level input	VH	DI	2.0			V
Low level input	Vπ	DI			0.8	V
Logic input current	IN1	DI	-2		2	uA
Output the current during a short circuit, with high short-circuit	IosD ₁	Short circuit to OV~12V	35		250	mA
Output the current during a short circuit, down to low	IosD ₂	Short circuit to -7V~0V	-250		-35	mA

(If not otherwise, VCC=3V~5.5V, Temp = TMIN ~ TMAX, typical value at Temp = 25) NOTE 1: VO D and? VOC is the change in VOD and VOC amplitude caused when the DI state of the input signal changes, respectively.



drive switch characteristics

Parameter	symbol	Test condition	Minimum	Typical case	Maximum	Unit
Input to output propagation delay (low to high)	tDPLH	RDIFF=54 Ω, CL=CL?=100pF(see Figure 3 and Figure 4)		12	35	ns
Input to output propagation delay (high to low)	tDPHL			12	35	ns
tDPLH-tDPHL	tsKEW1			6	10	ns
Rise time /fall time	tDR,tDF			9	25	ns
Enable to high output	tpZH	R=110Ω (seeFigure 5 and 6)		20	90	ns
Enable to output low	tpZL			20	90	ns
Input low to disable	tpLZ	R=110Ω (seeFigure 5 and 6)		20	80	ns
Enable high input	tpHZ			20	80	ns
Enable high outputunder off condition	tDSH	R=110Ω (seeFigure 5 and 6)		500	900	ns
Enable low outputunder shutdown conditions	tDSL	RL=110Ω (seeFigure 5 and 6)		500	900	ns

Supply Current

Parameter	symbol	Test condition	Minimum	Typical case	Maximum	Unit
Supply current	Iccl	/RE=0V,DE=0V		220	400	uA
	Icc2	/RE=VCC, DE=VCC		240	400	uA
Turn-off current	IsHDN	/RE=VCC,DE=0V		0.5	10	uA



DC Electrical Characteristics of the Receiver

Parameter	symbol	Test condition	Minimum	Typical case	Maximum	Unit
Input current(A,B)	IN2	VCC=0 or 3.3V VIN=12V			125	uA
		VCC=0 or 3.3V VIN=-7V	-100			uA
Forward input threshold voltage	VIT+	$-7V \leq V_{cm} \leq 12V$			-10	mV
Reverse input threshold voltage	VIT-	$-7V \leq V_{cm} \leq 12V$	-200			mV
Input hysteresis voltage	Vhys	$-7V \leq V_{cm} \leq 12V$	10	30		mV
High level output voltage	VoH	IoUT=-4mA, VID=+200 mV	VCC-1.5			V
Low level output voltage	VoL	IoUT=+4mA, VID=-200 mV			0.4	V
Three state input leakage cur-rent	IozR	$0.4V < V_o < 2.4V$			±1	uA
Input resistance of receiver	RIN	$-7V \leq V_{cM} \leq 12V$	96			kΩ
Receiver short circuit curr-ent	IosR	$0V \leq V_o \leq VCC$	±7		±95	mA



Function table

Receiving function table			
control		input	output
/RE	DE	A-B	RO
0	X	$\geq -10\text{mV}$	H
0	X	$\leq -200\text{mV}$	L
0	X	Open/short circuit	H
1	X	X	Z
X: any level; Z: high impedance.			

Send function table				
control		input	output	
/RE	DE	DI	Y	Z
X	1	1	H	L
X	1	0	L	H
0	0	X	Z	Z
1	0	X	Z(shutdown)	
X: any level; Z: high impedance.				

Additional description

Introduction
The 491E is a full-duplex high-speed transceiver for RS-485/RS-42 communication, containing a driver and a receiver. It has fail-safe, overvoltage protection, and overcurrent protection. The TUDI-MAX491E achieves error-free transmission up to 2.5Mbps.
fail-safe
The 491E guarantees a logic high receiver output if the receiver input is short-circuited or open-circuited, or drivers connected to the terminated transmission line are disabled (idle). This is achieved by setting the receiver input thresholds to -10mV and -20mV , respectively. RO is logic high if the differential receiver input voltage $(A-B) \geq -10\text{mV}$, and RO is logic low if the voltage $(A-B) \leq -200\text{mV}$. Logic high with a minimum noise margin of 50mV can be realized depending on the receiver thresholds. The -10mV to -200mV threshold voltage is in accordance with the EIA/TIA-485 of $\pm 200\text{mV}$.
256 transceivers on the bus
The input impedance of the standard RS485 receiver is $12\text{k}\Omega$ (1 unit load), and the standard driver can drive to 32 unit loads. The receiver of the 491E transceiver has an input impedance of $1/8$ unit load ($96\text{k}\Omega$), allowing up to 256 transceivers to be connected in parallel on the same communication bus. These devices can be combined arbitrarily, or combined with other 485 transceivers, as long as the total load does not exceed 256 unit loads, they can be connected to the same bus.
Drive output protection
Protection against excessive output current and dissipation by fault or bus contention is provided by overcurrent and overvoltage protection mechanisms, with fast short-circuit throughout the common-mode voltage range (see Typical Operating Characteristics).

The circuit diagram on the left shows a Schmitt trigger implemented with a 74VHC14 hex inverters. The input of the inverter is connected to a square wave generator (labeled 'GENERATOR (NOTE 4)') through a 50Ω resistor. The output of the inverter is labeled 'OUT'. A feedback network consisting of a 110Ω resistor and a 50pF capacitor is connected between the output and the input. The input signal is labeled 'S1'. The output signal is labeled 'OUT'. The output voltage is defined as $V_{OM} = \frac{V_{OH} + V_{OL}}{2} \approx 1.5V$.

The timing diagram on the right shows the input signal 'IN' and the output signal 'OUT'. The input signal is a square wave with a high level of 1.5V and a low level of 0V. The output signal is a square wave with a high level of 3V and a low level of 0V. The propagation delay is labeled t_{pZH} and t_{pHZ} . The output voltage is labeled V_{OM} and V_{OH} . The output signal is shown with a 0.25V offset.

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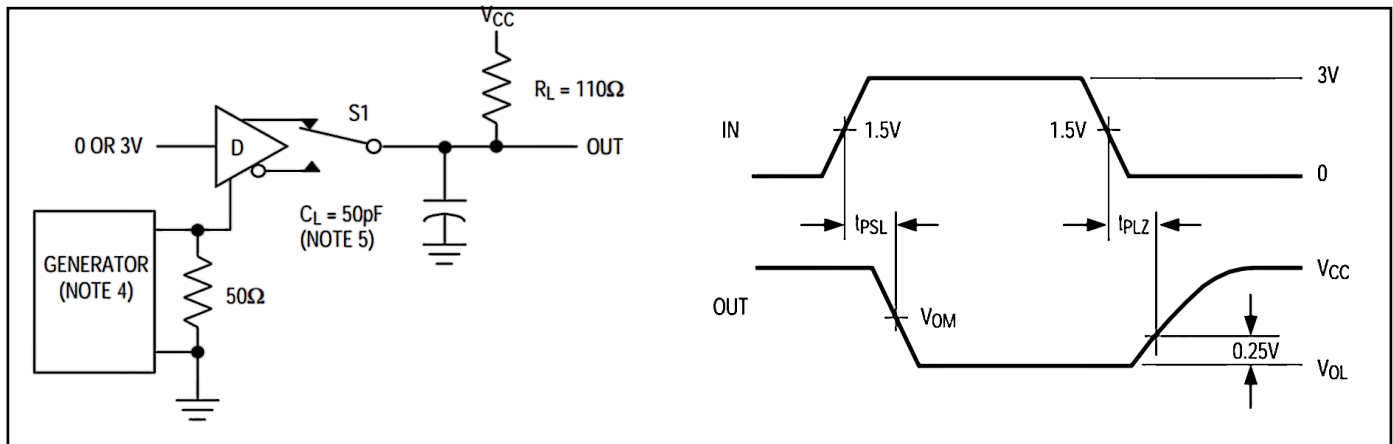


Figure 6 Drive enable and disable time

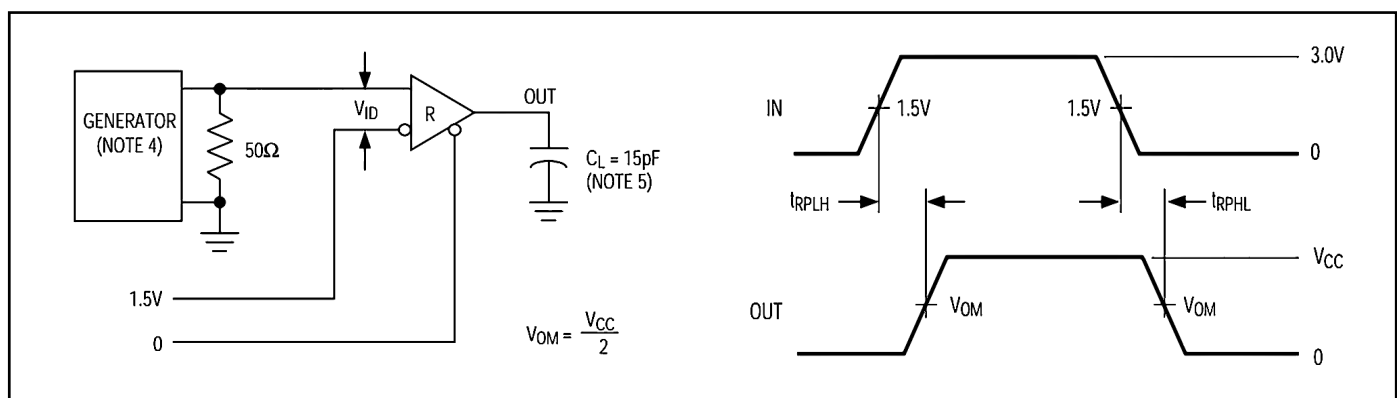
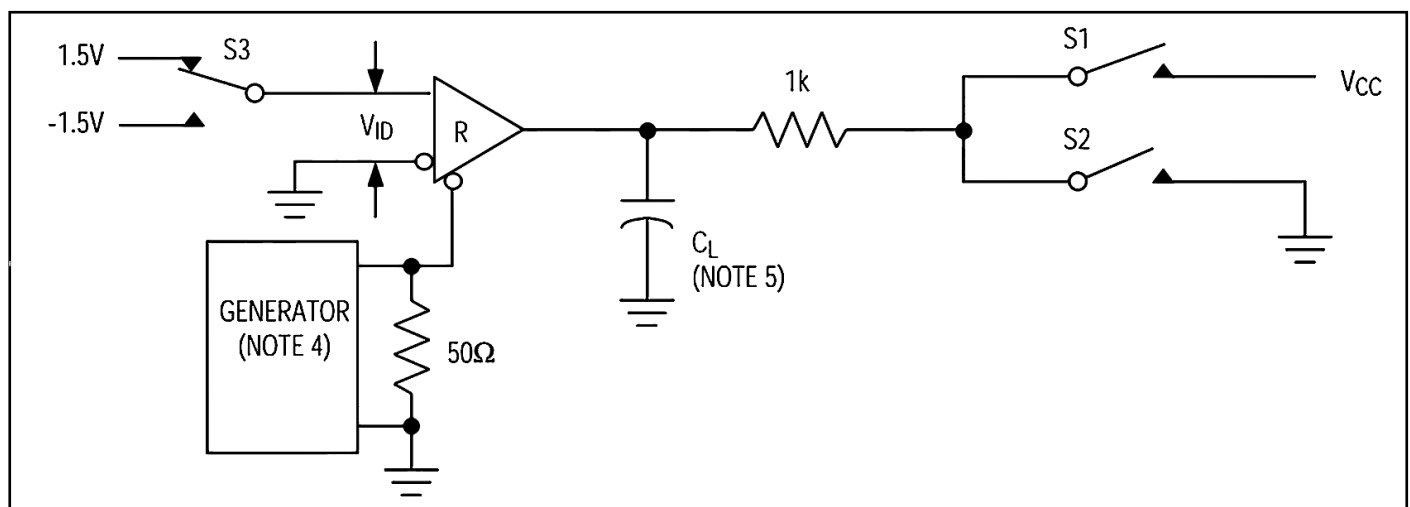


Figure 7: Receiver Propagation Delay Test Circuit



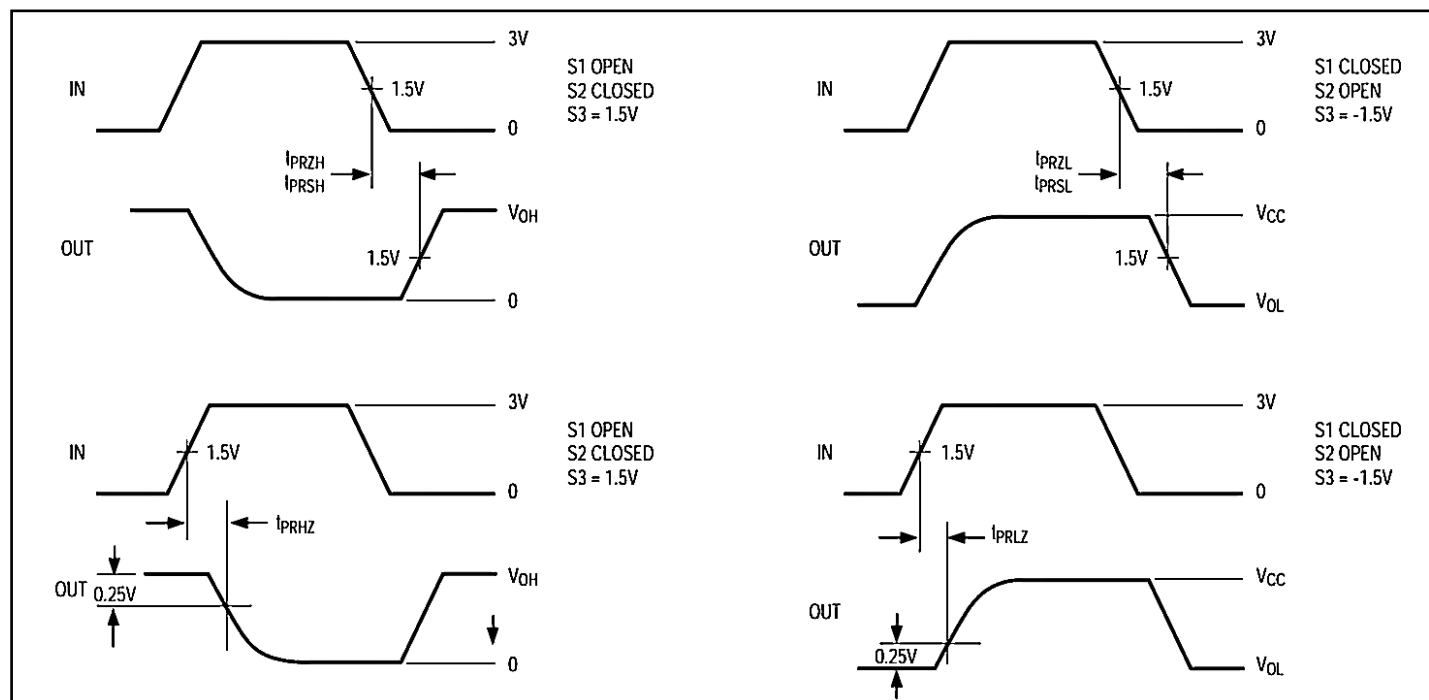
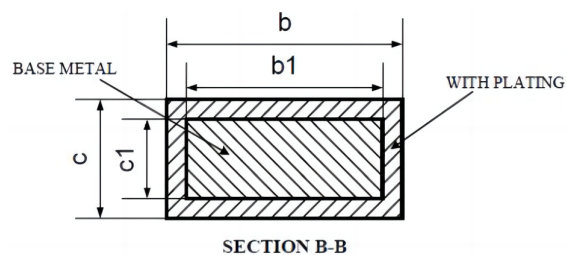
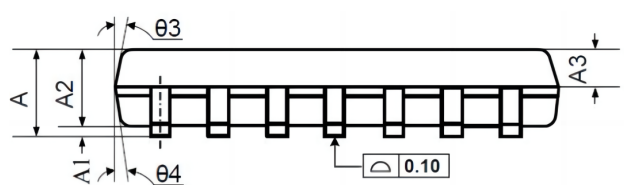
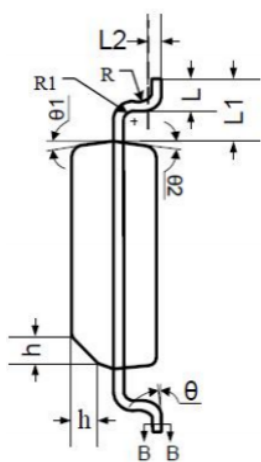
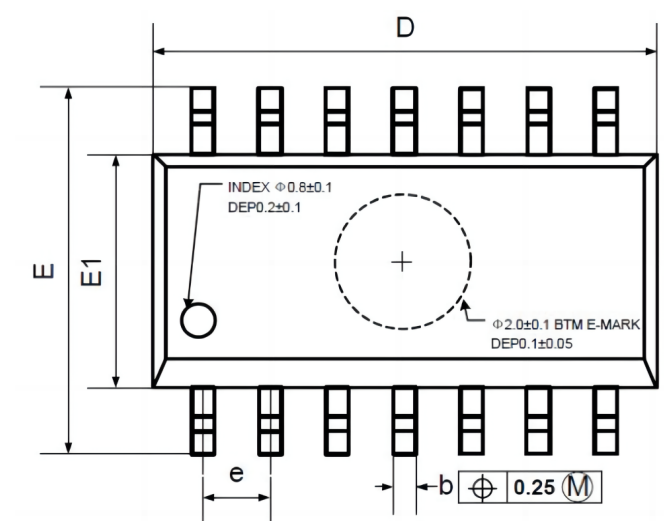


Figure 8 Receive enable and disable time

Order information

Order Number	Package	Package Quantity	Marking On The park	Temperature
MAX491ECPD-TUDI	DIP14	Tube,25,A box of 1000	MAX491ECPD	0°C to 70°C
MAX491ECSD-TUDI	SOP14	Tape,Reel,2500	MAX491ECSD	
MAX491ECPD-TUDI	DIP14	Tube,25,A box of 1000	MAX491ECPD	- 40°C to 85°C
MAX491EESD-TUDI	SOP14	Tape,Reel,2500	MAX491EESD	

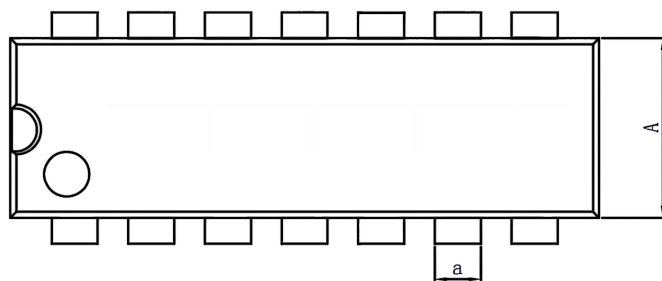
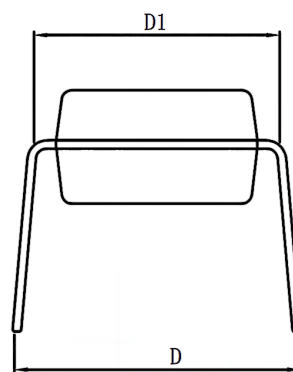
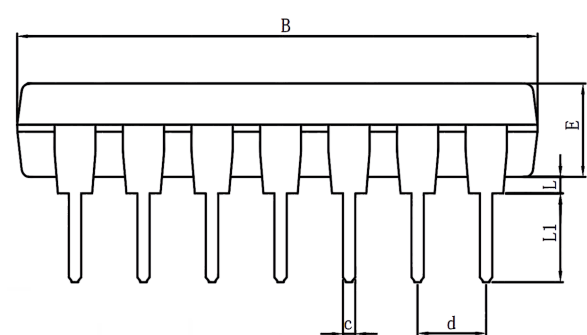
Package SOP14



Symbol	Dimensions In Millimeters		
	MIN	NOM	MAX
A	1.35	1.60	1.75
A1	0.10	0.15	0.25
A2	1.25	1.45	1.65
A3	0.55	0.65	0.75
b	0.36		0.49
b1	0.35	0.40	0.45
C	0.16		0.25
c1	0.15	0.20	0.25
D	8.53	8.63	8.73
E	5.80	6.00	6.20
E1	3.80	3.90	4.00
e	1.27 BSC		
L	0.45	0.60	0.80
L1	1.04 REF		
L2	0.25 BSC		
R	0.07		
R1	0.07		
h	0.30	0.40	0.50
θ	0°		8°
θ1	6°	8°	10°
θ2	6°	8°	10°
θ3	5°	7°	9°
θ4	5°	7°	9°



Package DIP14



DIM.	MIN	TYP	MAX	DIM.	MIN	TYP	MAX
A	6.100	6.300	6.680	a	1.504	1.524	1.544
B	18.940	19.200	19.560	C	0.437	0.457	0.477
D	8.200	8.700	9.200	d	2.530	2.540	2.550
D1	7.42	7.62	7.82	L	0.500	—	0.800
E	3.100	3.300	3.550	L1	3.000	3.200	3.600



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