



钜地半导体
Tudi Semiconductor

Product Specification

TUDI-TJA1043

Low-power CAN FD bus transceiver with
wake-up and fault protection

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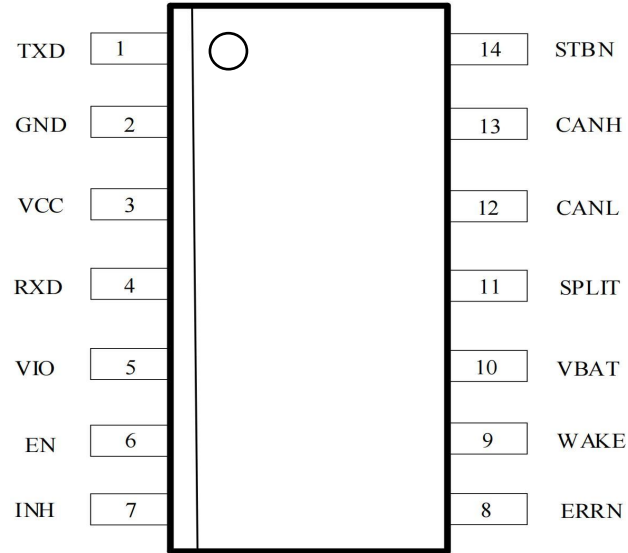
**semiconductor device
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- Design
- research and development
- production
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Features

- Fully compliant with the "ISO 11898-2:2016" standard
- Features low-power sleep mode and standby mode
- With remote and local wake-up functions
- Bus port withstands voltage of ± 58 V
- ± 30 V receiver common-mode input voltage
- The IO port supports a 3.3V/5V MCU.
- Driver (TXD) Explicit Timeout Function
- The VBAT, VCC, and VIO power pins feature under-voltage protection.
- High-speed CAN, supporting 5 Mbps CAN with Flexible Data Rate
- The INH output pin for sleep mode has a power disable function.
- Operates within a temperature range of -40°C to 150°C , with built-in overtemperature protection.
- The typical loop delay from TXD to RXD is approximately 100 ns.
- High resistance to electromagnetic interference
- Nodes that are not powered on do not interfere with the bus.
- With common-mode stable output pin SPLIT
- SOP14 packaging



Pin Diagram

Description

The TJA1043 is an interface chip designed for use between CAN protocol controllers and physical buses, supporting a flexible data rate of 5 Mbps and enabling differential signal transmission between the bus and the controller. Its bus port withstands voltages ranging from -58 V to $+58$ V, while the receiver's common-mode input voltage ranges from -30 V to $+30$ V, making it suitable for 12 V or 24 V applications. The chip features multiple power supply options and comprehensive system protection and diagnostic functions to enhance both device and CAN bus stability. Additionally, the TJA1043 offers five operating modes—normal, silent, standby, sleep-wait, and sleep—which support local and remote wake-up in low-power mode, significantly reducing power consumption in CAN bus systems.

Application

- Body Control Module
- Advanced Driver Assistance Systems (ADAS)
- Automotive Gateway
- Infotainment



Pin Definitions

Pin Number	Pin Name	Pin Functions
1	TXD	Sender Data Input Port
2	GND	The earth
3	VCC	5V Bus Power Supply
4	RXD	Receiver Data Output Port
5	VIO	Power supply for the I/O port
6	EN	Enable Control Input Port
7	INH	Used to control the operating state of the external voltage regulator ;set to high level after a wake-up event occurs.
8	ERRN	Error Instruction Output Port
9	WAKE	Local Wake Input Port
10	VBAT	Battery-powered power supply
11	SPLIT	Bus Common Mode Stable Output Port
12	CANL	Low-voltage CAN bus input/output terminals
13	CANH	High-voltage CAN bus input/output terminals
14	STBN	Standby Control Input Port



Structured Flowchart

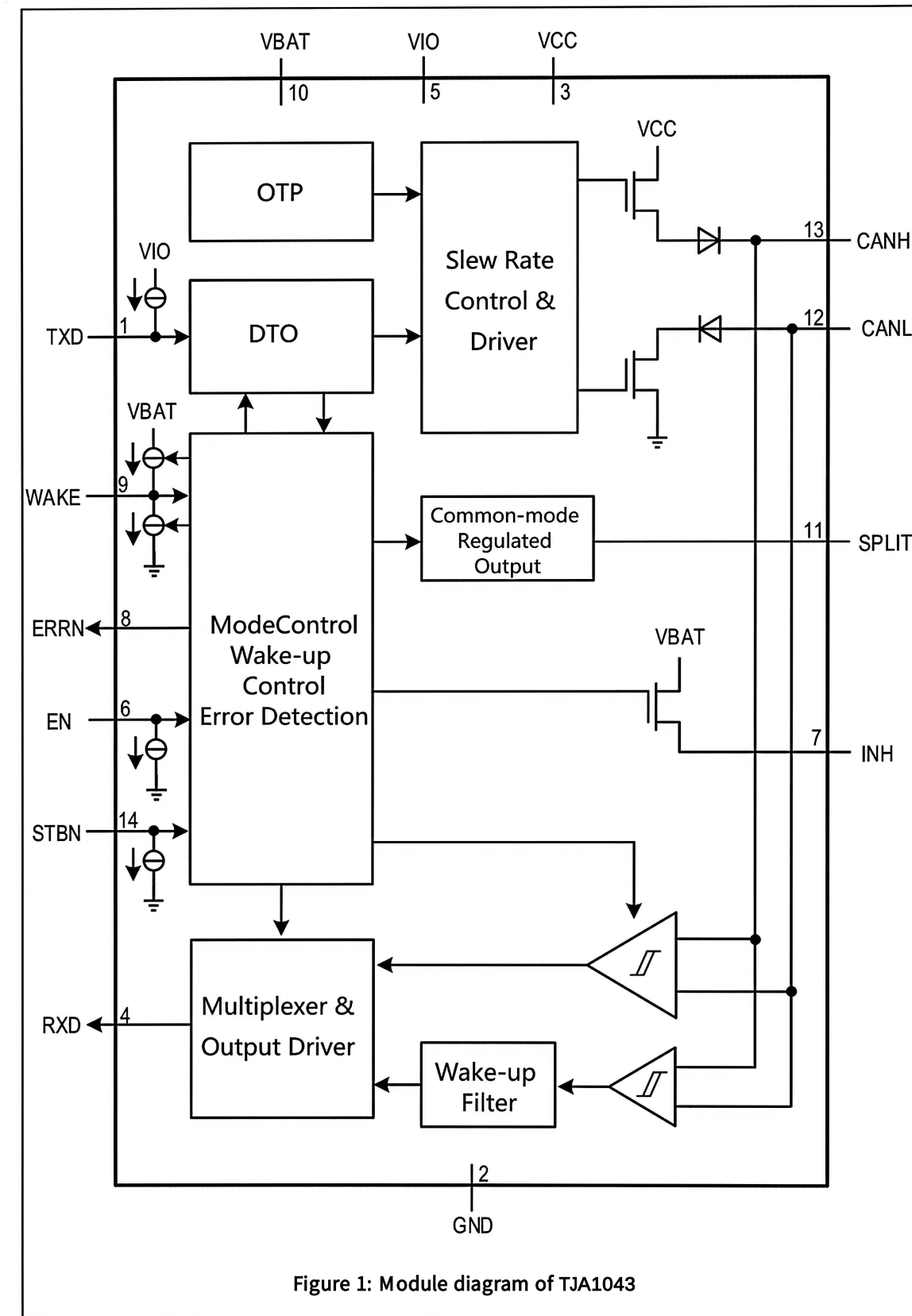


Figure 1: Module diagram of TJA1043



Recommended Work Status

Parameter	Symbol	Big or small	Unit
VBAT Power Supply Voltage	VBAT	4.5~40	V
VCC service voltage	VCC	4.5~5.5	V
VIO service voltage	VIO	2.8~5.5	V
High-level output current of logic output pins(RXD&ERRN)	$I_{OH(Logic)}$	>-2	mA
Low-level output current of the logic output pin(RXD&ERRN)	$I_{OL(Logic)}$	<2	mA
INH output	$I_{O(INH)}$	<1	mA
Operating ambient temperature	T_A	-40~150	°C

Limit Parameter

Parameter	Symbol	Big or small	Unit
Battery Power Supply Voltage	VBAT	-0.3~+58	V
Bus power supply voltage	VCC	-0.3~+6	V
MCU Side Port	TXD,RXD,ENSTBN, VIO,ERRN	-0.3~+6	V
Bus-side input voltage	CANH,CANL	-58~+58	V
Bus differential input voltage	V(CANH-CANL)	-20~+20	V
Storage Operating Temperature Range		-55~150	°C
Junction temperature		-40~150	°C

Maximum limit parameter values are those beyond which the device may suffer irreversible damage. Operating under these conditions compromises normal functionality, and continuous operation at maximum allowable ratings may affect reliability. All voltage measurements are referenced to ground.

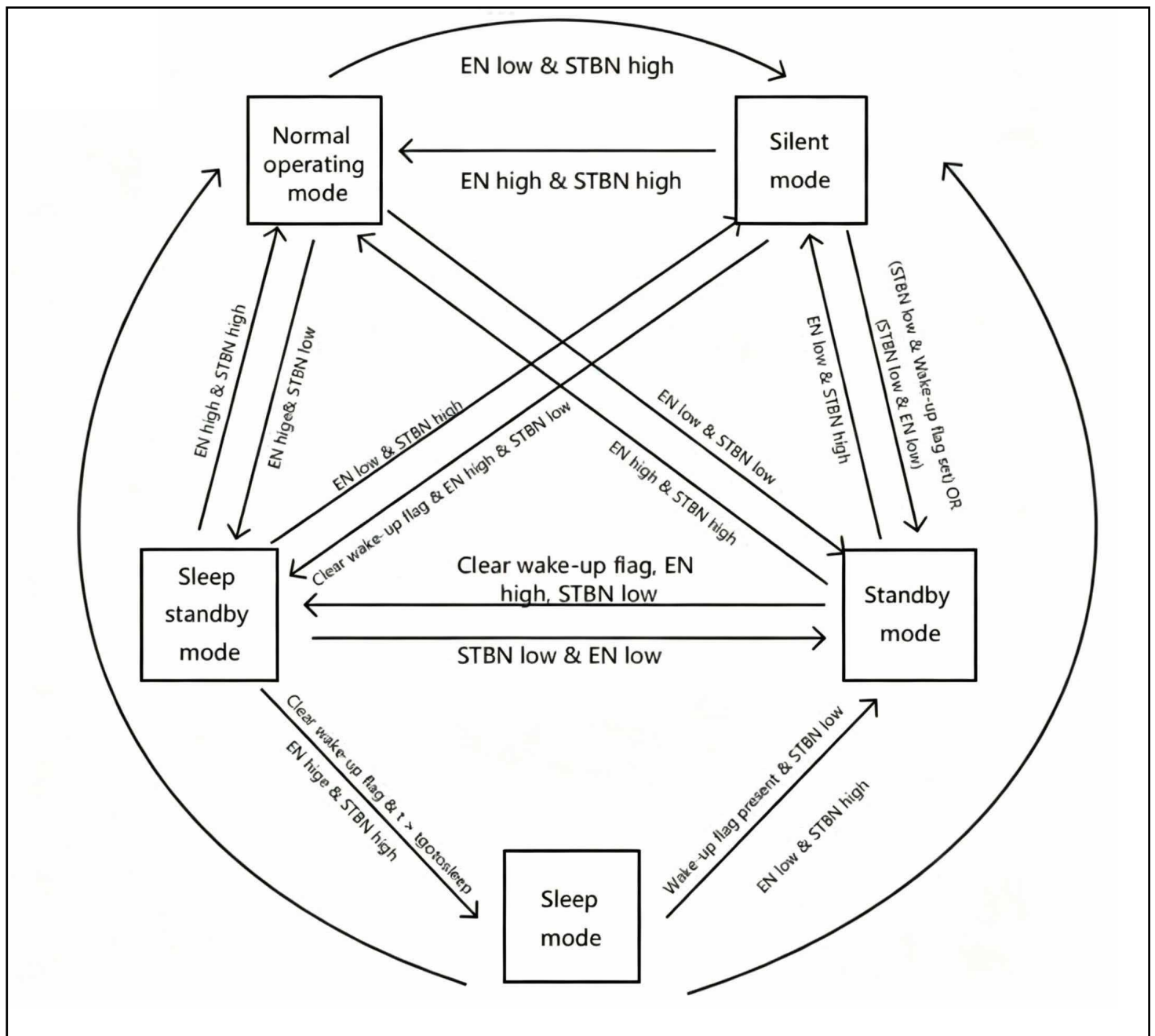


Figure 2: Pattern Switching Diagram

Note: The power ports VBAT, VCC, and VIO are properly powered.



Work Pattern

Normal Operating Mode

When the power supply is properly connected and both EN and STBN are set to high level, the device enters normal operating mode. In this mode, the driver and high-speed receiver are enabled: the driver converts the digital input signal on TXD into a bus analog level, while the receiver monitors the bus level and transmits it to port RXD. During normal operation, INH remains elevated.

Silence Mode

When powered normally, set EN to low level and STBN to high level to activate silent mode (also known as listen-only or receive-only mode). In this mode, the driver is disabled while the high-speed receiver remains enabled; explicit and implicit signals from CANH and CANL are transmitted via the receiver to the RXD port, the bus voltage is set to 0.5 VCC, and INH is pulled high.

Standby mode

When powered normally, setting both EN and STBN to low level puts the device into standby mode—a low-power state where the driver and high-speed receiver are disabled, INH is set high, yet the device remains capable of detecting local and remote wake-up events. Additionally, VBAT under-voltage conditions also trigger standby mode, though the device does not detect wake-up events during this state.

Sleep Wait Mode

The power supply is operating normally; set EN to high and STBN to low. When $t < t_{go-to-slep}$, the device enters a sleep-wait mode, which serves as an intermediate state before transitioning to sleep mode. In this mode, the transceiver operates similarly to standby mode: the driver and high-speed receiver are disabled, and INH remains high. If the duration in this mode exceeds $t_{go-to-sleep}$, the device switches to sleep mode, and INH transitions to a high-impedance state.

Sleep Mode

The device operates with normal power supply; set EN to high and STBN to low. Sleep mode can be activated when $t > t_{go-to-slep}$. Sleep mode is the lowest-power operating state; during this mode, the driver and high-speed receiver are disabled, the output port INH remains in a high-impedance state (indicating external voltage regulator disconnection), and both the transceiver and MCU's VCC power supply become unavailable. In this state, TJA1043 maintains power supply via battery pin VBAT to ensure local and remote wake-up monitoring functions. Additionally, if either VCC or VIO experiences undervoltage lasting longer than t_{DETUVD} , the device enters sleep mode with INH in high-impedance state; local or remote wake-up events can activate INH to switch it to high impedance.



Function Mode Table

VCC or VIO	VABT	EN	STB N	Wake-up Flag	Pattern	Actuator	High speed Acceptor	Low Power Power Consumption Collection	RXD	Bus State	INH
Normal	Normal	H	H	X	Normal Work Pattern	Enable	Enable	Forbidden energy	Following Bus	VCC/2	H
Normal	Normal	L	H	X	Loudspeaker mute Pattern	Forbidden energy	Enable	Forbidden energy	Following Highway	VCC/2	H
Normal	Normal	H	L	Clean up	Sleep Wait Pattern	Forbidden energy	Forbidden energy	Enable	H	GND	H
Normal	Normal	H	L	Clean up	Sleep Pattern	Forbidden energy	Forbidden energy	Enable	H	GND	Z
Normal	Normal	H	L	Set up	Await the opportunity moment Pattern	Forbidden energy	Forbidden energy	Enable	L	GND	H



Normal	Normal	L	L	Clean up	Await the opportune moment Pattern	Forbidden energy	Forbidden energy	Enable	H	GND	H
Normal	Normal	L	L	Set up	Await the opportune moment Pattern	Forbidden energy	Forbidden energy	Enable	L	GND	H
Undervoltage	Normal	X	X	X	Sleep Pattern	Forbidden energy	Forbidden energy	Enable	H	GND	Z
Normal	Undervoltage	X	X	X	Await the opportune moment Pattern	Forbidden energy	Forbidden energy	Forbidden energy	H	Z	H

Note: H = high level; L = low level; Z = high impedance state; X = irrelevant.

Driver Status Table

Work pattern	TXD import	Bus out		Bus Driver State
		CANH	CANL	
Normal Operating Mode	L	H	L	Dominant
	H perhaps Open	Z	Z	Bus voltage set to $VCC/2$
Silence Mode	X	Z	Z	Bus voltage set to $VCC/2$
Standby mode	X	Z	Z	Bus is biased to GND
Sleep Wait Mode	X	Z	Z	Bus is biased to GND
Sleep Mode	X	Z	Z	Bus is biased to GND

Note: H = high level; L = low level; Z = high impedance state; X = irrelevant.



Receiver Function Table

Work pattern	Bus Differential Input $V_{OD}=CANH-CANL$	Bus State	RXD output
Normal Operating Mode and Silent Mode	$V_{OD} \geq 0.9V$	Dominant	L
	$0.9V > V_{OD} > 0.5V$	?	X
	$V_{OD} \leq 0.5V$	Latent	H
Standby mode, Sleep Wait mode, and Sleep mode	$V_{OD} \geq 1.15V$	Dominant	H: When the wake-up flag appears, it is set to L
	$1.15V > V_{OD} > 0.4V$	?	
	$V_{OD} \leq 0.4V$	Latent	

Note: H = high level; L = low level; ? = uncertain; power supply is normal.

Internal Identification Signal

Marking signal	Causes	External Instruction	Clear the signal flag	Remarks
Shanghai Electric Logo	VBAT power on	Enter silent mode (from standby, sleep, etc.) Mode (Active Mode, Sleep Mode) ERRN=L	Enter normal operating mode	
Wake Request Flag	Remote Wake, Local Wake, Initial Power-Up	Enter standby mode, sleep wait mode, or sleep mode (ERRN = RXD=L)	Entering normal operating mode: VCC or VIO voltage is too low	
Wake-up Source Flag(1)	Remote Wake, Local Wake, Initial Power-Up	Enter normal operating mode: ERRN=L indicates local wake-up, ERRN=H indicates remote wake-up	Under normal operating mode, TXD experiences a transition(2), departing from the normal operating state, with VCC or VIO under-voltage.	The establishment of the power-on flag sets the wake-up source flag.



UVDNoMUnder-voltage indicator	VCC undervoltage	No external indication	VCC has been restored;awake-up request flag hasappeared.	
	VIO undervoltage	No external indication	VIO restored; Wakerequest flag appears	
UVDvBAT Undervoltage Flag	VBAT undervoltage	No external indication	VBAT recover	
Bus short-circuit indicator	The bus shorts to anypower supply or GND	Only in normal operat-ing mode (ERRN=L3)	Exit normal working mode	If the short-circuit duration is less than fourTXD explicit/ implicittransitions, they willnot be detected.
Local Error Flag	TXD Dominant Timeout	When switching from normal operatingmode to silent mode, ERRN=L	RXD=L&TXD=H; Enternormal operating mode	Once a TXD dominanttimeout occurs,the driver will be disabl-ed.
	TXD short-circuited to RXD			Once a TXD shortcircuit occurs to theRXD,the driver willbe disabled.
	Bus explicit timeout		RXD=H;enters normal operating mode	Bus timeout occurred while the dri-ver remains enab-led
	Overheat Protection		When junction temper-ature returns to normaland RXD=L&TXD=H; when junction tempera-ture returns to normaland the system reverts tonormal operating mode	Once a overheatingcondition occurs,the drive will be disabled.

(1) The wake-up flag recognizes only the first wake-up request signal.

(2) Four dominant-recessive transitions of TXD are observed, with each dominant-recessive cycle lasting at least 4 μ s.

(3) ERRN may only indicate a bus short circuit after four dominant-to-recessive transitions of TXD occur (each dominant-to-recessive cycle lasting at least 4 μ s).



The device performs system diagnostics internally using the aforementioned series of flag signals and identifies the cause of faults. The MCU can determine the system's operational status or the root cause of failures by switching between modes and monitoring the indications on the transceiver chip's ERRN and RXD pins.

Power-on flag

The power-on flag specifically refers to the power-on event of the battery power supply VBAT. This flag is set when VBAT recovers from a voltage below to the normal operating voltage. When the device transitions from standby or sleep mode to silent mode, ERRN is pulled low to indicate that the power-on flag has been set; it is cleared upon returning to normal operation. The power-on flag also clears the under-voltage flag and sets both the wake-up request flag and the wake-up source flag.

Wake-up request flag

The TJA1043 supports low-power wake-up functionality in two ways: local wake-up and remote wake-up.

Local Wakeup

The TJA1043 supports local wake-up functionality via the WAKE port. In standby or sleep mode, any valid rising or falling edge on the WAKE pin is detected as a local wake-up event.

An effective rising edge refers to the voltage at the WAKE port jumping from a level below $V_{th(WAKE)}$ to a level above $V_{th(WAKE)}$, with the duration of this jump exceeding $t_{wake(local)}$; such an edge is considered an effective rising edge, as shown in Figure 3. An effective falling edge refers to the voltage at the WAKE port jumping from a level above $V_{th(WAKE)}$ to a level below $V_{th(WAKE)}$, with the duration of this jump exceeding $t_{wake(local)}$; such an edge is considered an effective falling edge, as shown in Figure 4. Any transitions with a duration less than $t_{wake(local)}$ and those that do not exceed the threshold voltage $V_{th(WAKE)}$ will be filtered out.

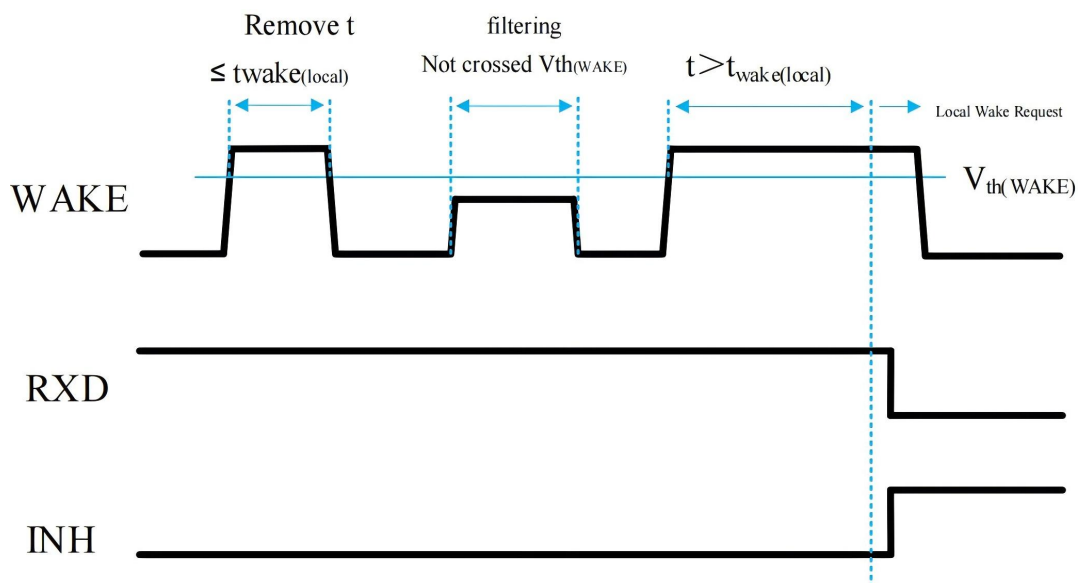


Figure 3 Schematic Diagram of Local Wake-up During the Rising Edge of WAKE

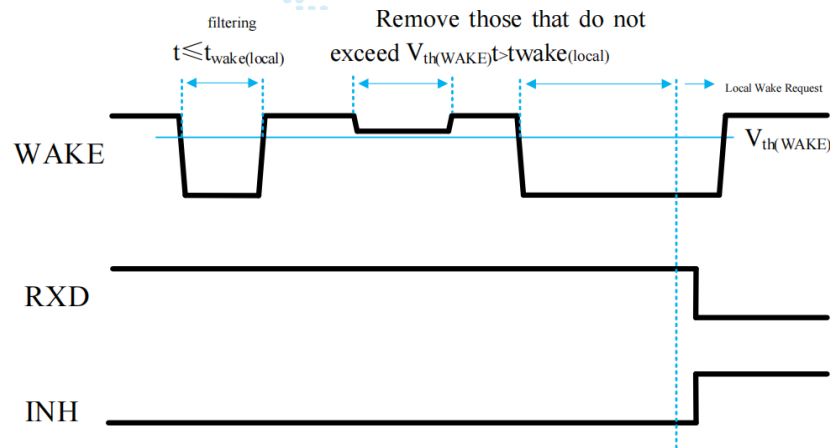


Figure 4: Schematic Diagram of the Local Wake-up Process Along the WAKE Descent Path

Remote Wakeup

The TJA1043 features a low-power receiver for remote wake-up functionality, notifying the MCU that the bus is activated and the node should resume normal operation. During sleep mode, upon receiving a valid Remote Wake-Up Request (WUP) signal, the device wakes up and transitions to standby mode, with RXD pulled low and INH pulled high.

According to ISO 11898-2:2016, a complete WUP includes: a filtered explicit level segment (with duration greater than $t_{wake(dom)}$), a filtered implicit level segment (with duration greater than $t_{wake(rec)}$), and another filtered explicit level segment (with duration greater than $t_{wake(dom)}$). This explicit-implicit-explicit level signal sequence must occur within the $t_{wake(timeout)}$ period; otherwise, the internal wake-up logic will be reset and bus monitoring will restart.

The RXD pin remains at a high level until a wake-up event is triggered. Both the explicit and implicit levels mentioned above will be ignored (filtered out) if their duration is shorter than $t_{wake(busdom)}$ OR $t_{wake(busrec)}$. The system will not respond to a wake-up event if any of the following conditions occur upon receiving a valid wake-up signal:

- (1) The device has switched to normal operating mode;
- (2) The complete wake request frame was not received within the $t_{wake(timeout)}$;
- (3) Undervoltage detected on VCC or VIO (UVDNOM flag signal set).

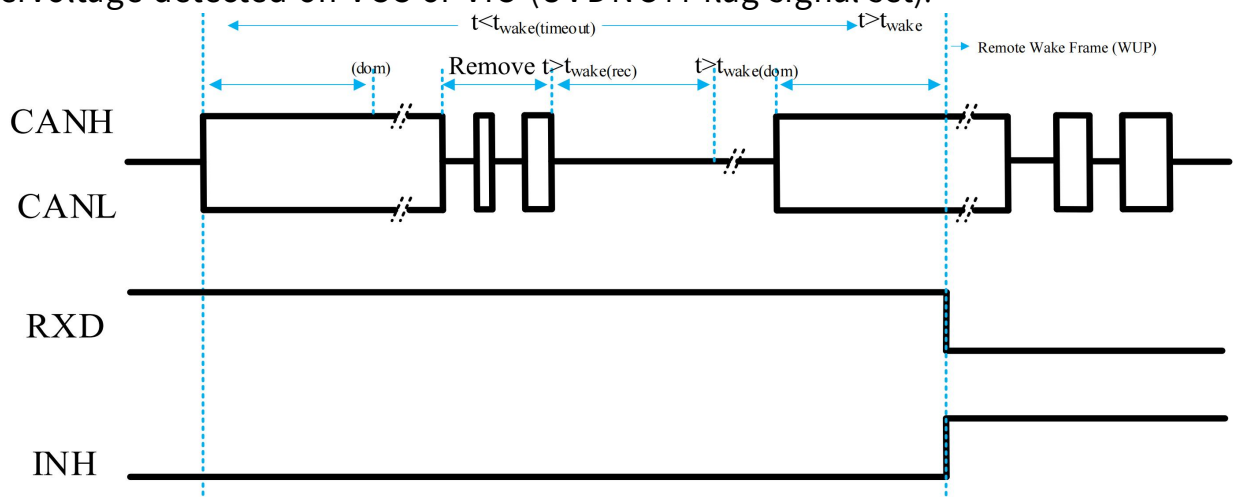


Figure 5 Schematic Diagram of Remote Wake-Up



Wake-up Source Identifier

The TJA1043 identifies the wake-up source via a wake-up flag, which is indicated by the voltage level at the ERRN pin when the chip enters normal operation mode. When a local wake-up request sent through the WAKE pin generates a wake-up flag, the ERRN pin transitions to a low level upon switching to normal mode; conversely, a high-level ERRN pin indicates a remote wake-up signal from the CAN bus. During normal operation, if a bus short-circuit flag is triggered after four transmit/detect transitions on the TXD port, it overrides the wake-up flag.

The wake-up flag is also cleared when the chip exits normal operation mode and is initially set upon power-on.

UVD_{NOM} Under-voltage indicator

The power supplies VCC and VIO of TJA1043 feature under-voltage detection functionality, which enables the setting of an UVD_{NOM} under-voltage flag to place the device in a protected state. When VCC falls below its under-voltage threshold V_{UVDVCC} for a duration exceeding $t_{DETUV D}$, or when VIO falls below its under-voltage threshold V_{UVDVIO} for a duration exceeding $t_{DETUV D}$, the device is forcibly entered into sleep mode via the activation of the UVD_{NOM} under-voltage flag; local and remote wake-up functions remain unaffected, while INH remains in high-impedance state indicating shutdown of the external voltage regulator, thereby reducing unnecessary power consumption and preventing bus interference. When VCC exceeds V_{UVDVCC} for a recovery period longer than t_{RECUVD} , or when VIO exceeds V_{UVDVIO} for a recovery period longer than $t_{DETUV D}$, the UVD_{NOM} under-voltage flag is cleared. Meanwhile, the establishment of the wake-up request flag and power-on flag, as well as transitions from low to high on the STB, will clear the UVD_{NOM} under-voltage flag.

UVD_{VBAT} Undervoltage Flag

The battery power supply VBAT of TJA1043 also features a voltage-low detection function. When VBAT falls below $V_{UVDVBAT}$, the UVD_{VBAT} voltage-low flag is set, causing the device to enter standby mode and disconnecting the transceiver from the bus (zero load). Upon recovery of VBAT voltage, the UVD_{VBAT} voltage-low flag is cleared, and the transceiver switches to operation mode determined by the logic levels on pins STBN and EN.

Bus short-circuit indicator

In normal operating mode, if the bus shorts to VBAT, VCC, or GND and the TXD pin experiences four consecutive visible-to-masked transitions (each cycle lasting at least 4 μs), the bus short-circuit flag is set; pulling ERRN low activates this flag. The flag is cleared upon power recovery or when the transceiver returns to normal operation.



Local Error Flag

The TJA1043 detects four local error events: TXD explicit timeout, TXD/RXD short circuit, bus explicit timeout, and overtemperature protection. When any of these events occurs, a local error flag is generated. Upon switching from normal operation to silent mode, ERRN is pulled low, indicating the occurrence of a local error flag.

TXD Dominant Timeout

In normal operating mode, if the low-level duration on pin TXD exceeds the internal timer value $t_{dom}(TXD)$, the transmitter is disabled and the drive bus enters a hidden state. This prevents pin TXD from being forcibly set to a permanent low level due to hardware or software failures, which could cause the bus to enter a permanent active state and block all network communications.

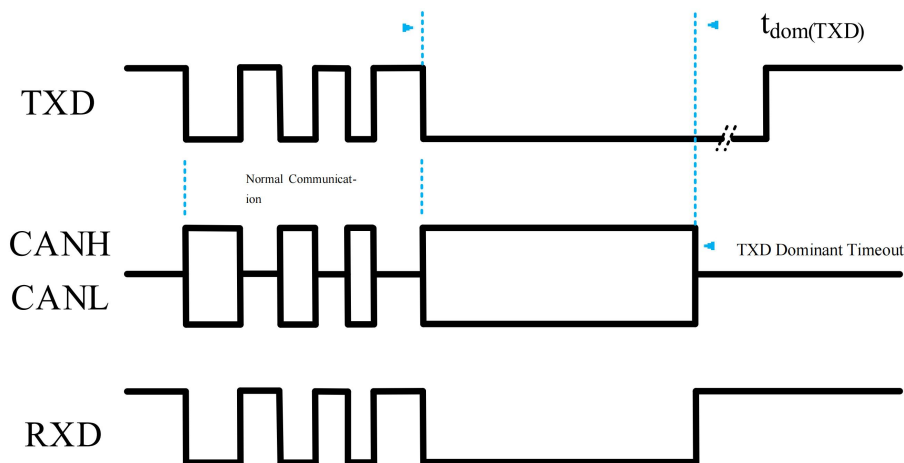


Figure 6 Schematic Diagram of TXD Dominant Timeout

TXD and RXD short circuit

The TJA1043 features protection against short circuits between the TXD and RXD pins, preventing periodic deadlocks in local components. Under normal operation or silent mode, if a short circuit occurs between the TXD and RXD pins and persists for longer than , the device detects a short circuit, sets a local error flag, and disables the driver.

Bus explicit timeout

When a short circuit occurs on the bus, if the duration of the short circuit exceeds the value $t_{dom}(BUS)$ set by the internal timer, it is recognized as a bus explicit timeout event, and a local error flag is raised.



Overheat Protection

The TJA1043 features an overtemperature protection function. If the device junction temperature exceeds the overtemperature shutdown threshold, the bus driver circuit is shut down, thereby cutting off the transmission path from TXD to the bus. During thermal shutdown, the CAN bus voltage remains at a low level, while other components of the chip continue to operate normally. Since the driver transistor is the primary power-consuming component, shutting it down reduces overall power consumption and lowers chip temperature.

DC Parameters

Testing was conducted under the recommended operating conditions: VBAT = 4.5 V to 40 V, VCC = 4.5 V to 5 V, VIO = 2.8 V to 5.5 V, and $T_{vj} = -40^{\circ}\text{C}$ to 150°C . Unless otherwise specified, all typical values were measured at 25°C with supply voltages of VBAT = 12 V, VCC = 5 V, VIO = 5 V, and $R_L = 60\ \Omega$.

Parameter	Symbol	Test condition	Minimum	Typical case	Maximum	Unit
Power Supply Characteristics						
VBAT Power Supply Current	IBAT	Normal Operating Mode Or Silent Mode	15	35	70	μA
		Standby mode, VCC > 4.5 V, VIO > 2.8 V, INH = WAKE = VBAT	5	16	30	μA
		Sleep Mode, VCC = VIO = INH = 0 V, WAKE = VBAT	5	16	30	μA



Parameter	Symbol	Test condition	Minimum	Typical case	Maximum	Unit
Power Supply Characteristics						
VCC supply current	I _{CC}	Dominant in normal functioning	30	48	65	mA
		Operates in silent or quietmode under normal condi-tions	3	6	9	mA
		Standby Mode orSleep Pattern of the Individual		1	4	μA
		Normal operation is dominant;busshort-circuited:-3V <(CANH =CANL)<+18V	3	79	109	mA
VIO supply current	I _{IO}	Dominant phenotypeunder normal condi-tions, TXD=0V		150	500	μA
		In normal operation, itoperates in silent orquiet mode;TXD=VIO		1	2	μA
		Standby Mode orSleep Pattern of the Individual		1	2	μA
VBAT Undervoltage Detection	V _{UVD} VBAT		3	3.5	4.3	V
VCC Undervoltage Detection	V _{UVD} VCC	VBAT>4.5V	3	3.5	4.3	V
VIO Under-voltage Detection	V _{UVD} VIO	VBAT>4.5V	1.5	1.8	2.1	V



Parameter	Symbol	Test condition	Minimum	Typical case	Maximum	Unit
TXD Port Characteristics						
TXD port high-level input current	$I_{IH(TXD)}$	TXD=VIO	-5	0	5	μA
TXD port low-level input current	$I_{IL(TXD)}$	TXD=0V	-260	-150	-30	μA
Leakage current of TXD when not powered on	$I_{off(TXD)}$	VIO=0V, TXD=5.5V	-1		1	μA
Enter the high level lower limit	V_{IH}		0.7VIO		VIO+0.3	V
Enter the low level upper limit	V_{IL}		-0.3		0.3VIO	V
RXD Port Characteristics						
RXD port high-level output current	$I_{OH(RXD)}$	RXD=VIO-0.4V	-12	-6	-1	mA
RXD port low-level output current	$I_{OL(RXD)}$	RXD=0.4 V, bus dominant	2	6	14	mA
STBN Port Characteristics						
STBN port high-level input current	$I_{IH(STBN)}$	STBN=VIO	1	5	10	μA
STBN port low-level input current	$I_{IL(STBN)}$	STBN=0V	-1		1	μA
Leakage current of STBN when not powered on	$I_{Off(STBN)}$	VIO=0V, STBN=5.5V	-1		1	μA
Enter the high level lower limit	V_{IH}		0.7VIO		VIO+0.3	V
Enter the low level upper limit	V_{IL}		-0.3		0.3VIO	V



Parameter	Symbol	Test condition	Minimum	Typical case	Maximum	Unit
EN Port Characteristics						
EN Port High-Level Input Current	$I_{IH}(EN)$	EN=VIO	1	5	10	μA
EN Port Low-Level Input Current	$I_{IL}(EN)$	EN=0V	-1		1	μA
Leakage current of EN when not powered on	$I_{Off}(EN)$	VIO=0V, EN=5.5V	-1		1	μA
Enter the high level lower limit	V_{IH}		0.7VIO		VIO+0.3	V
Enter the low level upper limit	V_{IL}		-0.3		0.3VIO	V
ERRN Port Characteristics						
ERRN port high-level output current	$I_{OH}(ERRN)$	ERRN=VIO-0.4V	-50	-20	-4	μA
ERRN port low-level output current	$I_{OL}(ERRN)$	ERRN=0.4V	0.1	0.5	2	mA
INH Port Characteristics						
High-level voltage difference at the INH port	ΔV^H	INH=-0.18mA	0	0.25	0.8	V
INH port leakage current	I_L	Sleep Mode	-2	0	2	μA
WAKE Port Characteristics						
WAKE Port High-Level Input Current	$I_{IH}(WAKE)$	WAKE=VBAT-1.8V	-18	-10		μA
WAKE port low-level input current	$I_{IL}(WAKE)$	WAKE=VBAT-3.6V		10	18	μA
WAKE High/Low Level Threshold	$V^{th}(WAKE)$	STBN=0	VBAT-3.5	VBAT-2.5	VBAT-1.9	V



Parameter	Symbol	Test condition	Minimum	Typical case	Maximum	Unit
SPLIT Port Characteristics						
SPLIT Port Output Voltage	V_{SPLIT}	Normal operating mode or silent mode- $500\mu A < I_{SPLIT} < 500\mu A$	0.3VCC	0.5VCC	0.7VCC	V
		Normal operating mode or silent mode $R_L = 1M\Omega$	0.45VCC	0.5VCC	0.55VCC	V
SPLIT port leakage current	I_L	Standby mode or sleep mode- $58V < V_{SPLIT} < 58V$	-3		3	μA
Overheat Protection						
Overheat Protection Circuit Breaker	$T_{j(sd)}$			190		$^{\circ}C$
Bus Driver DC Characteristics						
CANH Output Voltage (Dominant)	$V_{OH(D)}$	Normal operating mode: $TXD=0V, R_L=50\Omega$ to 65Ω	2.75	3.5	4.5	V
CANL Output Voltage (Dominant)	$V_{OL(D)}$		0.5	1.5	2.25	V
Bus output differential voltage (Dominant)	$V_{OD(D)}$	Normal operating mode: $TXD=0V, R_L=50\Omega$ to 65Ω	1.5		3	V
		Normal operating mode: $TXD=0V, R_L=45\Omega$ to 70Ω	1.4		3.3	V
		Normal operating mode: $TXD=0V, R_L=2240\Omega$	1.5		5	V
Bus Output Voltage (Implicit)	$V_{O(R)}$	Normal operating mode or silent mode; $TXD=V_{IO}$; no load	2	0.5VCC	3	V



Parameter	Symbol	Test condition	Minimum	Typical case	Maximum	Unit
Bus differential output voltage (Implicit)	$V_{OD(R)}$	Normal operating mode or silent mode, TXD = VIO; no load	-500		50	mV
Bus output voltage (bus biased to ground)	$V_{O(S)}$	Sleep mode or standby mode, no load	-0.1		0.1	V
Bus differential output voltage (bus offset to ground)	$V_{OD(S)}$	Sleep mode or standby mode, no load	-0.2		0.2	V
Symmetry of the dominant output voltage	$V_{dom(TX)sym}$	$V_{dom(TX)sym} = V_{CC} - CANH - CANL$	-400		400	mV
Output voltage symmetry	V_{TXsym}	$V_{TXsym} = CANH + CANL, R_L = 60\Omega, C_{sPLIT} = 4.7nF, f_{TXD} = 1MHz$	$0.9V_{CC}$		$1.1V_{CC}$	V
Dominant and recessive dominant modal output voltage difference	$V_{cm(step)}$	Graph 9	-150		150	mV
Dominant/Recessive Co-mode Peak Value	$V_{ecm(p-p)}$	Graph 9	-300		300	mV
Dominant short-circuit output current	$I_{o(sc)DOM}$	Normal operating mode: TXD = 0V, CANH = -15V to 40V	-100	-70	-40	mA
		Normal operating mode: TXD = 0V, CANL = -15V to 40V	40	70	100	mA



Parameter	Symbol	Test condition	Minimum	Typical case	Maximum	Unit
Hidden short-circuit output current	$I_{O(SC)REC}$	Normal operating mode :TXD=VIO; CANH=CANL=-27Vto 32V	-3		3	mA
Bus receiver DC characteristics						
Receiver threshold voltage	$V_{th(RX)dif}$	Normal operating mode or silent mode,-30V <VcM<30V	0.5		0.9	V
		Standby mode or sleep mode -12V<VcM<12V	0.4		1.15	V
Receiver threshold voltage hysteresis range	$V_{hys(RX)dif}$	Normal operating mode or silent mode,-30V<Vcm<30V	50	120	400	mV
Receiver implicit voltage range	$V_{rec(RX)}$	Normal operating mode or silent mode,-30V <VcM<30V	-3		0.5	V
		Standby mode or sleep mode -12V<VcM<12V	-3		0.4	V
Receiver's Explicit Voltage Range	$V_{dom(RX)}$	Normal operating mode or silent mode,-30V<VcM<30V	0.9		8	V
		Standby mode orsleep mode-12V<VcM<12V	1.15		8	V
Bus leakage current	I_L	VCC=VIO=VBAT=0V,CANH=CANL=5V	-5		5	μA



Parameter	Symbol	Test condition	Minimum	Typical case	Maximum	Unit
CANH,CANL input resistances	R^{IN}	$-2V \leq CANH \leq 7V$ $-2V \leq CANL \leq 7V$	9	15	28	k Ω
CANH,CANL differential input resistance	R^{ID}	$-2V \leq CANH \leq 7V$ $-2V \leq CANL \leq 7V$	19	30	52	k Ω
CANH and CANL input resistance mismatch degree	ΔR^{IN}	$0V \leq CANH \leq 5V$ $0V \leq CANL \leq 5V$	-3		3	%
CANH,CANL ground input capacitors	C^{IN}	TXD=VIO		24		pF
CANH,CANL differential input capacitors	C^{ID}	TXD=VIO		12		pF

Exchange Parameters

Unless otherwise specified, all typical values were measured under the following conditions: 25°C, power supply voltage VBAT = 12 V, VCC = 5 V, VIO = 5 V, RL = 60 Ω , CBUS = 100 pF, and CRXD = 15 pF

Parameter	Symbol	Test condition	Minimum	Typical case	Maximum	Unit
Drive AC Characteristics						
Propagation Delay (from low to high)	$t_{a(TXD-busdom)}$	Normal operating mode, Figure 7		45		ns
Propagation Delay (from high to low)	$t_{d(TXD-busrec)}$	Normal operating mode, Figure 7		55		ns
Differential output rise time	$t_r(BUS)$	Normal operating mode, Figure 7		45		ns
Differential output fall time	$t_f(BUS)$	Normal operating mode, Figure 7		45		ns
TXD Dominant Timeout Time	$t_{dom(TXD)}$	TXD=0, graph 6	0.3	0.6	1.2	ms



Parameter	Symbol	Test condition	Minimum	Typical case	Maximum	Unit
Receiver AC Characteristics						
Propagation Delay (from low to high)	$t_{a(busdom-RXD)}$	Normal operating mode or silent mode, Figure 7		45		ns
Propagation Delay (from high to low)	$t_{d(busrec-RXD)}$	Normal operating mode or silent mode, Figure 7		45		ns
RXD Signal Rise Time	$t_{r(RXD)}$	Normal operating mode or silent mode, Figure 7		8		ns
RXD Signal Fall Time	$t_{f(RXD)}$	Normal operating mode or silent mode, Figure 7		8		ns
BUS Dominant Timeout Time	$t_{dom(BUS)}$	VOD > 0.9V	0.3	0.6	1.2	ms
TXD to RXD loop delay						
Loop delay:1, from the falling edge of TXD to the falling edge of RXD	t_{oop1}	Normal operating mode, Figure 7	40		160	ns
Loop delay:2, from the rising edge of TXD to the rising edge of RXD	t_{oop2}	Normal operating mode, Figure 7	40		175	ns
CANFD Bit Time						
BUS Output Bit Time	$t_{bit(BUS)}$	$t_{bit(TXD)} = 500ns$, Figure 8	435		530	ns
		$t_{bit(TXD)} = 200ns$, Figure 8	155		210	ns



Parameter	Symbol	Test condition	Minimum	Typical case	Maximum	Unit
RXD Output Bit Time	t _{bit(RXD)}	bit(TXD)=500ns, Figure 8	400		550	ns
		t _{bit(TXD)} =200ns, Figure 8	120		220	ns
Time Difference Between BUS and RXD Output Bits	Δt _{ree}	Δt _{rec} =t _{bit(RXD)} -t _{bit(BUS):bit(TXD)} =500ns	-65		40	ns
		Δt _{rec} =t _{bit(RXD)} -t _{bit (BUS):bit (TXD)} =200ns	-45		15	ns
Device Switching Characteristics						
Sleep Wait Mode Duration	t _{go_to_sleep}	EN=VIO,STBN=0	20		60	μs
Remote Wake-up Explicit Time	t _{wake(dom)}	Sleep Mode or Device Standby Mode	0.5		1.8	μs
Remote Wake-Up Implicit Time	t _{wake(rec)}	Sleep Mode or Device Standby Mode	0.5		1.8	μs
Remote Wake Up Timeout Time	t _{wake(timeout)}		0.3	0.6	1.2	ms
Local Wake Up Time	t _{wake(local)}	Sleep Mode or Device Standby Mode	5	25	50	μs
Undervoltage detection time	t _{DETUV D}		100		350	ms
Undervoltage recovery time	t _{RECUVD}		1		5	ms
STBN and EN Port Filtering Time	t _{filter IO}		1		4	μs



Waveform Time Sequence Diagram

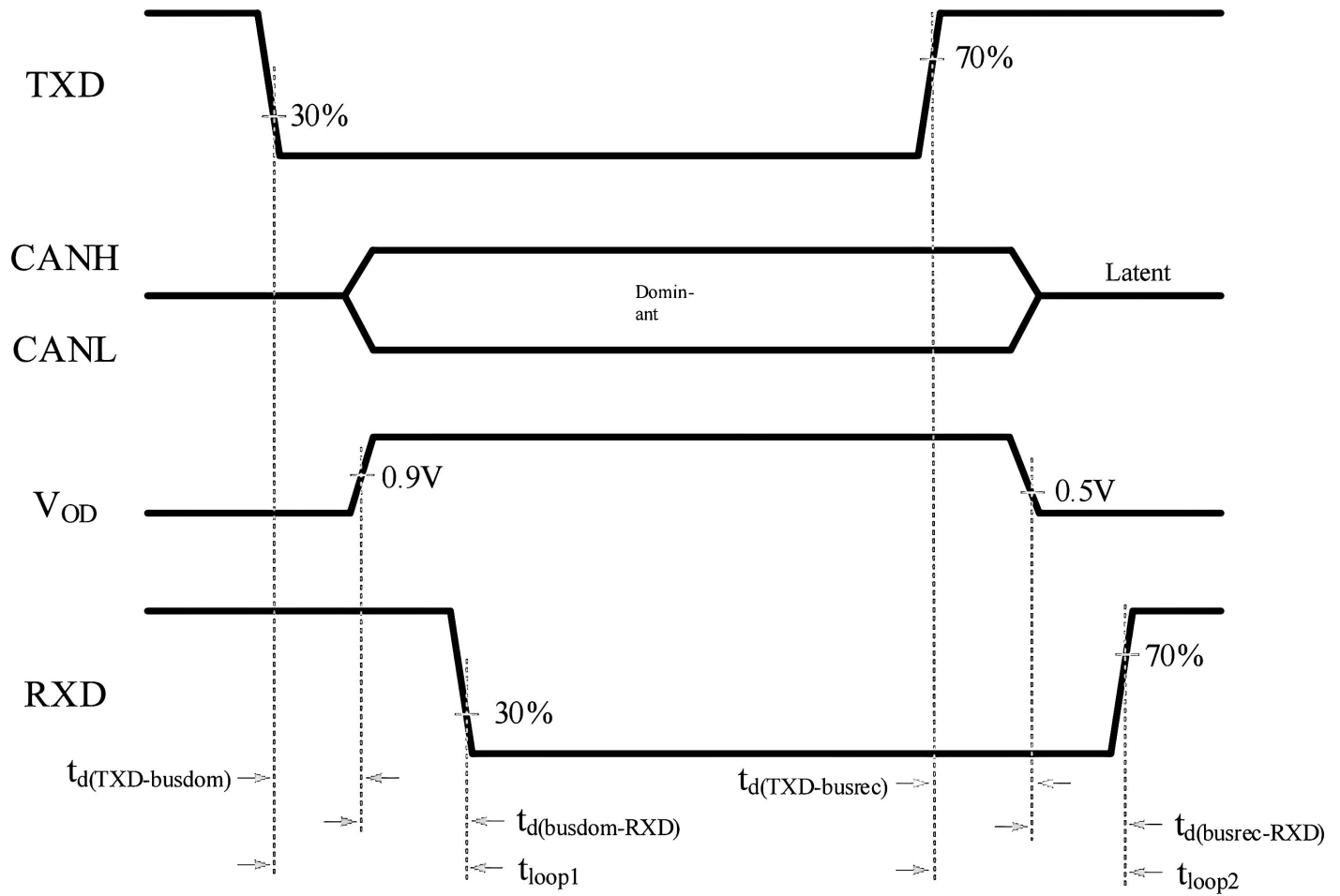


Figure 7 Schematic Diagram of Transmitter/receiver Transmission Delay

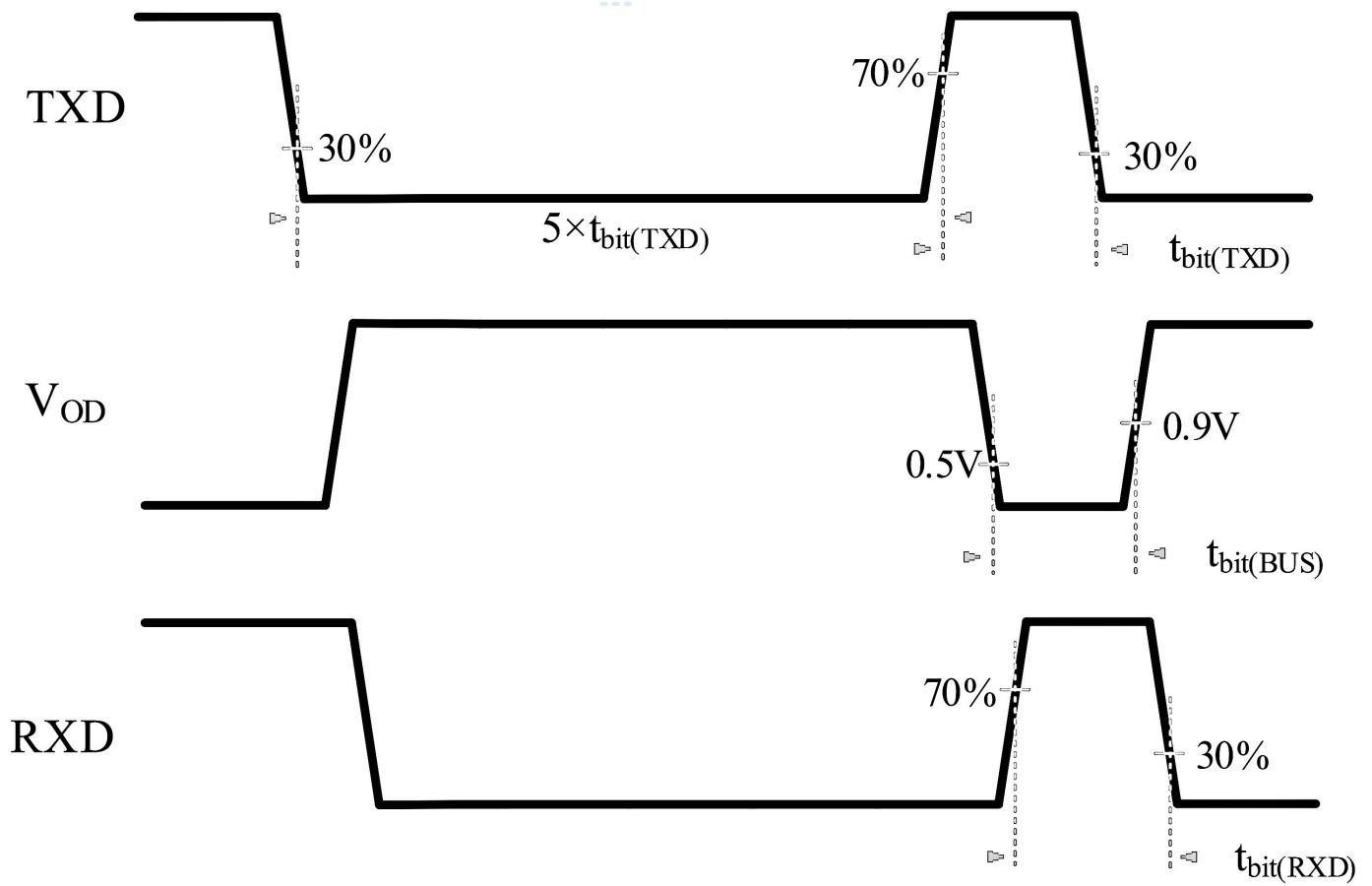


Figure 8: Schematic Diagram of Tbit Delay

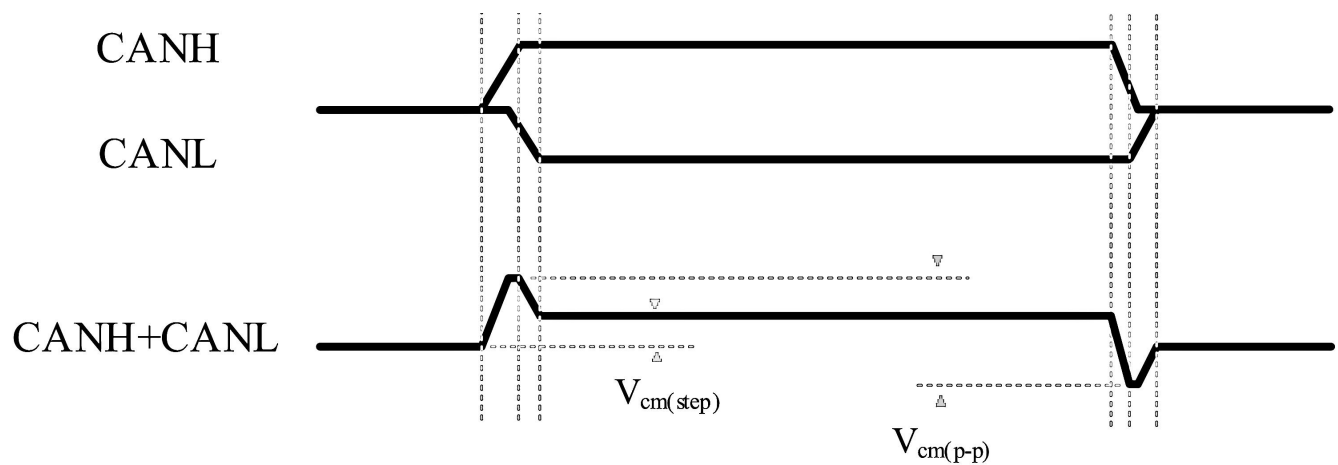


Figure 9 Bus Common-Mode Voltage (SAE 1939-14)

Typical Application

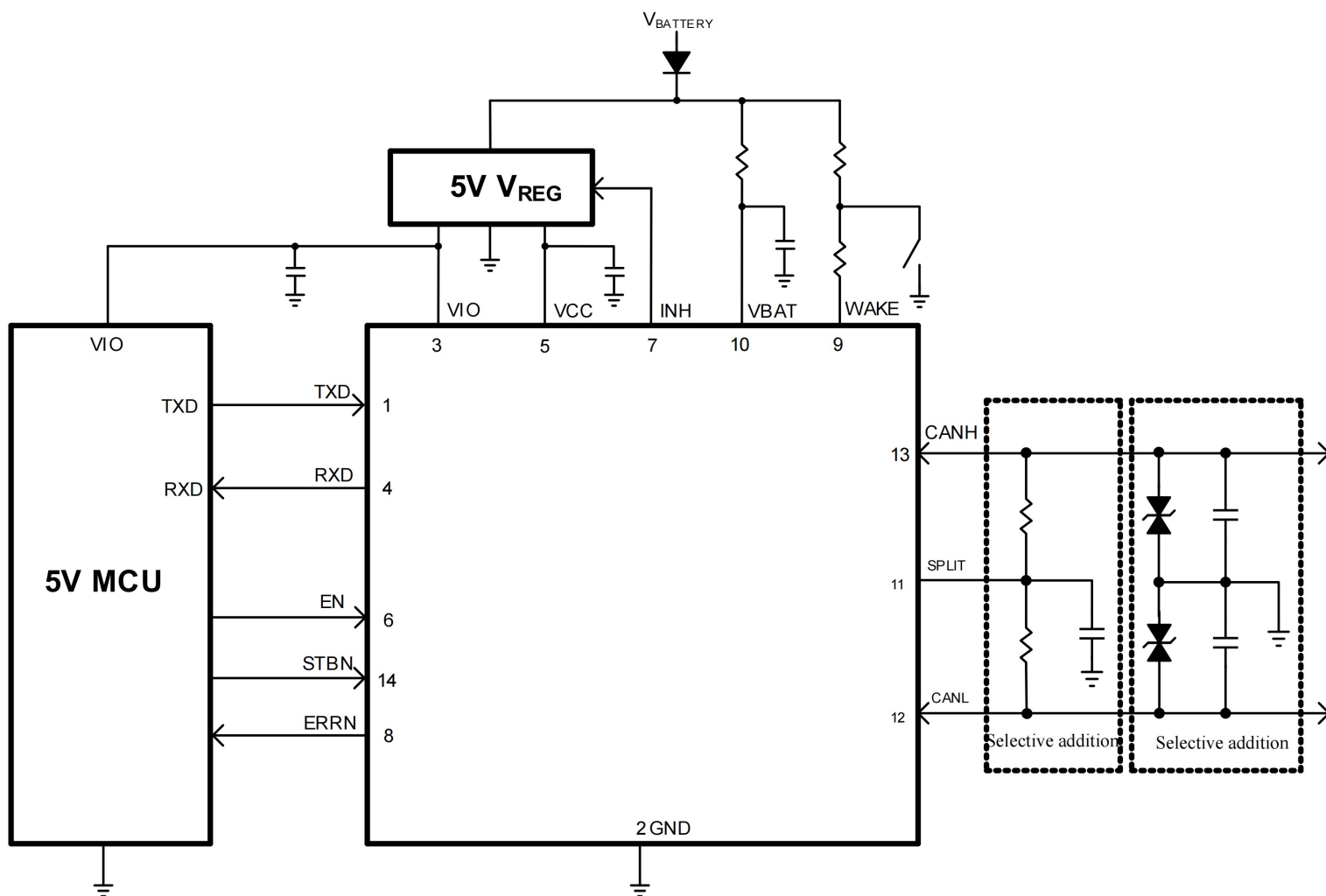


Figure 10 TJA1043 & 5V MCU Typical Application Schematic

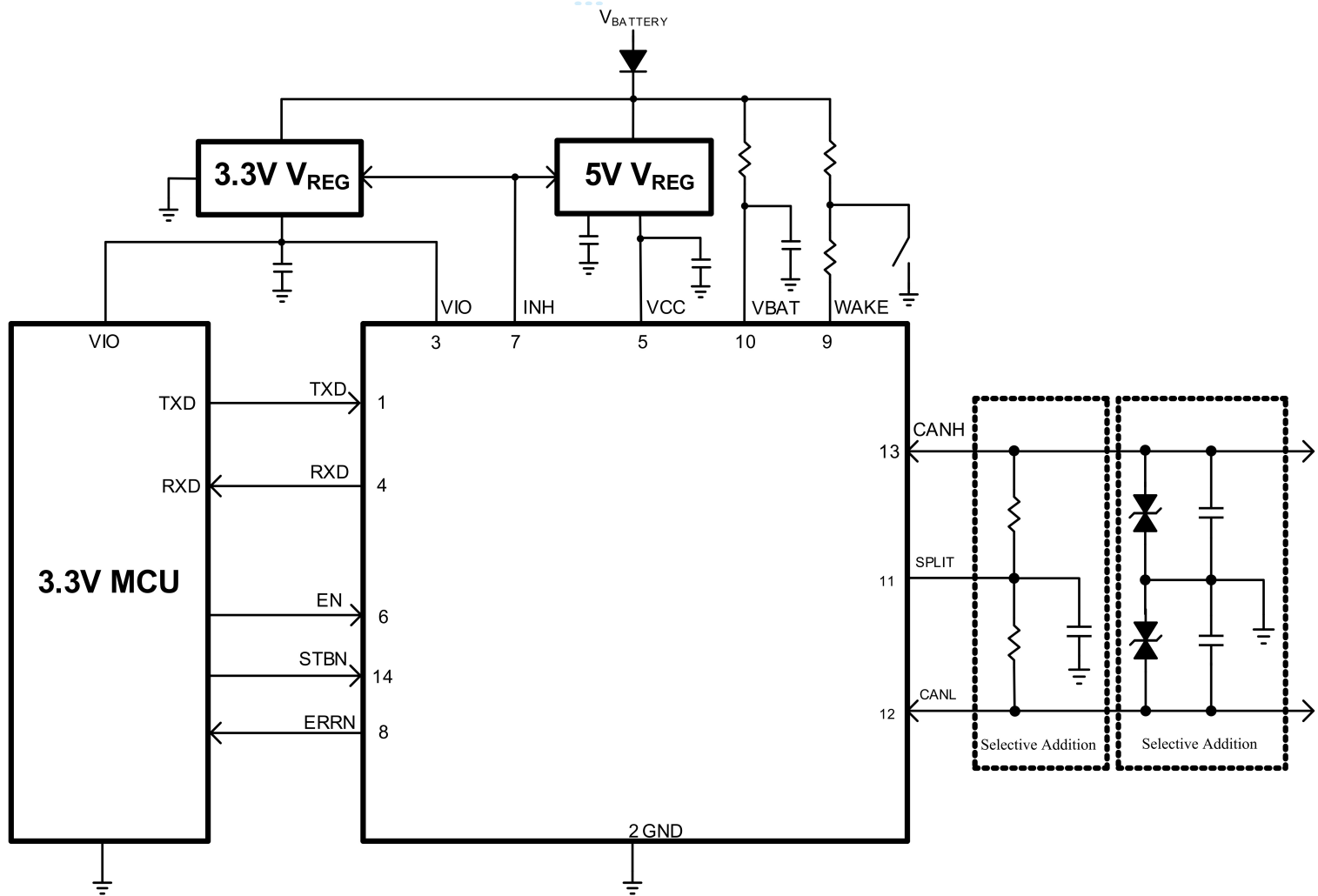
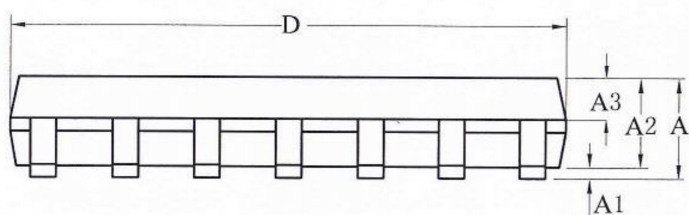
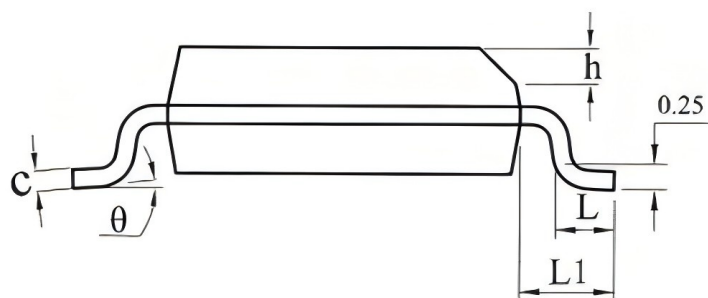
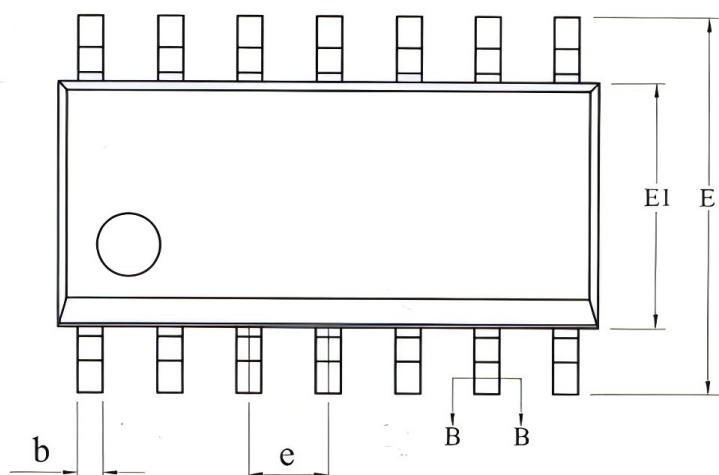


Figure 11 TJA1043 & 3.3V MCU Typical Application Schematic



Packaging Size

SOP14



SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	-	-	1.75
A1	0.05	-	0.225
A2	1.30	1.40	1.50
A3	0.60	0.65	0.70
b	0.39	-	0.47
b1	0.38	0.41	0.44
c	0.20	-	0.24
cl	0.19	0.20	0.21
D	8.55	8.65	8.75
E	5.80	6.00	6.20
E1	3.80	3.90	4.00
e	1.27BSC		
h	0.25	-	0.50
L	0.50	-	0.80
L1	1.05REF		
θ	0	-	8°



ORDERING INFORMATION

Order Number	Package	Package Quantity	Marking On The park	Temperature
TJA1043T,118-TUDI	SOP14	Tape,Reel,4000	TJA1043	-40°C to +125°C



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