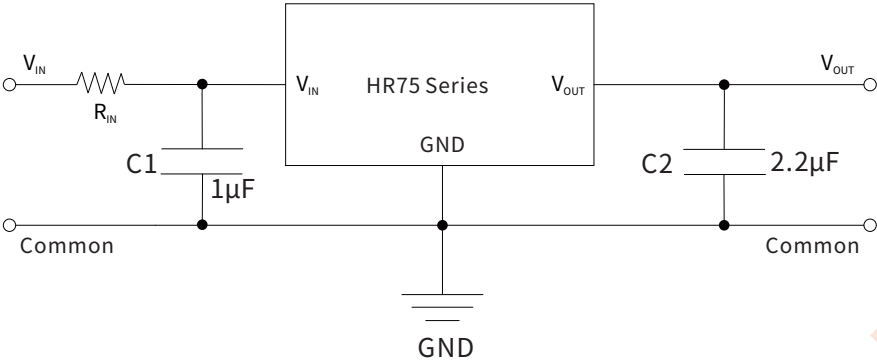


● Typical Application Circuit



● Absolute Maximum Ratings ($T_A = 25^{\circ}\text{C}$ Unless otherwise specified.)

Parameter	Symbol	Value	Unit
Input Voltage	V_{IN}	45	V
Operating Current	I_O	250	mA
Power Dissipation	P_D	SOT89: 500	mW
		SOT-23(-3): 200	
Thermal Resistance Junction-Ambient	$R_{\theta JA}$	SOT89: 200	$^{\circ}\text{C} / \text{W}$
		SOT-23(-3): 500	
Solder Temperature/Time	T_d	260/10	$^{\circ}\text{C} / \text{S}$
Operating Ambient Temperature	T_A	-50 to +125	$^{\circ}\text{C}$
Junction and Storage Temperature	T_J, T_{stg}	-40 to +125	$^{\circ}\text{C}$

Note: Exceed these limits to damage to the device, exposure to Absolute Maximum Rating conditions may affect the reliability of the chip.

● Electrical Characteristics ($T_A = 25^{\circ}\text{C}$ Unless otherwise specified.)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Input Voltage	V_{IN}	$T_A = 25^{\circ}\text{C}$	--	40	--	V
Output Voltage	V_{OUT}	$I_{OUT} = 1\text{mA}, V_{IN} = V_{OUT} + 2.0\text{V}$	$V_{OUT} \times 0.99$	V_{OUT}	$V_{OUT} \times 1.01$	V
Output Current	I_O	$V_{IN} = V_{OUT} + 2.0\text{V}$	--	250	--	mA
Quiescent Current	I_Q	$I_{OUT} = 0\text{mA}$	--	2.5	3.4	μA
Line Regulation	$\Delta V_{OUT} / \Delta V_{IN} \cdot V_{OUT}$	$I_{OUT} = 1\text{mA}$ $V_{OUT} + 1.0\text{V} \leq V_{IN} \leq 40\text{V}$	--	0.01	0.2	%/V
Load Regulation	ΔV_{OUT}	$1\text{mA} \leq I_{OUT} \leq 200\text{mA}$ $V_{IN} = V_{OUT} + 2.0\text{V}$	--	10	72	mV
Output Voltage Temperature Coefficient	$\Delta V_{OUT} / \Delta T_A \cdot V_{OUT}$	$I_{OUT} = 1\text{mA}, V_{IN} = V_{OUT} + 2.0\text{V}$ $T_A = -40$ to 125°C	--	60	--	ppm/ $^{\circ}\text{C}$
Dropout Voltage	V_D	$I_{OUT} = 100\text{mA}, \Delta V_{OUT} = 2\%$	--	550	--	mV

Note: The dropout voltage is defined as $V_{IN} - V_{OUT}$, when V_{OUT} is 98% of the normal value of V_{OUT} .

● Functional Description

Input Capacitor

A 10 μ F ceramic capacitor is recommended to connect between V_{IN} and GND pins to decouple input power supply glitch and noise. The amount of the capacitance may be increased without limit. This input capacitor must be located as close as possible to the device to assure input stability and less noise. For PCB layout, a wide copper trace is required for both V_{IN} and GND.

Output Capacitor

An output capacitor is required for the stability of the LDO. The recommended minimum output capacitance is 2.2 μ F, Tantalum capacitor is recommended, and temperature characteristics are X7R or X5R. Higher capacitance values help to improve load/line transient response. The output capacitance may be increased to keep low undershoot/overshoot.

Place output capacitor as close as possible to V_{OUT} and GND pins.

Thermal Considerations

For continuous operation, do not exceed absolute maximum junction temperature. The maximum power dissipation depends on the thermal resistance of the IC package, PCB layout, rate of surrounding airflow, and difference between junction and ambient temperature. The maximum power dissipation can be calculated by the following formula: $P_{D(MAX)} = (T_{J(MAX)} - T_A) / R_{\theta JA}$.

Where $T_{J(MAX)}$ is the maximum operation junction temperature 125°C, T_A is the ambient temperature and the $R_{\theta JA}$ is the junction to ambient thermal resistance. The power dissipation definition in device is: $P_D = (V_{IN} - V_{OUT}) * I_{OUT} + V_{IN} * I_Q$.

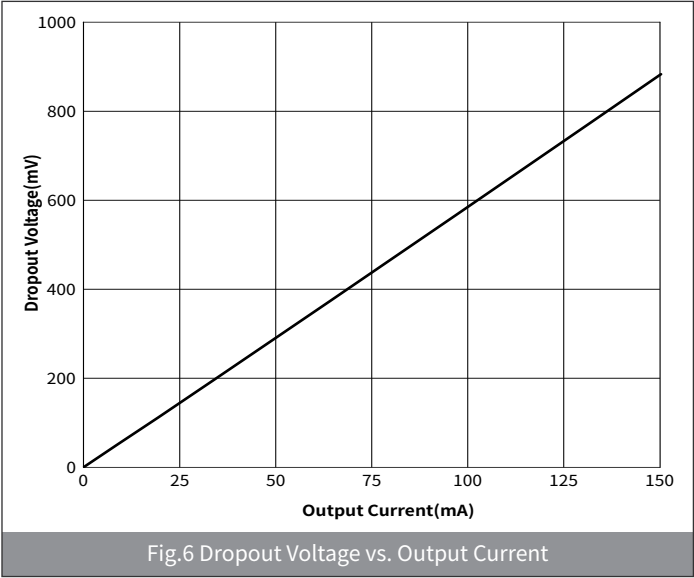
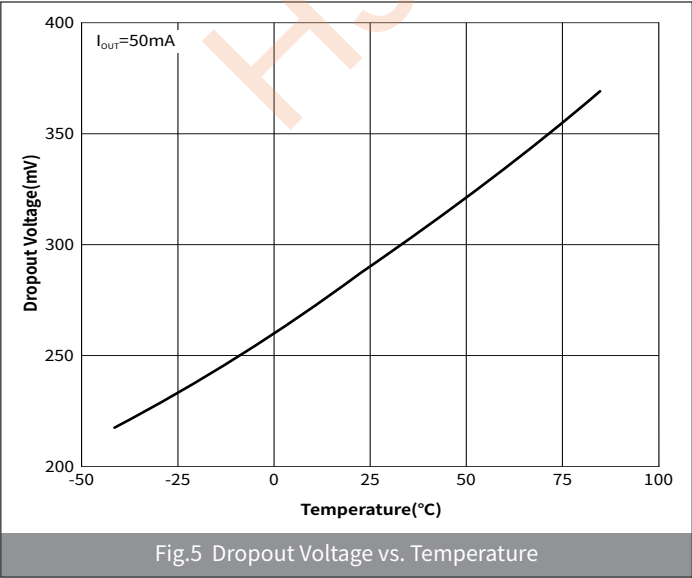
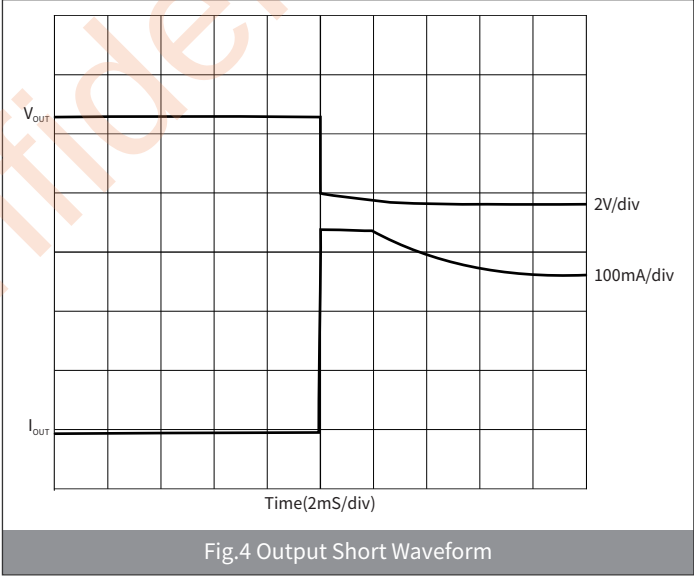
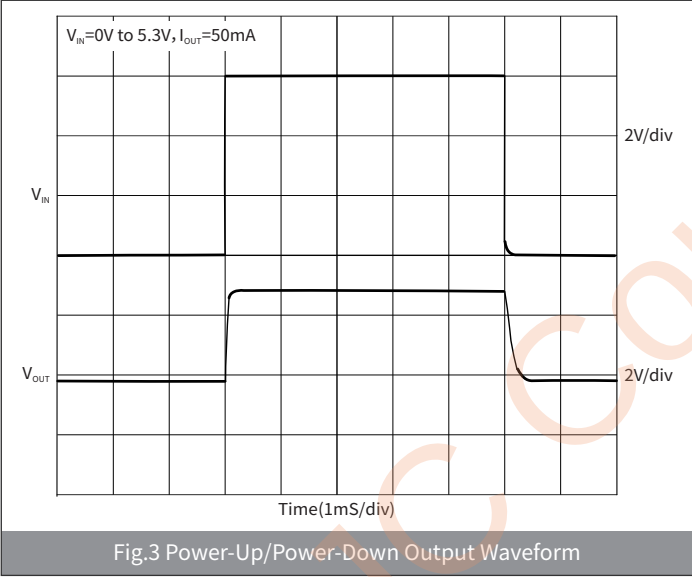
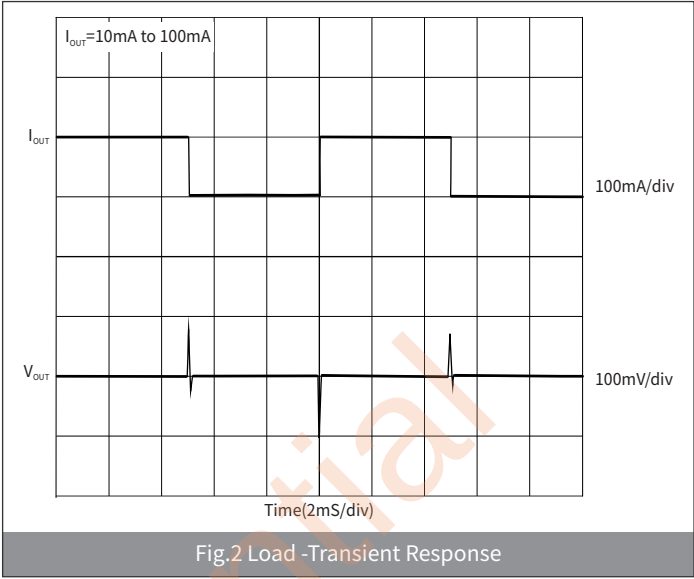
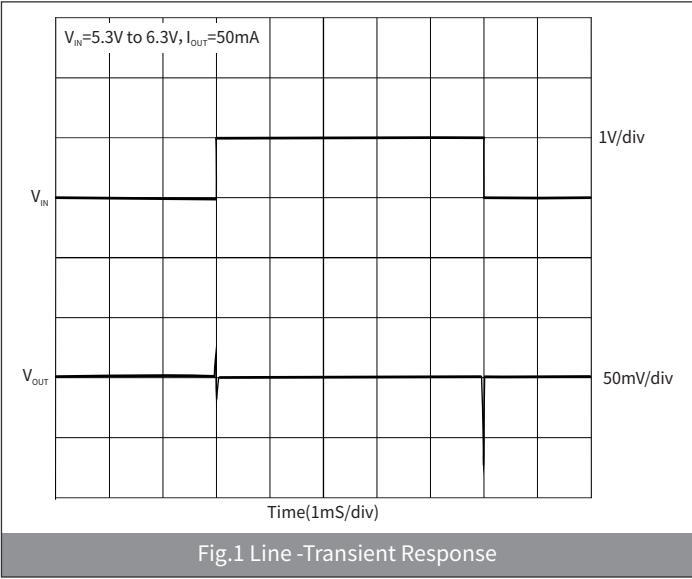
Input Resistance

Place a resistor with an appropriate resistance in series before the V_{IN} of the LDO, which can help the device dissipate some energy during surges. The resistance of the resistor should not be too large. The specific resistance value depends on the application of the circuit. Generally, the resistance of such a resistor should not exceed 20 Ω .

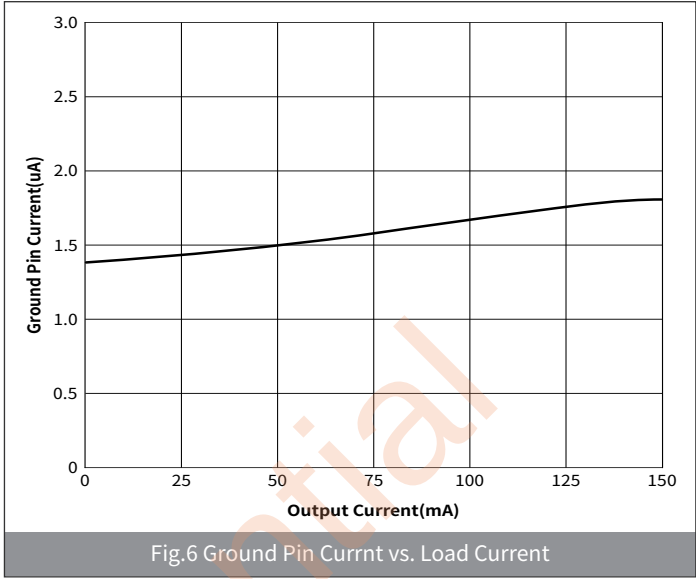
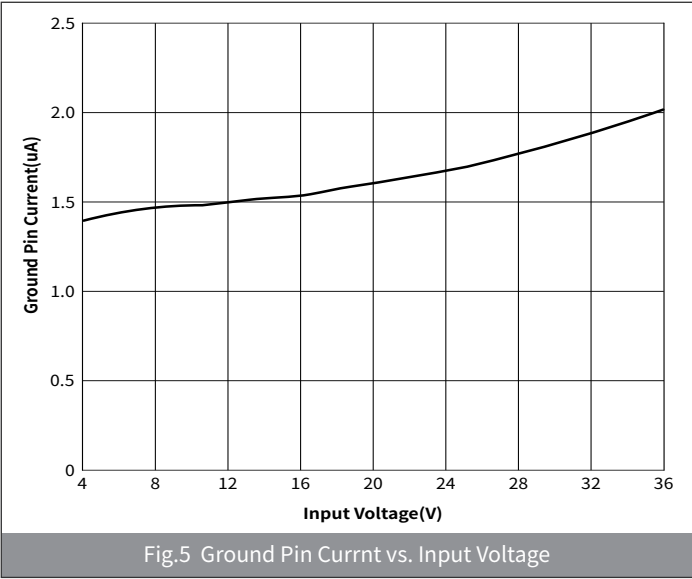
Layout Consideration

By placing input and output capacitors on the same side of the PCB as the LDO, and placing them as close as is practical to the package can achieve the best performance. The ground connections for input and output capacitors must be back to the HR75 Series ground pin using as wide and as short of a copper trace as is practical. Connections using long trace lengths, narrow trace widths, and connections through via must be avoided. These add parasitic inductances and resistance that results in worse performance especially during transient conditions.

● Ratings And Characteristics Curves(HR7530, $T_A = 25^{\circ}\text{C}$ Unless otherwise specified.)



● Ratings And Characteristics Curves(Cont.)



HR75 Series

Low Dropout Linear Regulator

Package Outline Dimensions (SOT-23)

Symbol	Dimensions			
	Millimeters		Inches	
	Min.	Max.	Min.	Max.
A	0.90	1.15	0.035	0.045
A1	-	0.10	-	0.004
A2	0.90	1.05	0.035	0.041
b	0.30	0.50	0.012	0.020
c	0.10	0.20	0.004	0.008
D	2.80	3.00	0.110	0.118
E	1.20	1.40	0.047	0.055
E1	2.25	2.55	0.089	0.100
e	0.950TYP		0.037TYP	
e1	1.80	2.00	0.071	0.079
L	0.550REF		0.022REF	
L1	0.30	0.50	0.012	0.020
θ	-	8°	-	8°

Suggested Pad Layout

Symbol	Dimensions			
	Millimeters		Inches	
	Min.	Max.	Min.	Max.
J	0.80	-	0.031	-
K	-	0.90	-	0.035
M	2.00	-	0.078	-
N	-	1.90	-	0.074

HR75 Series

Low Dropout Linear Regulator

Package Outline Dimensions (SOT-23-3L)

Symbol	Dimensions			
	Millimeters		Inches	
	Min.	Max.	Min.	Max.
A	1.05	1.25	0.041	0.049
A1	-	0.10	-	0.004
A2	1.05	1.15	0.041	0.045
b	0.30	0.50	0.012	0.020
c	0.10	0.20	0.004	0.008
D	2.82	3.02	0.111	0.119
E	1.50	1.70	0.059	0.067
E1	2.65	2.95	0.104	0.116
e	0.90	1.00	0.035	0.039
e1	1.80	2.00	0.071	0.079
L	0.45	0.65	0.018	0.026
L1	0.30	0.60	0.012	0.024
θ	-	8°	-	8°

Suggested Pad Layout

Symbol	Dimensions			
	Millimeters		Inches	
	Min.	Max.	Min.	Max.
J	0.80	-	0.031	-
K	-	0.95	-	0.037
M	2.00	-	0.078	-
N	-	2.0	-	0.079

HR75 Series

Low Dropout Linear Regulator

Package Outline Dimensions (SOT-89)

Symbol	Dimensions			
	Millimeters		Inches	
	Min.	Max.	Min.	Max.
A	4.40	4.60	0.173	0.181
B	1.35	1.83	0.053	0.072
C	3.75	4.25	0.148	0.167
D	2.29	2.60	0.090	0.102
E	2.95	3.05	0.116	0.120
a	0.35	0.48	0.014	0.019
b	0.40	0.56	0.016	0.022
L	0.80	1.20	0.031	0.047
G	0.35	0.44	0.014	0.017
H	1.40	1.60	0.055	0.063

Suggested Pad Layout

Symbol	Dimensions			
	Millimeters		Inches	
	Min.	Max.	Min.	Max.
c	0.80	1.00	0.032	0.04
d	1.30	1.50	0.052	0.060
e	0.70	0.90	0.028	0.036
J	1.80	2.00	0.072	0.080
K	1.40	1.60	0.056	0.064
X	2.50	2.70	0.100	0.108
X1	1.30	1.50	0.052	0.060
Y	4.30	4.50	0.172	0.180
Y1	3.10	3.30	0.124	0.132
θ	-	45°	-	45°