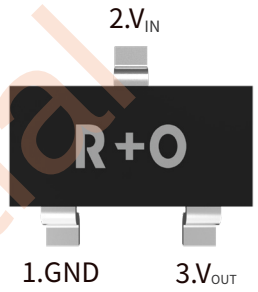
300mA CMOS Voltage Regulators

Features

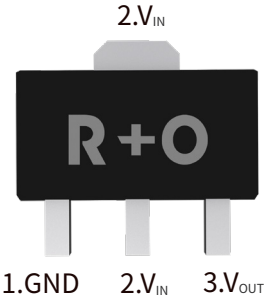
- Quiescent Current: 2.0μA
- Shutdown Current : 0.1μA
- Input Voltage Range: -0.3V to 60V
- Output Current: 300mA
- Low Dropout Voltage: 400mV(Typ.)@100mA
- Output Voltage: 2.0V,2.4V,2.8V,3.0V,3.3V,3.6V,4.0V,4.4V,5.0V
- Output Voltage Accuracy: ±2%（Typ.）

Output Current
300mA
Input Voltage
60V

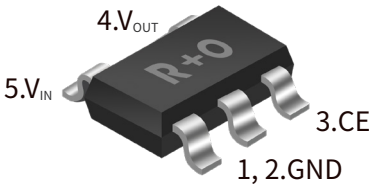
SOT-23



SOT-89



SOT-23-5



Applications

- Battery Power Supply Equipment
- Communication Equipment
- Audio/Video Equipment
- Laptop, Palmtops, Notebook Computers

General Description

The HR75U Series consists of a current limiter circuit, a driver transistor, a precision reference voltage and an error correction circuit. The series is compatible with low ESR ceramic capacitors. The current limiter's foldback circuit operates as a short circuit protection as well as the output current limiter for the output pin.

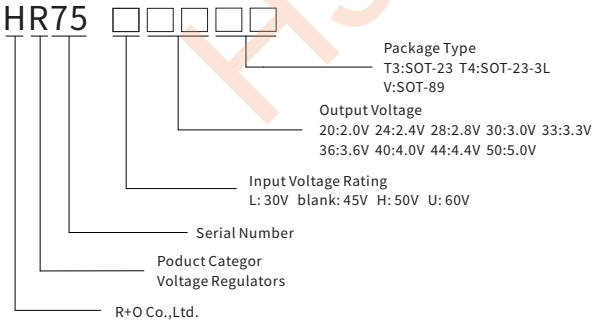
Reference News

SOT-23 Marking:
HR75U28T3: 75U28
HR75U30T3: 75U30
HR75U33T3: 75U33
HR75U36T3: 75U36
HR75U40T3: 75U40
HR75U44T3: 75U44
HR75U50T3: 75U50
HR75U90T3: 75U90

SOT-23-5 Marking:
HR75U28T5: 75U28
HR75U30T5: 75U30
HR75U33T5: 75U33
HR75U36T5: 75U36
HR75U40T5: 75U40
HR75U44T5: 75U44
HR75U50T5: 75U50
HR75U90T5: 75U90

SOT-89 Marking:
HR75U28V: 75U28
HR75U30V: 75U30
HR75U33V: 75U33
HR75U36V: 75U36
HR75U40V: 75U40
HR75U44V: 75U44
HR75U50V: 75U50
HR75U90V: 75U90

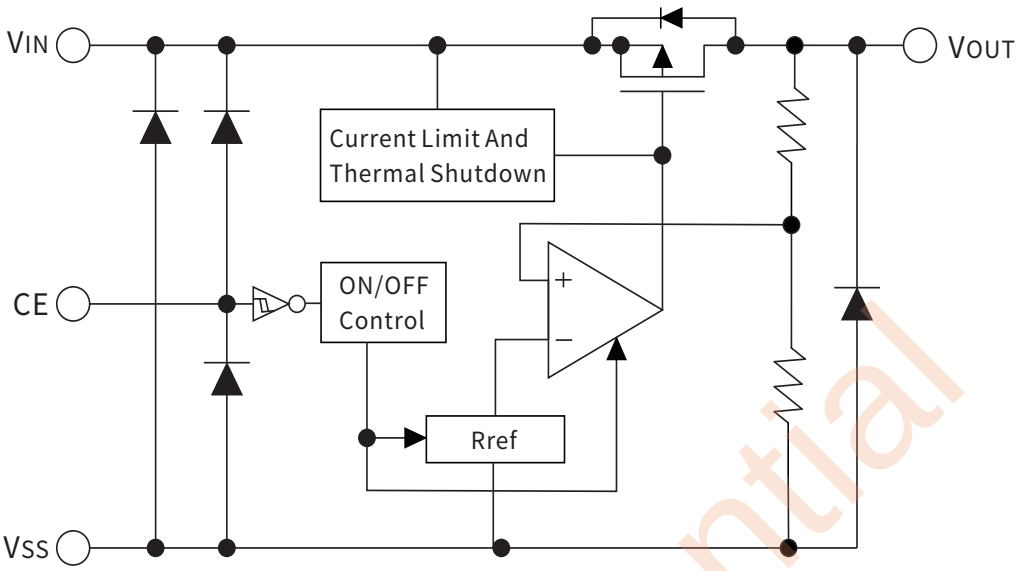
Part Numbering



Ordering Information

Package	Package Code	Unit Weig75H(g)	Reel(pcs)	Box(pcs)	Carton(pcs)	Delivery Mode	MSL
SOT-23	R1	0.008	3000	30000	180000	7''	3
SOT-23-5	R1	0.0146	3000	30000	120000	7''	3
SOT-89	R1	0.045	1000	8000	48000	7''	3

Block Diagram



Pin Description

Pin Number	Pin Name	Description
1	GND	Common ground.
2	GND	Common ground.
3	CE	Enable input. A low voltage (< $V_{CE(LOW)}$) on this input turns the regulator off and discharges the output pin to GND. A high voltage (> $V_{CE(HI)}$) on this pin enables the regulator output.
4	V_{OUT}	Regulated output voltage. A low equivalent series resistance (ESR) capacitor is required from OUT to ground for stability. Place the output capacitor as close to the OUT and GND pins of the device as possible.
5	V_{IN}	Input voltage supply. For best transient response and to minimize input impedance, use a 10μF value capacitor or larger capacitor from IN to ground. Place the input capacitor as close to the IN and GND pins of the device as possible.

Absolute Maximum Ratings (T_A = 25°C Unless otherwise specified)

Parameter	Symbol	Value	Unit
Input Voltage	V_{IN}	60	V
Enable input Voltage	V_{CE}	60	V
Operating Current	I_O	300	mA
Power Dissipation	P_D	SOT89: 500	mW
		SOT-23/SOT-23-5: 200	
Solder Temperature/Time	T_d	260/10	°C /S
Operating Ambient Temperature	T_A	-40 to +125	°C
Junction and Storage Temperature	T_J,T_{stg}	150, -50 to +125	°C

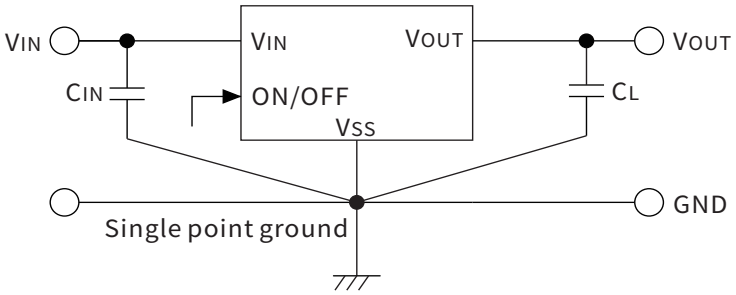
Note: Exceed these limits to damage to the device, exposure to Absolute Maximum Rating conditions may affect the reliability of the chip.

Electrical Characteristics(T_A = 25°C Unless otherwise specified)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Input Voltage	V_{IN}	T_A = 25°C	--	--	60	V
Output Voltage	V_{OUT}	I_{OUT} = 1mA, V_{IN} = V_{OUT} + 2.0V	V_{OUT} × 0.98	V_{OUT}	V_{OUT} × 1.02	V
Output Current	I_O	V_{IN} = V_{OUT} + 2.0V	--	300	--	mA
Quiescent Current	I_Q	V_{CE} = V_{IN}	--	2.0	5.0	μA
Shutdown Ground Current	I_{SHDN}	V_{CE} = 0 V	--	0.1	2.5	μA
High Input Threshold	V_{CEH}	V_{IN} = V_{OUT} + 2.0V	2.0	--	60	V
Low Input Threshold	V_{CEL}	V_{IN} = V_{OUT} + 2.0V	0	--	0.6	V
Short-Circuit Current Limit	I_{SHORT}	V_{OUT} = 0 V	--	25	--	mA
Power-Supply Rejection Ratio	PSRR	I_{OUT} = 50mA, 100Hz	--	80	--	dB
		I_{OUT} = 50mA, 1KHz	--	70	--	
		I_{OUT} = 50mA, 10KHz	--	60	--	
		I_{OUT} = 50mA, 100KHz	--	50	--	
Line Regulation	$\triangle V_{OUT}/\triangle V_{IN}.V_{OUT}$	I_{OUT} = 1mA V_{OUT} + 1.0V ⩽ V_{IN} ⩽ 60V	--	0.01	0.2	%/V
Load Regulation	$\triangle V_{OUT}$	1mA ⩽ I_{OUT} ⩽ 200mA V_{IN} = V_{OUT} + 2.0V	--	10	72	mV
Output Voltage Temperature Coefficient	$\triangle V_{OUT}/\triangle T_A.V_{OUT}$	I_{OUT} = 1mA, V_{IN} = V_{OUT} + 2.0V T_A = -40 to 125°C	--	50	--	ppm/°C
Dropout Voltage	V_D	I_{OUT} = 100mA, $\triangle V_{OUT}$ = 2%	--	400	1000	mV
Thermal Shutdown	T_{SD}	T_J Rising: I_{OUT} = 1mA	160			°C
		T_J Falling: I_{OUT} = 1mA	140			°C

Note: The dropout voltage is defined as V_{IN} − V_{OUT}, when V_{OUT} is 98% of the normal value of V_{OUT}.

Typical Application Circuit



1.CIN used to stabilize input capacitance
2.CL ceramic capacitors greater than or equal to 1μF can be used

Functional Description

Input Capacitor

A 10μF ceramic capacitor is recommended to connect between V_{IN} and GND pins to decouple input power supply glitch and noise. The amount of the capacitance may be increased without limit. This input capacitor must be located as close as possible to the device to assure input stability and less noise. For PCB layout, a wide copper trace is required for both V_{IN} and GND.

Output Capacitor

An output capacitor is required for the stability of the LDO. The recommended minimum output capacitance is 1μF, Tantalum capacitor is recommended, and temperature characteristics are X7R or X5R. Higher capacitance values help to improve load/line transient response. The output capacitance may be increased to keep low undershoot/overshoot.
Place output capacitor as close as possible to V_{OUT} and GND pins.

Thermal Considerations

For continuous operation, do not exceed absolute maximum junction temperature. The maximum power dissipation depends on the thermal resistance of the IC package, PCB layout, rate of surrounding airflow, and difference between junction and ambient temperature. The maximum power dissipation can be calculated by the following formula : $P_{D(MAX)} = (T_{J(MAX)} - T_A) / R_{\theta JA.}$
Where $T_{J(MAX)}$ is the maximum operation junction temperature 125°C , T_A is the ambient temperature and the $R_{\theta JA}$ is the junction to ambient thermal resistance.The power dissipation definition in device is: $P_D = (V_{IN} - V_{OUT}) * I_{OUT} + V_{IN} * I_Q$.

Layout Consideration

By placing input and output capacitors on the same side of the PCB as the LDO, and placing them as close as is practical to the package can achieve the best performance. The ground connections for input and output capacitors must be back to the HR75U Series ground pin using as wide and as short of a copper trace as is practical.Connections using long trace lengths, narrow trace widths, and connections through via must be avoided. These add parasitic inductances and resistance that results in worse performance especially during transient conditions.

Ratings And Characteristics Curves(HR75U33, T_A = 25°C Unless otherwise specified)

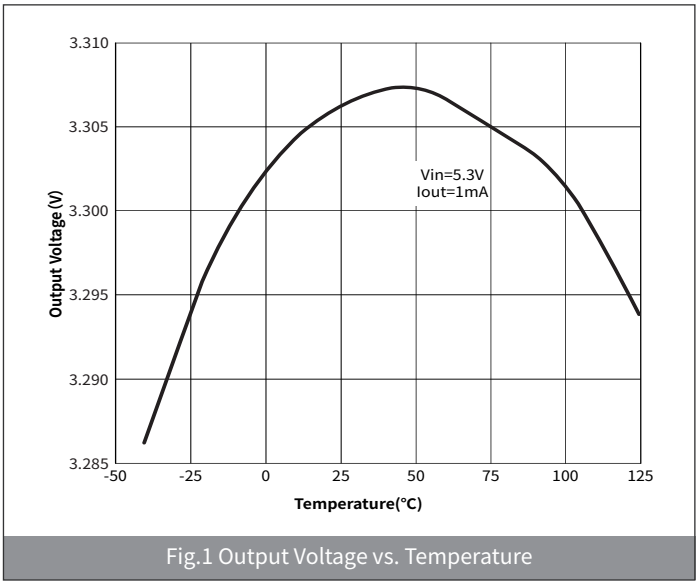


Fig.1 Output Voltage vs. Temperature

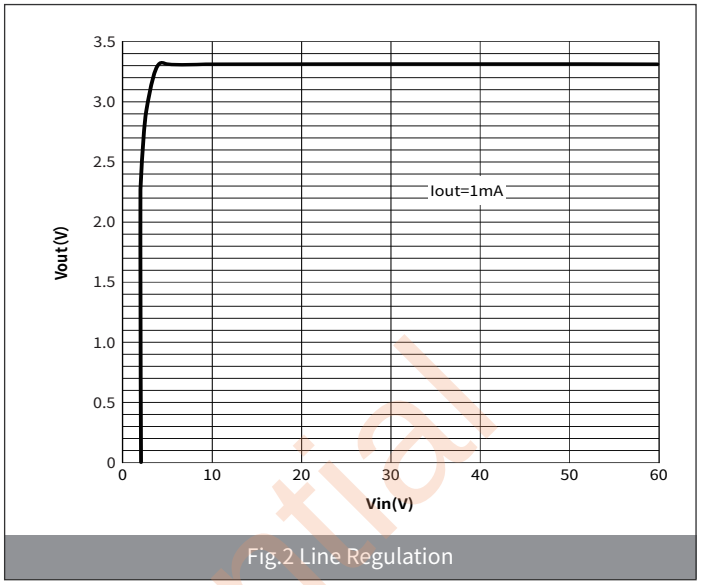


Fig.2 Line Regulation

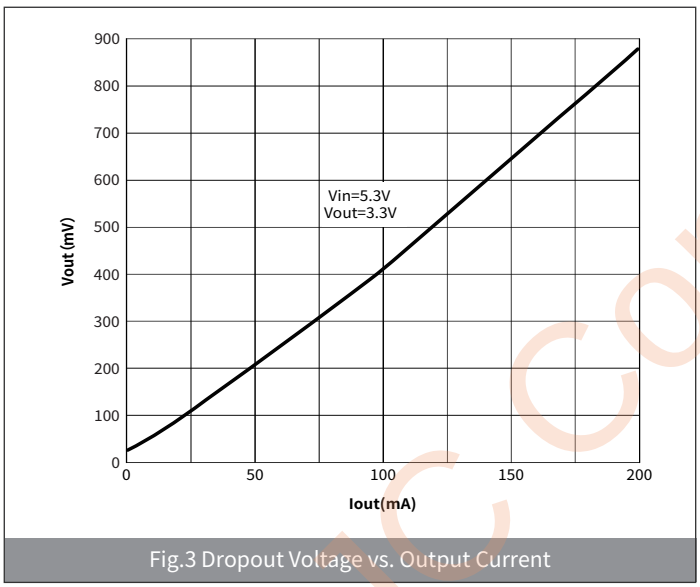


Fig.3 Dropout Voltage vs. Output Current

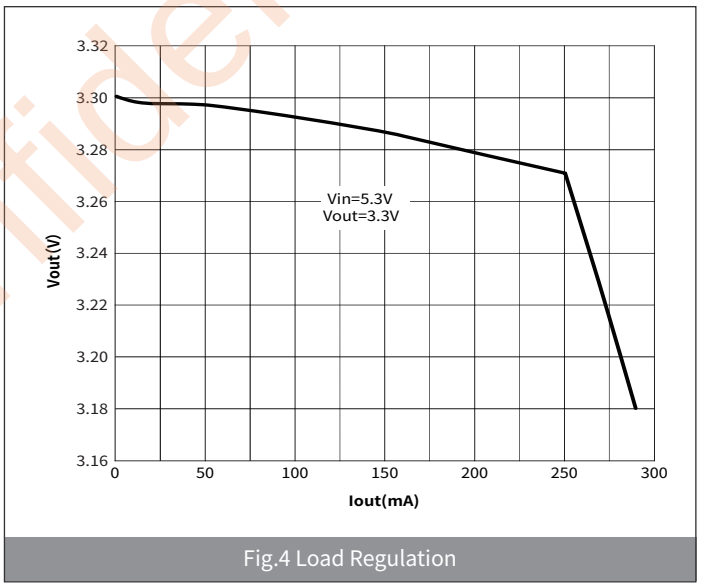


Fig.4 Load Regulation

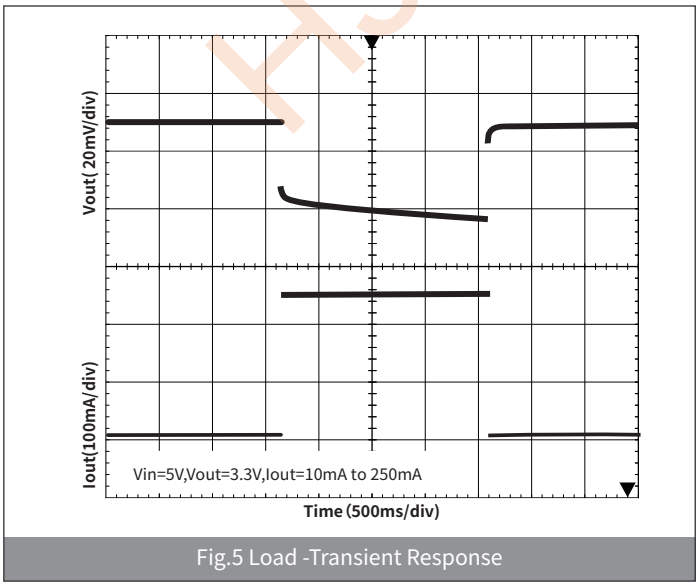


Fig.5 Load -Transient Response

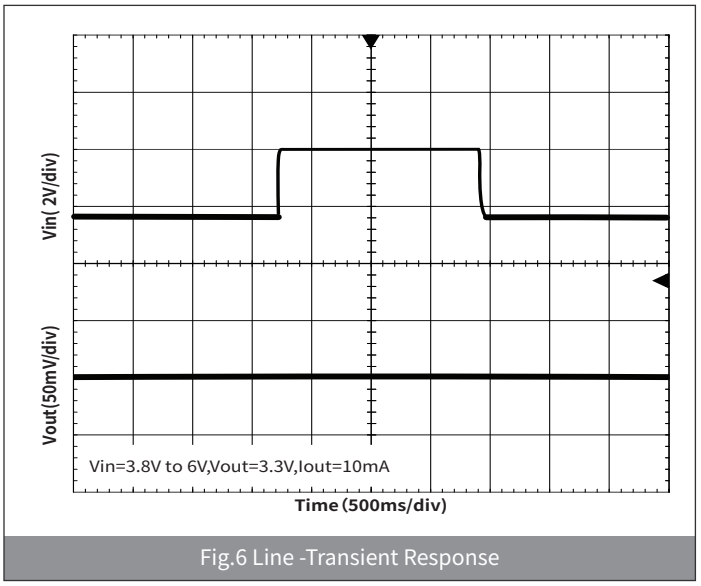


Fig.6 Line -Transient Response

Ratings And Characteristics Curves(Cont.)

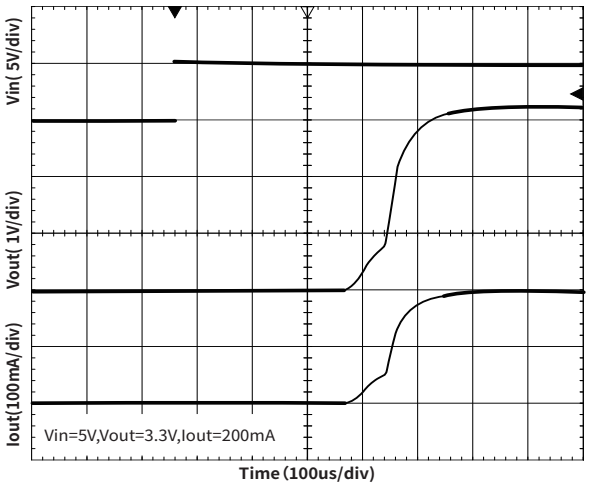
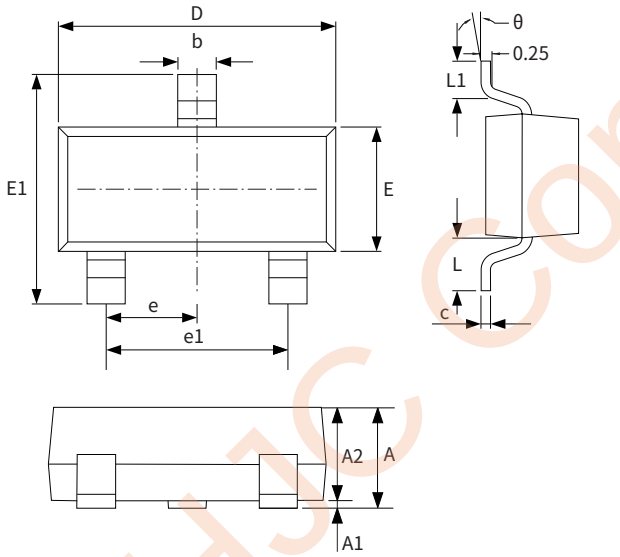


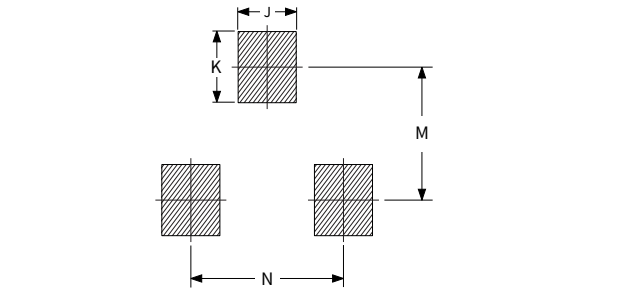
Fig.7 Power Up Response

Package Outline Dimensions (SOT-23)



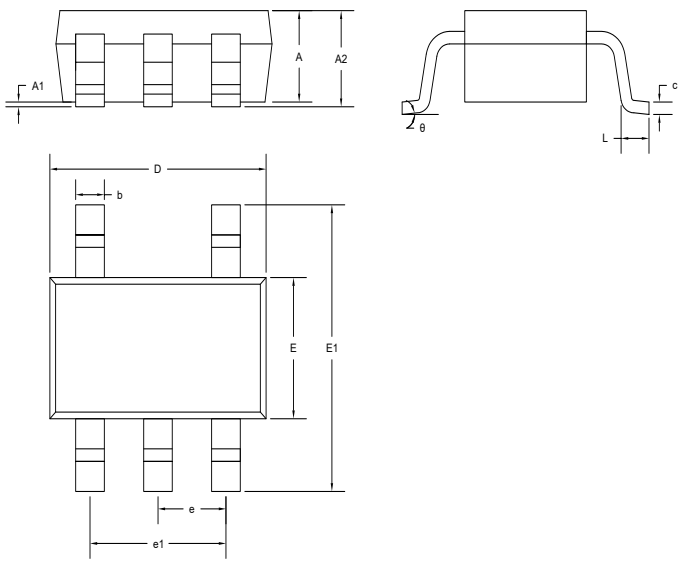
Symbol	Dimensions			
	Millimeters		Inches	
	Min.	Max.	Min.	Max.
A	0.90	1.15	0.035	0.045
A1	-	0.10	-	0.004
A2	0.90	1.05	0.035	0.041
b	0.30	0.50	0.012	0.020
c	0.10	0.20	0.004	0.008
D	2.80	3.00	0.110	0.118
E	1.20	1.40	0.047	0.055
E1	2.25	2.55	0.089	0.100
e	0.950TYP		0.037TYP	
e1	1.80	2.00	0.071	0.079
L	0.550REF		0.022REF	
L1	0.30	0.50	0.012	0.020
θ	-	8°	-	8°

Suggested Pad Layout



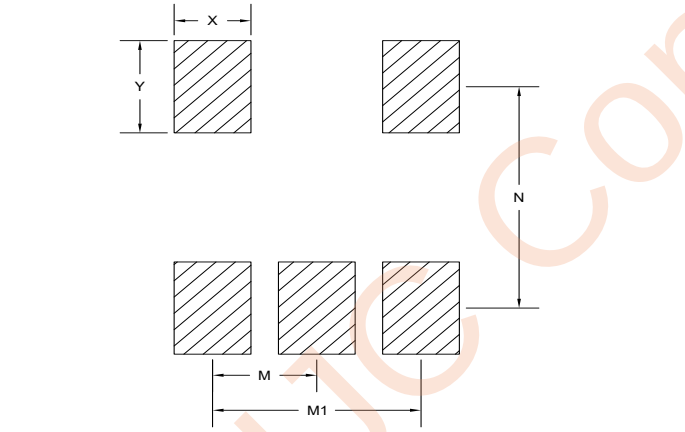
Symbol	Dimensions			
	Millimeters		Inches	
	Min.	Max.	Min.	Max.
J	0.80	-	0.031	-
K	-	0.90	-	0.035
M	2.00	-	0.078	-
N	-	1.90	-	0.074

Package Outline Dimensions (SOT-23-5)



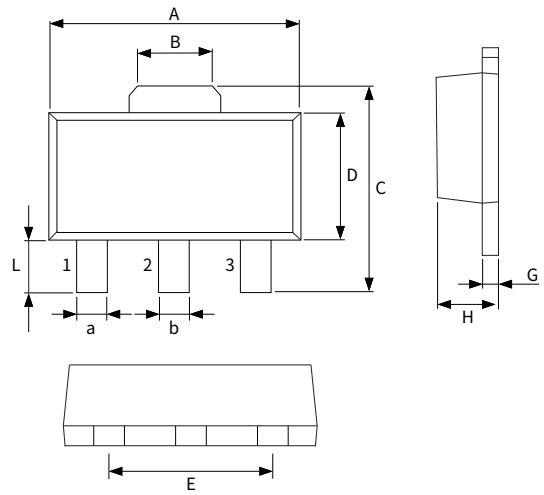
Symbol	Dimensions			
	Millimeters		Inches	
	Min.	Max.	Min.	Max.
A	1.05	1.25	0.041	0.049
A1	0	0.13	0.000	0.005
A2	1.05	1.15	0.041	0.045
b	0.3	0.5	0.012	0.020
c	0.10	0.2	0.004	0.008
D	2.82	3.02	0.111	0.119
E	1.50	1.70	0.059	0.067
E1	2.65	2.95	0.104	0.116
e	0.95 BSC		0.037BSC	
e1	1.90 BSC		0.075 BSC	
L	0.3	0.60	0.012	0.024
θ	0	8°	0	8°

Suggested Pad Layout



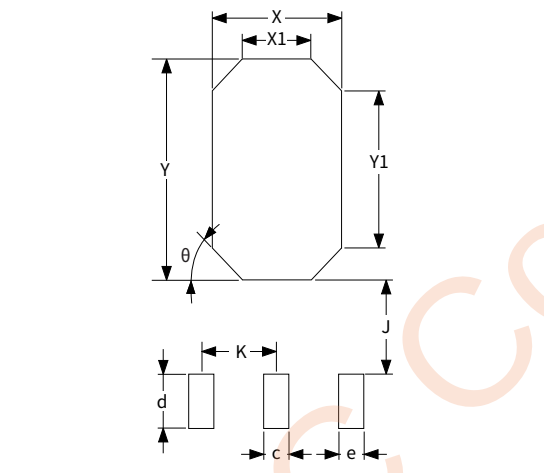
Symbol	Dimensions			
	Millimeters		Inches	
	Min.	Max.	Min.	Max.
X	0.85	0.85	0.033	0.033
Y	0.90	1.10	0.035	0.043
M	0.85	1.05	0.033	0.041
M1	1.80	2.0	0.071	0.079
N	2.3	2.5	0.091	0.098

Package Outline Dimensions (SOT-89)



Symbol	Dimensions			
	Millimeters		Inches	
	Min.	Max.	Min.	Max.
A	4.40	4.60	0.173	0.181
B	1.35	1.83	0.053	0.072
C	3.75	4.25	0.148	0.167
D	2.29	2.60	0.090	0.102
E	2.95	3.05	0.116	0.120
a	0.35	0.48	0.014	0.019
b	0.40	0.56	0.016	0.022
L	0.80	1.20	0.031	0.047
G	0.35	0.44	0.014	0.017
H	1.40	1.60	0.055	0.063

Suggested Pad Layout



Symbol	Dimensions			
	Millimeters		Inches	
	Min.	Max.	Min.	Max.
c	0.80	1.00	0.032	0.04
d	1.30	1.50	0.052	0.060
e	0.70	0.90	0.028	0.036
J	1.80	2.00	0.072	0.080
K	1.40	1.60	0.056	0.064
X	2.50	2.70	0.100	0.108
X1	1.30	1.50	0.052	0.060
Y	4.30	4.50	0.172	0.180
Y1	3.10	3.30	0.124	0.132
θ	-	45°	-	45°