Features

- Split Gate Trench MOSFET technology
- Excellent package for heat dissipation
- High density cell design for low $RDS_{(ON)}$

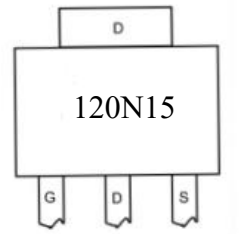
Bvdss	Rdson	ID
150V	11mΩ	120A

Application

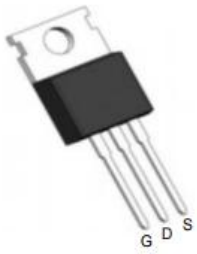
RoHS

- DC-DC Converters
- Power management function
- Synchronous-rectification applications

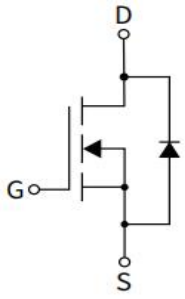
Package



Marking and pin assignment



TO220 top view



Schematic diagram

Package Marking and Ordering Information

Device Marking	Device	Device Package	Quantity
120N15	S120N15T	TO220	50

Absolute Maximum Ratings (T_C=25℃unless otherwise specified)

Parameter		Symbol	Value	Unit
Drain-Source Voltage		V_{DS}	150	V
Gate-Source Voltage		V_{GS}	±20	V
Continuous Drain Current,V_{GS}@10V[1]	T_C=25℃	I_D	120	A
	T_C=100℃		54	A
Pulsed Drain Current[2]		I_{DM}	205	A
Single Pulsed Avalanche Energy[3]		EAS	436	mJ
Avalanche Current		I_{AS}	-	A
Power Dissipation[4]		P_D	56	W
Operating Junction Temperature Range		T_J	-55 ~ 150	℃
Storage Temperature Range		T_{STG}	-55 ~ 150	℃

Thermal Resistance Ratings

Parameter	Symbol	Value	Unit
Thermal Resistance, Junction-to-Ambient[1]	$R_{\theta JA}$	51	℃/W
Thermal Resistance, Junction-to-Case[1]	$R_{\theta JC}$	1.2	℃/W

Ordering Information

Ordering Number	Package	Pin Assignment			Packing
Halogen Free		G	D	S	
HLS70N10T	TO220	1	2	3	Tube

Electrical Characteristics (T_J=25℃unless otherwise noted)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Units
Drain to Source Breakdown Voltage	V_{DSS}	I_D = 250μA,V_{GS}=0V	150	-	-	V
Drain-Source Leakage Current	I_{DSS}	V_{DS}=150V,V_{GS}=0V,T_J=25℃	-	-	1	μA
		V_{DS}=150V,V_{GS}=0V,T_J=100℃	-	-	100	μA
Gate to Source Leakage Current	I_{GSS}	V_{GS}=±20V,V_{DS}=0V	-	-	±100	nA
Gate Threshold Voltage	$V_{GS(th)}$	V_{GS}=V_{DS},I_D=250uA	2.5	3.4	4.5	V
Static Drain-Source On-Resistance[2]	$R_{DS(on)}$	V_{GS}=10V,I_D=1A	-	11	12.5	mΩ
Gate Resistance	R_g	V_{DS}=0V,V_{GS}=0V,f=1MHz	-	1.6	-	Ω
Input Capacitance	C_{iss}	V_{GS}=0V,V_{DS}=75V, f=1MHz	-	2049	-	pF
Output Capacitance	C_{oss}		-	247	-	
Reverse Transfer Capacitance	C_{rss}		-	12	-	
Total Gate Charge	Q_g	V_{GS}=10V,V_{DS}=75V, I_D=20A	-	28	-	nC
Gate Source Charge	Q_{gs}		-	9.4	-	
Gate Drain Charge	Q_{gd}		-	6.3	-	
Turn-ON Delay Time	$t_{d(on)}$	V_{GS}=10V,V_{DD}=75V, I_D=20A,R_G=3Ω	-	4	-	ns
Rise Time	t_r		-	17	-	
Turn-OFF Delay Time	$t_{d(off)}$		-	18	-	
Fall Time	t_f		-	7.4	-	
Diode Forward Current[1,4]	I_S	V_G=V_D=0V,Force Current	-	-	120	A
Diode Forward Voltage[2]	V_{SD}	I_S=20A,V_{GS}=0V	-	-	1.2	V
Reverse Recovery time	t_{rr}	IF=20A ,di/dt=100A/μs	-	102	-	ns
Reverse Recovery Charge	Q_{rr}		-	207	-	nC

Notes:

1. Repetitive rating, pulse width limited by junction temperature $T_{J(MAX)}$=150°C
2. The EAS data shows Max. rating . The test condition is VDD=75V, VGS=10V, L=1mH,
3. The data tested by surface mounted on a 1 inch2 FR-4 board with 2OZ copper, The value in any given application depends on the user's specific board design.
4. The data tested by pulsed , pulse width ≤ 300us , duty cycle ≤ 2%.
5. This value is guaranteed by design hence it is not included in the production test.

Typical Performance Characteristics

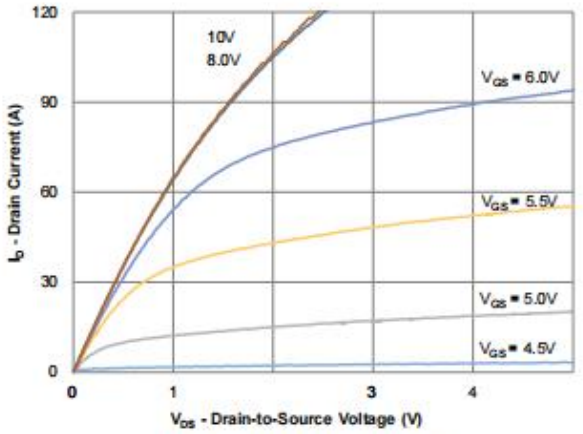


Figure 1: Output Characteristics

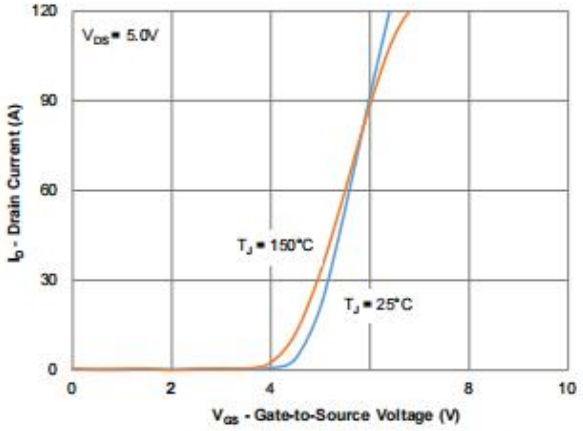


Figure 2: Transfer Characteristics

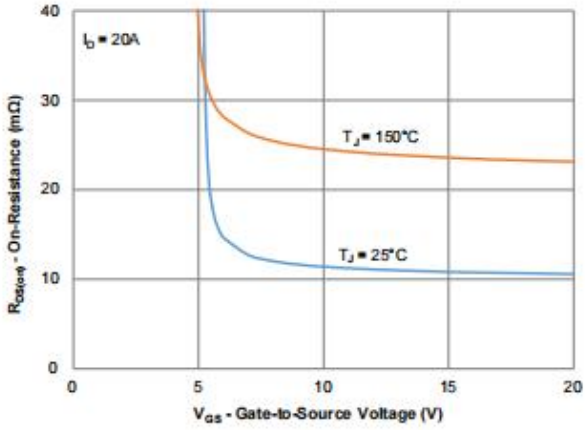


Figure 3: On-Resistance vs. Gate-Source Voltage

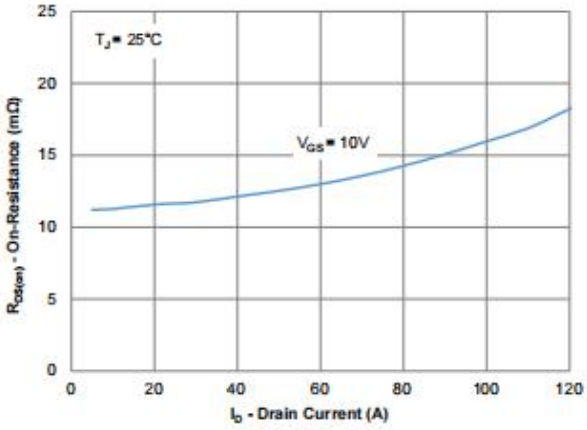


Figure 4: On-Resistance vs. Drain Current and Gate Voltage

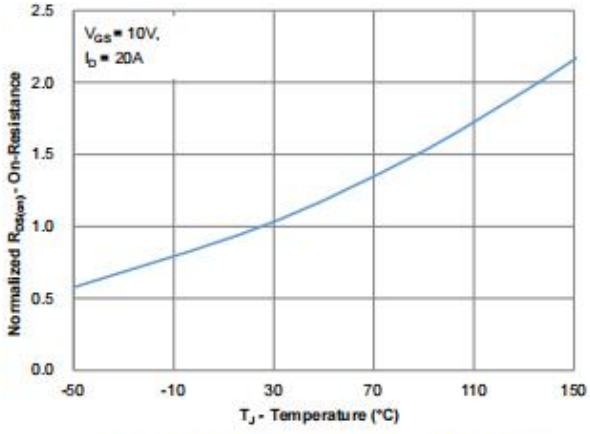


Figure 5: On-Resistance vs. Junction Temperature

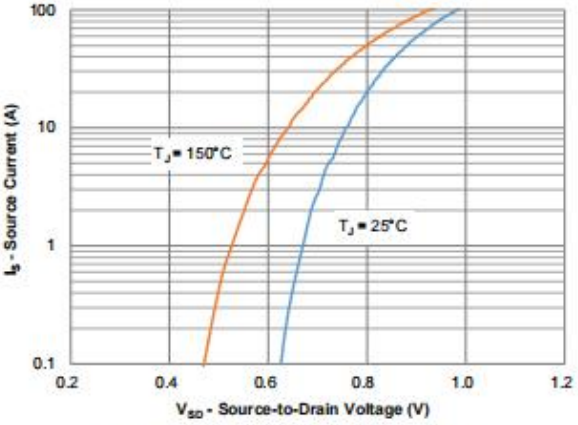


Figure 6: Source-Drain Diode Forward Voltage

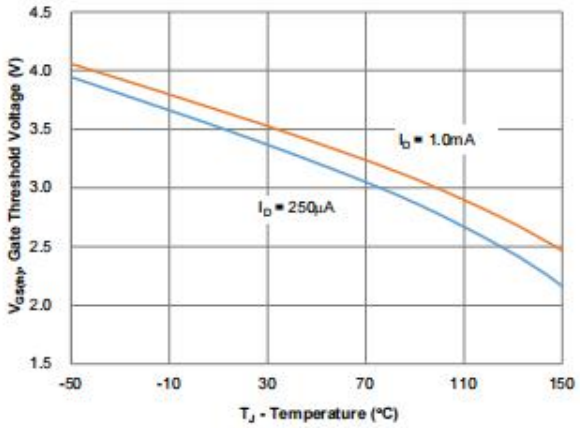


Figure 7: Gate Threshold Variation vs. Junction Temperature

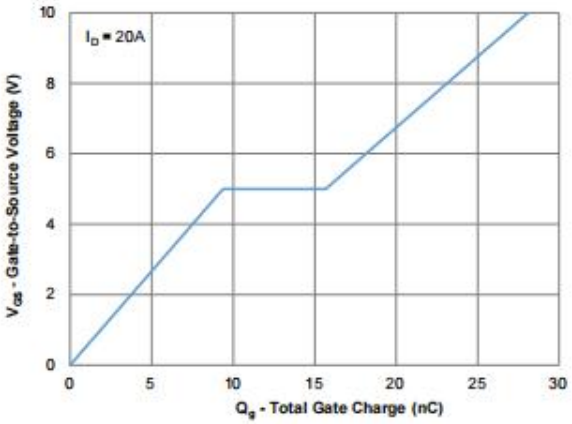


Figure 8: Gate Charge Characteristics

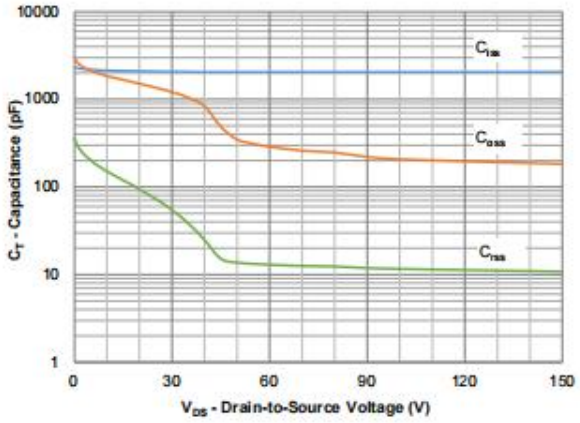


Figure 9: Capacitance Characteristics

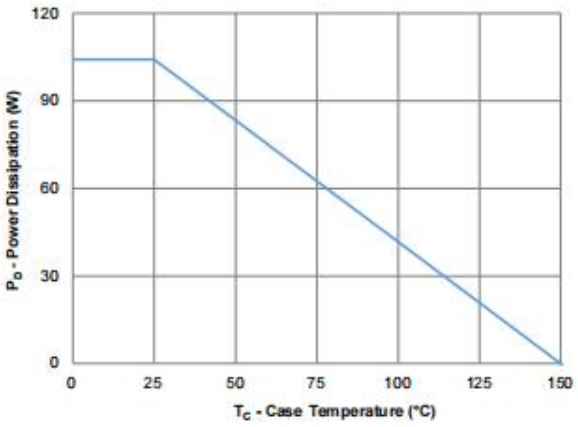


Figure 10: Power Derating

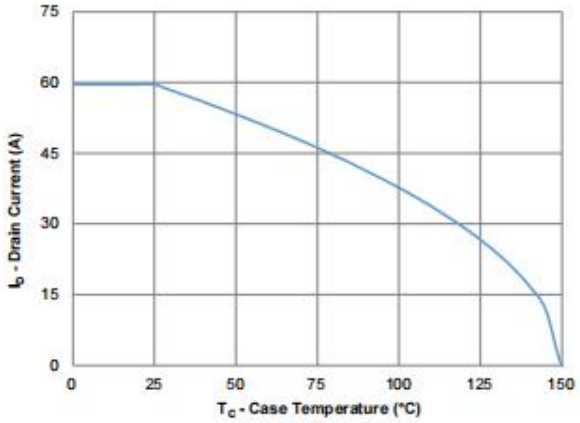


Figure 11: Current Derating

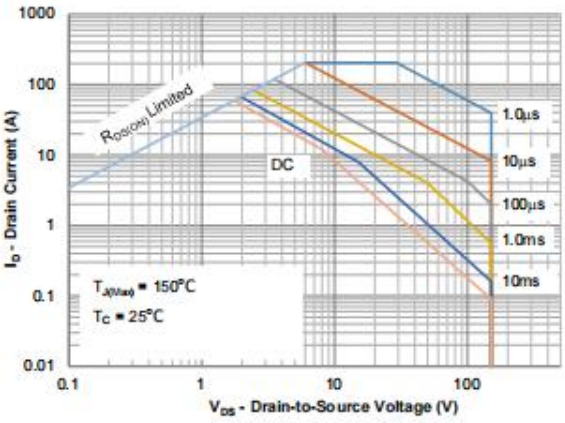


Figure 12: Safe Operating Area

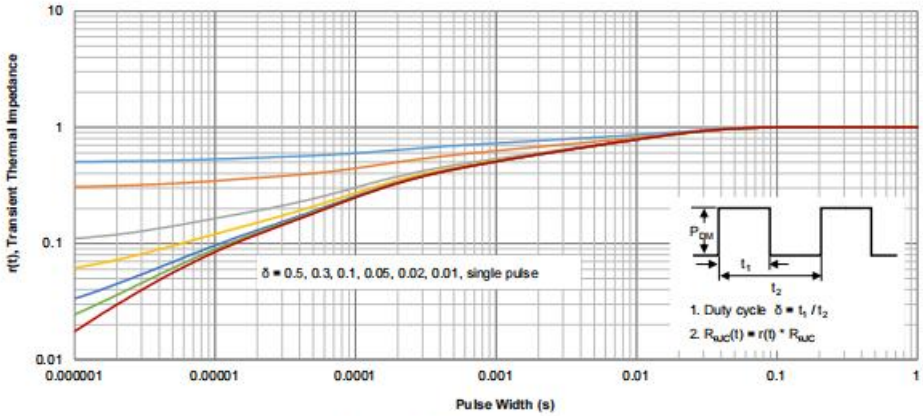
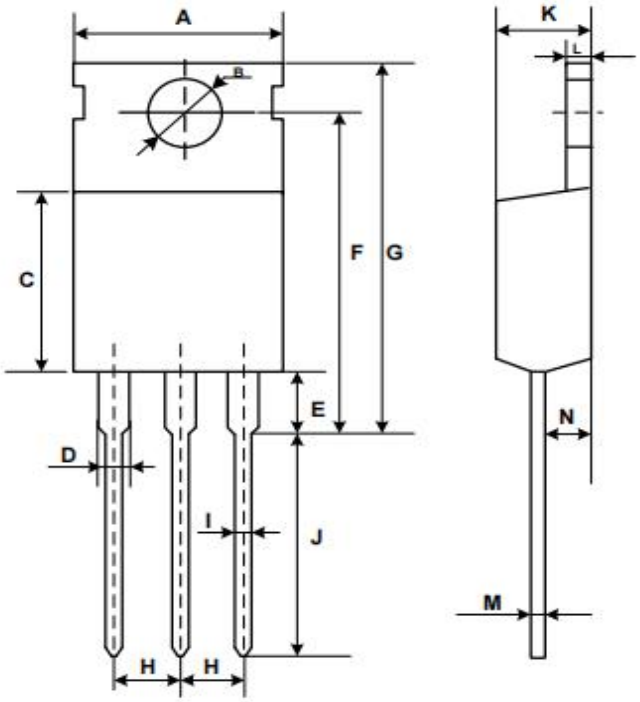


Figure 13: Normalized Maximum Transient Thermal Impedance

Package Dimensions TO220



SYMBOL	MM	
	MIN	MAX
A	9.70	10.30
B	3.40	3.80
C	8.80	9.40
D	1.17	1.47
E	2.60	3.50
F	15.10	16.70
G	19.55MAX	
H	2.54REF	
I	0.70	0.95
J	9.35	11.00
K	4.30	4.77
L	1.20	1.45
M	0.40	0.65
N	2.20	2.60

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Chip revision change

Date	Revision	Remarks