JWH5084

17V/12A

Sync. Step-Down Converter

Preliminary Specifications Subject to Change without Notice

DESCRIPTION

The JW®H5084 is a monolithic buck switching regulator based on I2 architecture for fast transient response. Operating with an input range of 4.5V~17V, JWH5084 delivers 12A of continuous output current with two integrated N-Channel MOSFETs. The internal synchronous power switches provide high efficiency without the use of an external Schottky diode. The operation frequency is set easily to 400 kHz, 800 kHz, or 1200 kHz with the MODE configuration, allowing the JWH5084 frequency to remain constant regardless of the input/output voltages.

JWH5084 guarantees robustness with output short protection, over-voltage protection, thermal protection and under voltage protection.

JWH5084 is available in QFN3.5 × 3.5-18 package, which provides a compact solution with minimal external components.

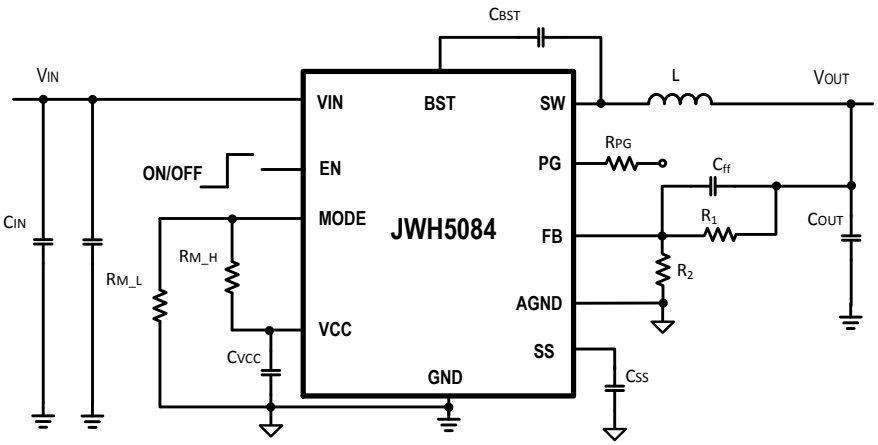
FEATURES

- 4.5V to 17V operating input range
- 12A output current
- Selectable accurate current limit level
- ±1% reference voltage over -40℃ to +125℃ junction temperature range
- FCCM operation mode
- Power good indicator
- Programmable soft-start time
- Selectable switching frequency from 400kHz, 800kHz, and 1200kHz
- Output discharge function
- Non-latch OCP, UVP, OVP, UVLO
- Thermal protection
- Available in QFN3.5X3.5-18 package

APPLICATIONS

- Telecom and Networking Systems
- Server, Cloud-Computing, Storage
- Base Stations
- General Purpose Point-of-Load

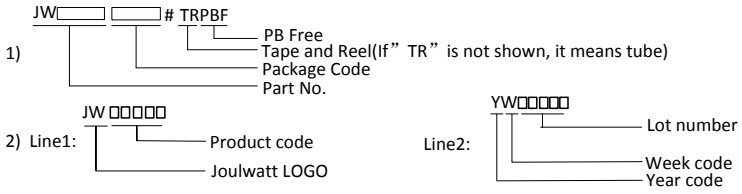
TYPICAL APPLICATION



ORDER INFORMATION

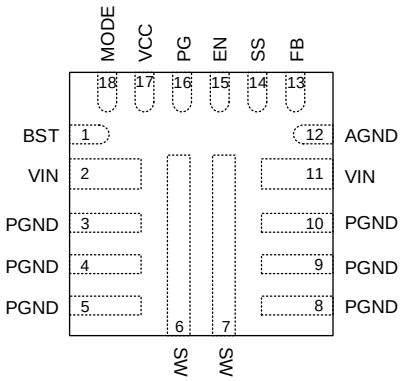
DEVICE[1)]	PACKAGE	TOP MARKING[2)]
JWH5084QFNZ#TRPBF	QFN3.5X3.5-18	JWH5084 YW□□□□□

Notes:



PIN CONFIGURATION

TOP VIEW



ABSOLUTE MAXIMUM RATING[1)]

VIN Pin..... -0.3V to 20V
SW Pin..... -0.3V (-5V for 25ns) to 20V (25V for 25ns)
VIN-SW.....-0.3V (-5V for 25ns) to 20.3V (25V for 25ns)
EN Pin……-0.3V to 20V
BST-SW ..... -0.3V to 4V (5V for 25ns)
VCC Pin ..... -0.3V to 4V
PG Pin ..... -0.3V to 6V
All other Pins ..... -0.3V to 4V
Junction Temperature [2)] 150ºC
Lead Temperature 260ºC
Storage Temperature……...-65 ºC to +150 ºC
ESD Susceptibility (Human Body Model) ..... ±2kV
Charged device model (CDM), per JEDEC specification JESD22- V C101..... ±500V

RECOMMENDED OPERATING CONDITIONS[3)]

Input Voltage V_{IN} ..... 4.5V to 17V
Output Voltage V_{OUT} ..... 0.6V to 5.5V
Maximum Output Current I_{OUT_MAX} 12A
Operation Junction Temperature T_j.. ..... -40°C to 125°C

THERMAL PERFORMANCE[4)]

	θ_{JA} [5)]	θ_{JB} [5)]	θ_{Jc_TOP} [5)]
QFN3.5X3.5-18	29.5	8.6	17.0

ºC/W

Note:

1) Exceeding these ratings may damage the device. These stress ratings do not imply function operation of the device at any other conditions beyond those indicated under RECOMMENDE OPERATING CONDITIONS.

2) The JWH5084 includes thermal protection that is intended to protect the device in overload conditions. Continuous operation over the specified absolute maximum operating junction temperature may damage the device.

3) The device is not guaranteed to function outside its operating conditions.

4) Measured on JESD51-7, 4-layer PCB.

5) θ_{JA} Thermal resistance from junction to ambient.

θ_{JB} Thermal resistance from junction to board around PGND pin soldering point.

θ_{Jc_TOP} Thermal resistance from junction to top of package.

ELECTRICAL CHARACTERISTICS

V_{IN}=12V, T_J=-40℃~125℃，Unless otherwise stated.

Item	Symbol	Conditions	Min.	Typ.	Max.	Unit
V_{IN} Under Voltage Lock-out Threshold	V_{IN_HTH}	V_{IN} rising, V_{CC}=3.3V	3.1	3.4	3.7	V
	V_{IN_LTH}	V_{IN} falling, V_{CC}=3.3V	2.95	3.25	3.55	V
Shutdown Current	I_{SD}	V_{EN}=0		8		μA
Supply Current	I_Q	V_{EN}=3.3V, V_{FB}=0.7V		580	800	μA
Enable Input Rising Threshold	V_{EN_HTH}		1.17	1.225	1.27	V
Enable Input Falling Threshold	V_{EN_LTH}		1.03	1.09	1.17	V
Enable Hysteresis	$V_{EN\_TH\_HYS}$			0.14		V
EN Pull-Up Current	I_{ENP1}	V_{EN}=1.0V	0.35	2	2.95	μA
	I_{ENP2}	V_{EN}=1.3V	3	4.3	5.5	μA
Feedback Voltage	V_{REF}		594	600	606	mV
Top Switch Resistance	$R_{DS(ON)T}$			13.3		mΩ
Bottom Switch Resistance	$R_{DS(ON)B}$			4.3		mΩ
Top Switch Leakage Current	I_{LEAK_TOP}	V_{IN}=17V, V_{SW}=0V			10	μA
Bottom Switch Leakage Current	I_{LEAK_BOT}	V_{IN}=17V, V_{SW}=17V			10	μA
Valley current limit	I_{LIM_POS1}		9.775	11.5	13.225	A
	I_{LIM_POS2}		11.73	13.9	15.87	A
Bottom Switch Negative Current Limit	I_{LIM_NEG}			-7.5		A
Minimum On Time[6)]	T_{ON_MIN}				50	ns
Minimum Off Time[6)]	T_{OFF_MIN}			100	180	ns
Switching Frequency	F_{SW}	25℃	340	400	460	kHz
		25℃	680	800	920	kHz
		25℃	1020	1200	1380	kHz
Discharge FET Ron	R_{DIS}			80	150	Ω
Soft-Start Charge Current	I_{SS_CHAR}	V_{SS}=0V	4.9	6	7.1	μA
Soft-Start Discharge FET Ron	$R_{SS\_DISCHAR}$	V_{CC}=3V	1.5	2.3	3	kΩ
Soft-Start Time[6)]	T_{SS}	Internal SS time		1		ms
VCC Under-voltage Lockout Threshold	V_{CC_HTH}	VCC rising	2.65	2.8	2.95	V
	V_{CC_LTH}	VCC falling	2.35	2.5	2.65	V
VCC Regulator	V_{CC}		3.1	3.2	3.35	V
VCC Output Current Limit	I_{LIM_VCC}		90	145	200	mA
VCC Load Regulation		I_{CC}=25mA		0.5		%
Power Good High Threshold	PG_{HTH}	V_{FB} from low to high	90%	93%	96%	V_{REF}
		V_{FB} from high to low	104%	107%	110%	V_{REF}

V_{IN}=12V, T_J=-40℃~125℃，Unless otherwise stated.						
Item	**Symbol**	**Conditions**	**Min.**	**Typ.**	**Max.**	**Unit**
Power Good Low Threshold	PG_{LTH}	V_{FB} from low to high	113%	116%	119%	V_{REF}
		V_{FB} from high to low	81%	84%	87%	V_{REF}
Power Good Delay Time	$PG_{\_DLY}$	V_{PG} from low to high	160	260	370	us
Power Good Sink Current	I_{PG}	V_{PG}=0.5V	10			mA
Output Over-voltage Threshold		V_{FB} Rising	118%	121%	124%	V_{REF}
Output Under-voltage Threshold		V_{FB} Falling	65%	68%	71%	V_{REF}
Thermal Shutdown[6)]	T_{TSD}			160		°C
Thermal Shutdown hysteresis[6)]	T_{TSD_HYST}			15		°C
VCC Regulator Thermal Shutdown[6)]				171		°C
VCC Regulator Thermal Shutdown hysteresis[6)]				18		°C

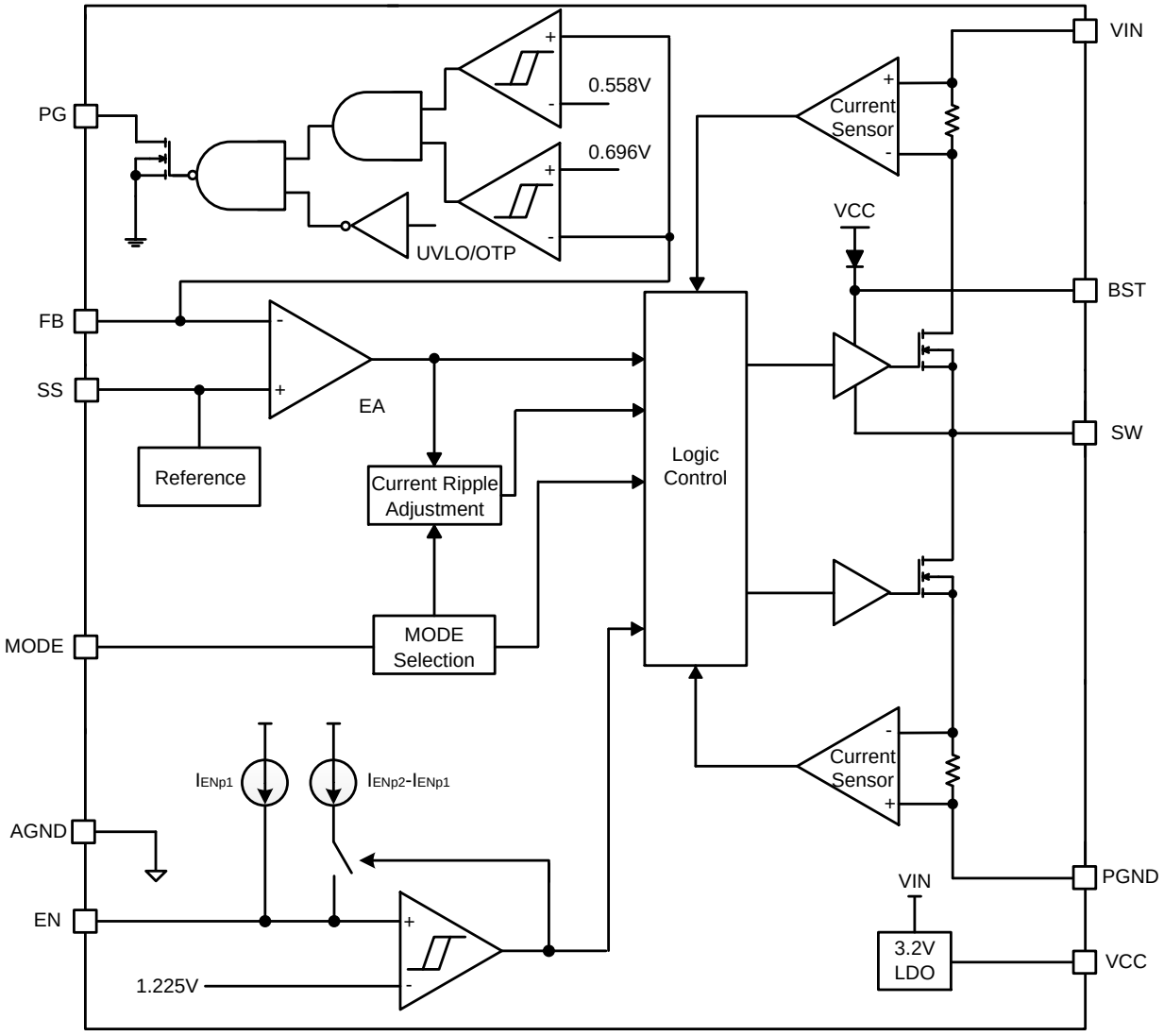
Note：

6) Guaranteed by design.

PIN DESCRIPTION

Pin	Name	Description
1	BST	Connect a 0.1uF capacitor between BST and SW pin to supply current for the top switch driver.
2,11	VIN	Input voltage pin. VIN supplies power to the IC. Connect a 4.5V to 17V supply to VIN and bypass VIN to GND with a suitably large capacitor to eliminate noise on the input to the IC
3,4,5,8,9,10	GND	Power ground pin
6,7	SW	SW is the switching node that supplies power to the output. Connect the output LC filter from SW to the output load.
12	AGND	Analog ground pin. Select AGND as the control circuit reference point.
13	FB	Feedback. An external resistor divider from the output to AGND (tapped to FB) sets the output voltage. It is recommended to place the resistor divider as close to FB as possible. Vias should be avoided on the FB traces.
14	SS	Soft-start time setting pin. The soft-start time is determined by the capacitance between SS pin and AGND.
15	EN	Enable control pin. Pull this pin high to turn on the regulator. Do not leave this pin floating.
16	PGOOD	Power good monitor output. Open drain output when the output voltage is within 93% to 116% of internal reference voltage.
17	VCC	Internal LDO Output. Power supply for internal analog circuits and driving circuit. Decouple this pin to ground with a minimum 1uF ceramic capacitor.
18	MODE	Operation mode selection. Program MODE to select the operating switching frequency, and current limit.

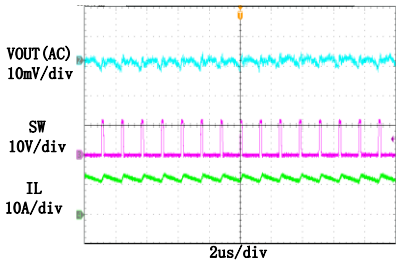
BLOCK DIAGRAM



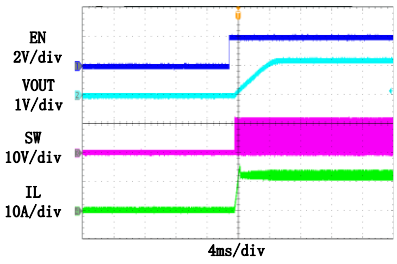
TYPICAL PERFORMANCE CHARACTERISTICS

V_{IN} = 12V, V_{OUT} = 1.2V, L = 0.68μH, C_{OUT} = 47μF×4, F_{SW} = 800kHz, T_A = +25°C, unless otherwise noted.

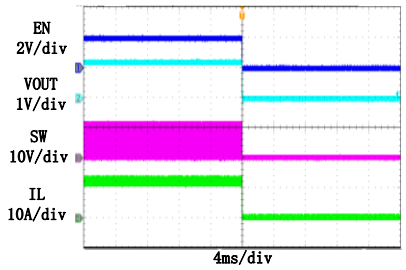
Steady State Test
V_{IN}=12V, V_{OUT}=1.2V
I_{OUT}=12A



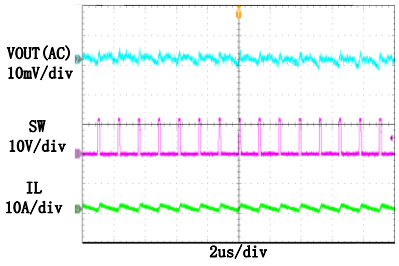
Startup through Enable
V_{IN}=12V, V_{OUT}=1.2V
I_{OUT}=12A



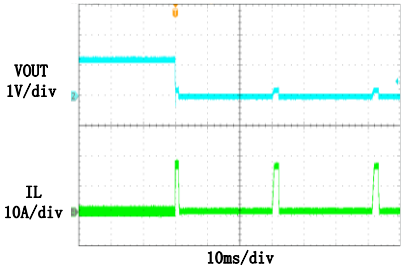
Shutdown through Enable
V_{IN}=12V, V_{OUT}=1.2V
I_{OUT}=12A



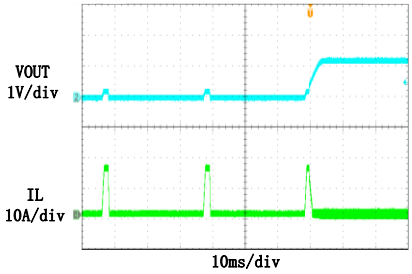
Steady State Test
V_{IN}=12V, V_{OUT}=1.2V
I_{OUT}=0A



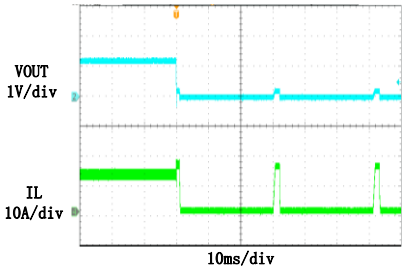
Short Circuit Protection
V_{IN}=12V, V_{OUT}=1.2V
I_{OUT}=0A→Short, I_{LIM_POS2}



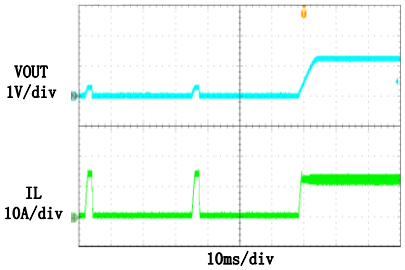
Short Circuit Recovery
V_{IN}=12V, V_{OUT}=1.2V
I_{OUT}=Short→0A, I_{LIM_POS2}



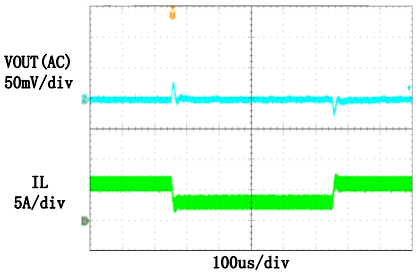
Short Circuit Protection
V_{IN}=12V, V_{OUT}=1.2V
I_{OUT}=12A→Short, I_{LIM_POS2}



Short Circuit Recovery
V_{IN}=12V, V_{OUT}=1.2V
I_{OUT}=Short→12A, I_{LIM_POS2}



Load Transient
V_{IN}=12V, V_{OUT}=1.2V
I_{OUT}=3A~6A



TYPICAL PERFORMANCE CHARACTERISTICS

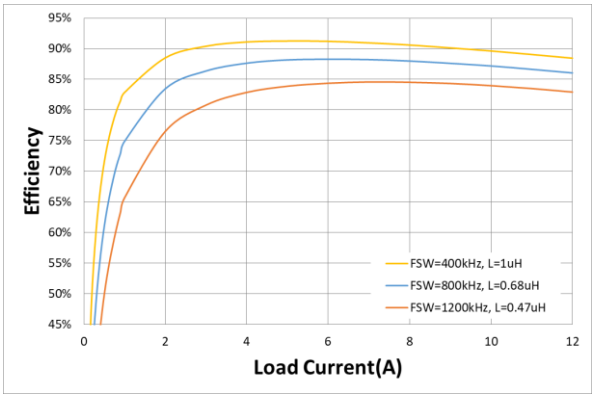


Figure 1. Efficiency vs. Load Current

(V_{IN}=12V, V_{OUT}=1.2V)

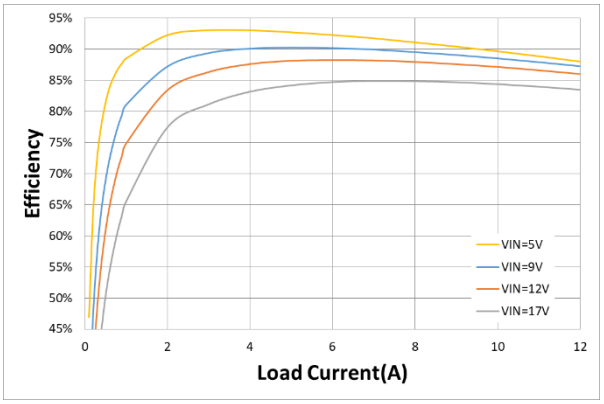


Figure 2. Efficiency vs. Load Current

(V_{OUT}=1.2V, L=0.68uH, F_{SW}=800kHz)

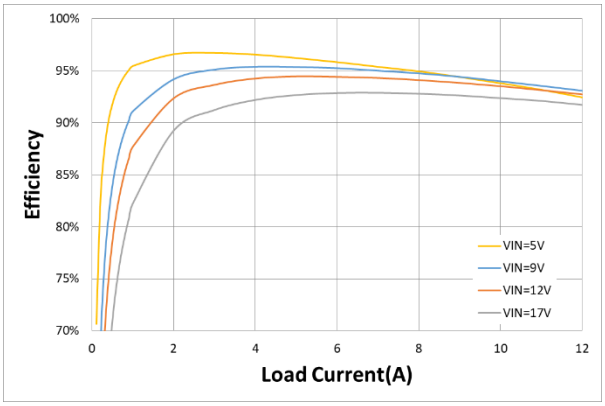


Figure 3. Efficiency vs. Load Current

(V_{OUT}=3.3V, L=1.5uH, F_{SW}=800kHz)

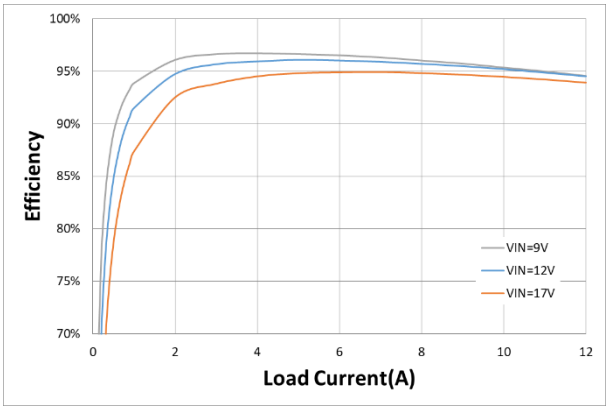


Figure 4. Efficiency vs. Load Current

(V_{OUT}=5V, L=2.2μH, F_{SW}=800kHz)

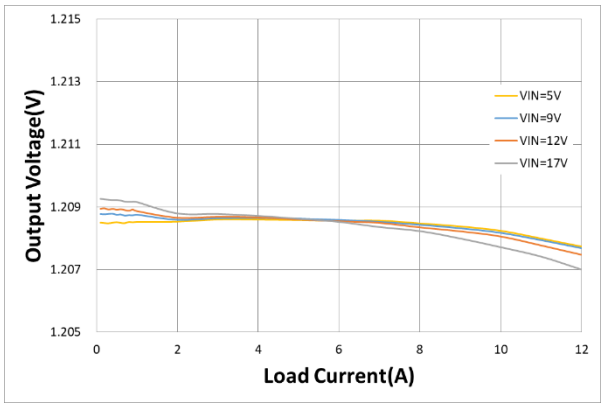


Figure 5. Load Regulation

(V_{OUT}=1.2V, L=0.68uH, F_{SW}=800kHz)

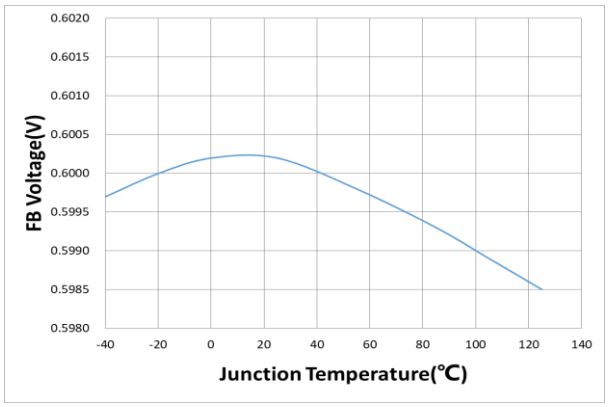


Figure 6. FB Voltage Regulaion vs. Junction Temperature

FUNCTIONAL DESCRIPTION

JWH5084 is a synchronous step-down regulator based on I2 control architecture. It regulates input voltages from 4.5V to 17V down to as low as 0.6V output voltage, and is capable of supplying up to 12A of load current.

Power Switch

N-Channel MOSFET switches are integrated on the JWH5084 to down convert the input voltage to the regulated output voltage. Since the top MOSFET needs a gate voltage greater than the input voltage, a boost capacitor connected between BST and SW pins is required to drive the gate of the top switch. The boost capacitor is charged by the internal LDO when SW is low.

Mode Selection

The JWH5084 operates in forced continuous conduction mode (FCCM), and the switching frequency is fairly constant.

The JWH5084 has three options for switching frequency selection. The switching frequency and current limit selection could be done by choosing the resistance value of the resistor connected between MODE and AGND or VCC (See Table 1).

Table 1 --- Mode selection

R_{M_L} (KΩ)	R_{M_H} (KΩ)	Current limit	Fs[7)]
5.1	300	I_{LIM_POS1}	400k
10	200	I_{LIM_POS2}	400k
20	160	I_{LIM_POS1}	800k
20	120	I_{LIM_POS2}	800k
51	200	I_{LIM_POS1}	1200k
51	180	I_{LIM_POS2}	1200k

Note:

7) Refer to ELECTRICAL CHARACTERISTICS for more accurate switching frequency data.

Shut-Down Mode

The JWH5084 shuts down when voltage at EN pin is below 0.3V. The entire regulator is off and the supply current consumed by the JWH5084 drops below 8uA.

V_{IN} Under-Voltage Protection

In addition to the enable function, the JWH5084 provides an Under Voltage Lock-out (UVLO) function that monitors the input voltage. To prevent operation without fully-enhanced internal MOSFET switches, this function inhibits switching when input voltage drops below the UVLO-falling threshold. The IC resumes switching when input voltage exceeds the UVLO-rising threshold.

Enable and Adjustable UVLO Protection

The JWH5084 is enabled when the VIN pin voltage rises above 3.4V and the EN pin voltage exceeds the enable threshold of 1.225V. The JWH5084 is disabled when the VIN pin voltage falls below 3.25V or when the EN pin voltage is below around 1.1V. Do not leave this pin floating. If an application requires a different turn-on and turn-off thresholds respectively, use a resistive divider connected between VIN and ground with the central tap connected to EN to adjust the input voltage UVLO. (Shown in Figure 7). The EN pin has a pull-up current I_{ENP1} that sets the default state of the pin when it is floating. This current increases to I_{ENP2} when the EN pin voltage crosses the turn-on threshold. The UVLO thresholds can be set by following equation:

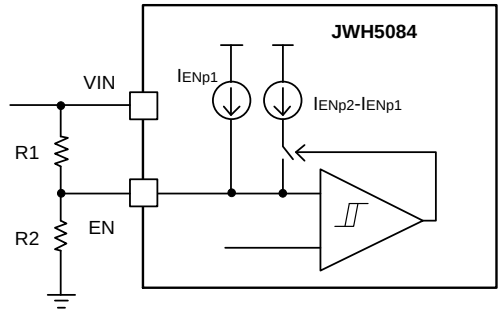


Figure 7. Adjustable UVLO

The input voltage UVLO threshold (V_{UVLO}) and hysteresis (V_{UVLO_HYS}) can be calculated by the following equation.

$$R_1 = \frac{V_{START} \times \frac{V_{EN\_LTH}}{V_{EN\_HTH}} - V_{STOP}}{I_{ENP1}\left(1 - \frac{V_{EN\_LTH}}{V_{EN\_HTH}}\right) + \left(I_{ENP2} - I_{ENP1}\right)}$$

$$R_2 = \frac{R_1 \times V_{EN\_HTH}}{V_{START} + \left(R_1 \times I_{ENP1}\right) - V_{EN\_HTH}}$$

where

V_{EN_HTH} = 1.225V

V_{EN_LTH} = 1.09V

I_{ENP2} = 4.3uA

I_{ENP1} = 2uA

Soft Start

Soft-start is designed in JWH5084 to prevent the converter output voltage from overshooting during startup and short-circuit recovery. An internal current source (I_{SS}) of 6uA is designed to charge the external soft-start capacitor (C_{SS}) and generates a soft-start (SS) voltage ramping up from 0V to 1.5V. When it is less than internal reference voltage ($V_{REF,}$ typ. 0.6V), SS voltage overrides V_{REF} and the error amplifier uses SS voltage as the reference. When SS exceeds V_{REF}, V_{REF} regains control.

The soft start time (10% to 90%) T_{SS} can be calculated by the following equation.

$$T_{SS}(ms) := \frac{C_{SS}(nF) \cdot V_{REF}(V) \cdot 0.8}{I_{SS}(\mu A)}$$

where C_{SS} is the soft-start capacitance connected between SS pin and AGND pin.

The JWH5084 has a configured external soft start time and a constant internal soft start time, it will follow the slower one between them. Therefore, the minimum soft start time is about 1ms even a smaller capacitor is used. The soft start will not be ready until both the internal and external SS voltage exceeds 0.85V.

At power up, the soft start pin is discharged before MOSFETs switching to ensure a proper power up. Also, during normal operation, the JWH5084 will stop switching and the soft-start pin will be discharged, when the VIN UVLO is exceeded, EN pin pulled below 1.1V, or a thermal shutdown event occurs.

Current Sense and Over-Current Protection (OCP)

The JWH5084 features an on-die current sense and two programmable positive current limit thresholds.

The current limit is active when the JWH5084 is enabled. During the low side MOSFET on state, the SW current (inductor current) is sensed, and compared with current limit cycle-by-cycle. The high side MOSFET is only allowed to turn on when the sensed current is below the internal OCP threshold I_{LIM} (during the low side MOSFET on state) to limit the SW valley current cycle-by-cycle.

The OCP HICCUP is active during soft start, once OCP HICCUP is active, if the JWH5084 detects over-current condition for consecutive 1000 cycles, it enters HICCUP mode. After soft start, when the current is limited by OCP, the output voltage tends to drop, if the FB drops below under-voltage protection (UVP) threshold for 1ms, it enters HICCUP mode. In HICCUP mode, the JWH5084 latches off the high side MOSFET immediately, and latches off low side MOSFET after ZCD is detected. Meanwhile, the SS capacitor is also discharged. After about 31ms, the JWH5084 will try to soft start

automatically. If the over-current condition still holds, the JWH5084 repeats this operation cycle until the over-current condition disappears, and the output voltage rises smoothly back to the regulation level.

Negative Inductor Current limit

When the low side MOSFET detects a -7.5A current, the part turns off the low side MOSFET to limit the negative current.

Pre-Bias Start-Up

The JWH5084 has been designed for a monotonic start-up into pre-biased loads. If the output is pre-biased to a certain voltage during start-up, the IC disables switching for both the high-side and low-side MOSFETs until the voltage on the SS capacitor exceeds the sensed output voltage at FB. Before SS voltage reaches pre-biased FB level, if the BST voltage (from BST to SW) is lower than 1.8V, the low-side MOSFET is turned on to allow the BST voltage to be charged through VCC. The low-side MOSFET is turned on for very narrow pulses, so the drop in pre-biased level is negligible.

Output Voltage Discharge

When the JWH5084 is disabled through EN, it enables the output voltage discharge mode. This causes both the high side MOSFET and the low side MOSFET to latch off. A discharge FET connected between SW and PGND is turned on to discharge the output voltage. The typical switch on resistance of this FET is about 80Ω. Once the FB voltage drops below 10%* V_{REF}, the discharge FET is turned off.

Output Over-voltage Protection

The JWH5084 monitors the output voltage by connecting FB to the tap of the output voltage feedback resistor divider to detect an overvoltage condition. This provides auto-recovery OVP mode.

If the FB voltage exceeds 116% of the REF voltage, the high side MOSFET is turned off and PG goes low after 60us delay until the FB voltage drops below 107% of REF voltage. Meanwhile, the low side MOSFET remains on until it hits the low-side negative current limit (NOCP). Once it hits NOCP, the low side MOSFET is turned off and the high side MOSFET is turned on until the negative current reaches to zero. The JWH5084 keeps this operation to try to bring down the output voltage. Furtherly, if the FB voltage exceeds 131% of the REF voltage, the secondary OVP is triggered and the high side MOSFET is not allowed turned on again until the FB voltage drops below 125% of REF voltage.

Power Good

The JWH5084 has power-good (PG) output. The PG pin is the open drain of a MOSFET. Connect to VCC or another voltage source through a resistor. After applying the input voltage, the power MOSFETs start switching, PG is pulled to GND before soft start is ready. After the FB voltage reaches 93% of the REF voltage and soft start is ready, PG is pulled high after about 260us. When the FB voltage drops to 84% of the REF voltage, PG is pulled low after 60us delay. And if the FB voltage drops to 68% of the REF voltage, PG is pulled low immediately.

When the FB voltage exceeds 116% of the REF voltage, PG is pulled low after 60us delay. And if the FB voltage exceeds 121% of the REF voltage, PG is pulled low immediately. When the FB voltage drops to 107% of the REF voltage, PG is pulled high again after 260us delay.

Once EN UVLO, OVP, UVP or OTP is triggered, PG is pulled low within 1us deglitch time.

If the input supply fails to power the JWH5084, PG is clamped low even though PG is tied to an external DC source through a pull-up resistor.

Thermal Protection

When the temperature of the JWH5084 rises above 160°C, it is forced into thermal shut-down. This is a non-latch protection, and the regulator becomes active again when the temperature goes below the thermal shutdown threshold.

There is a second higher thermal protection, the threshold is at typically 171°C. The internal LDO will shut down once temperature goes beyond 171°C. The LDO re-starts working when the temperature goes below the second thermal shutdown threshold.

APPLICATION INFORMATION

Output Voltage Set

The output voltage is determined by the resistor divider connected at the FB pin, and the voltage ratio is:

$$V_{FB} = V_{OUT} * \frac{R_L}{R_H + R_L}$$

where V_{FB} is the feedback voltage and V_{OUT} is the output voltage.

To improve efficiency at very light load, using larger value resistors is preferred. However, using too high of resistance causes the circuit to be more susceptible to noise, and voltage errors from the V_{FB} input current will be more noticeable. If R_H is determined, such as 10kΩ, and then R_L can be calculated by:

$$R_L = \frac{R_H}{\frac{V_{OUT}}{0.6} - 1}$$

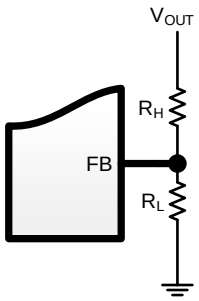


Figure 8. Output Voltage Set

Input Capacitor

The input capacitor is used to supply the AC input current to the step-down converter and maintain the DC input voltage. The capacitors must have a ripple current rating that exceeds the converter's maximum input ripple current. The RMS ripple current through the input capacitor can be calculated by:

$$I_{CIN} = I_{OUT} * \sqrt{\frac{V_{OUT}}{V_{IN}} * \left(1 - \frac{V_{OUT}}{V_{IN}}\right)}$$

where I_{OUT} is the load current, V_{OUT} is the output voltage, V_{IN} is the input voltage.

Thus, the input capacitor can be calculated by the following equation when the input ripple voltage is determined.

$$C_{IN} = \frac{I_{OUT}}{F_{SW} * \Delta V_{IN}} * \frac{V_{OUT}}{V_{IN}} * \left(1 - \frac{V_{OUT}}{V_{IN}}\right)$$

where C_{IN} is the input capacitance value, F_{SW} is the switching frequency, ΔV_{IN} is the input ripple voltage.

The input capacitor can be electrolytic, tantalum or ceramic. To minimizing the potential noise, a small X5R or X7R ceramic capacitor, e.g., 0.1μF, should be placed as close to the IC as possible when using electrolytic capacitors. 3x10μF/25V ceramic capacitors are recommended in typical application.

Output Capacitor

The output capacitor is required to maintain the DC output voltage, and the capacitance value determines the output ripple voltage. The output voltage ripple can be calculated by:

$$\Delta V_{OUT} = \frac{V_{OUT}}{F_{SW} * L} * \left(1 - \frac{V_{OUT}}{V_{IN}}\right) * \left(R_{ESR} + \frac{1}{8 * F_{SW} * C_{OUT}}\right)$$

where C_{OUT} is the output capacitance value and R_{ESR} is the equivalent series resistance value of the output capacitor.

The output capacitor can be low ESR electrolytic, tantalum or ceramic, which lower ESR capacitors get lower output ripple voltage.

The output capacitors also affect the system stability and transient response, and 4x47μF ceramic capacitors are recommended in typical application.

Inductor

The inductor is used to supply constant current to the output load, and the value determines the ripple current which affect the efficiency and the

output voltage ripple. The ripple current is typically allowed to be 30% of the maximum switch current limit, thus the inductance value can be calculated by:

$$L = \frac{V_{OUT}}{F_{SW} * \Delta I_L} * \left(1 - \frac{V_{OUT}}{V_{IN}}\right)$$

where V_{IN} is the input voltage, V_{OUT} is the output voltage, F_{SW} is the switching frequency, and ΔI_L is the peak-to-peak inductor ripple current.

External Bootstrap Capacitor

The bootstrap capacitor is required to supply voltage to the top switch driver. A 0.1μF low ESR ceramic capacitor is recommended to connected to the BST pin and SW pin.

PCB Layout Note

The PCB layout is critical for best operating performance, follow the guidelines as below.

1. Four-layer or six-layer PCB with maximum ground plane is highly recommended for good thermal performance.
2. Place the input decoupling capacitor as close to device (VIN pin and PGND) as possible to eliminate noise at the input pin. The loop area formed by input capacitor and GND must be minimized. VIN pins should have equal input capacitors on each side of the IC.
3. AGND island and PGND plane is recommended to be connected at the single point close to AGND Pin (Pin 12), as shown in figure 9. If a solid PGND plane on inner layer is not available for PCB design, it is highly recommended to connect the AGND to the point of the VOUT capacitor's ground directly.
4. Place as many PGND vias as possible and make the ground plane as large as possible to optimize heat dissipation and parasitic impedance.
5. Place the VCC decoupling capacitor as close as possible to the VCC pin.
6. Place the BST capacitor as close as possible to the BST pin. 20mil or wider traces are recommended for the connection.
7. Place the feedback resistors close to device to minimize the feedback trace, and put the feedback trace far away from the inductor and noisy power traces like SW node.
8. Keep the switching node SW short to prevent excessive capacitive coupling.
9. Make VIN, VOUT and ground bus connections as wide as possible to reduce voltage drop on the input and output paths of the converter and maximize efficiency.

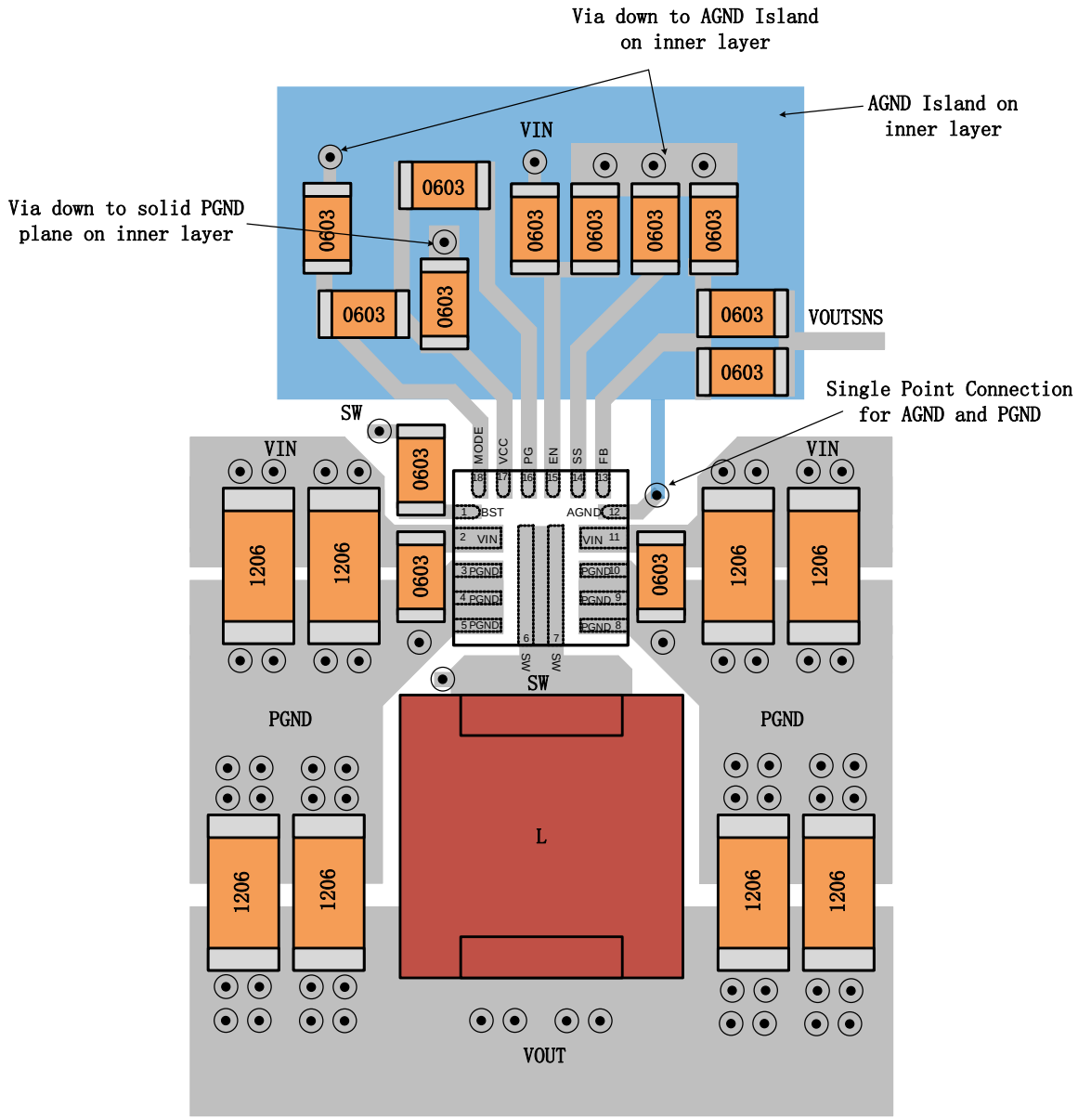
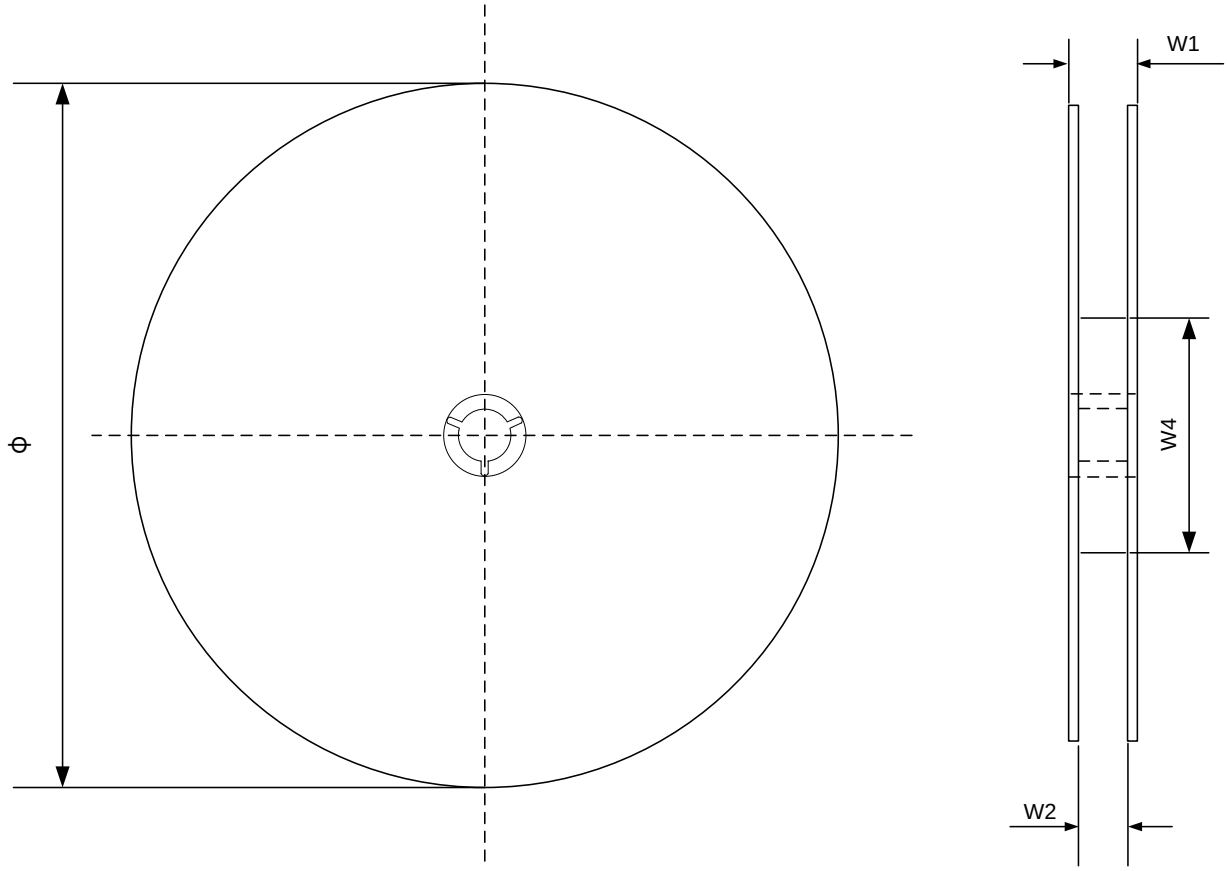


Figure 9. PCB Layout Recommendation

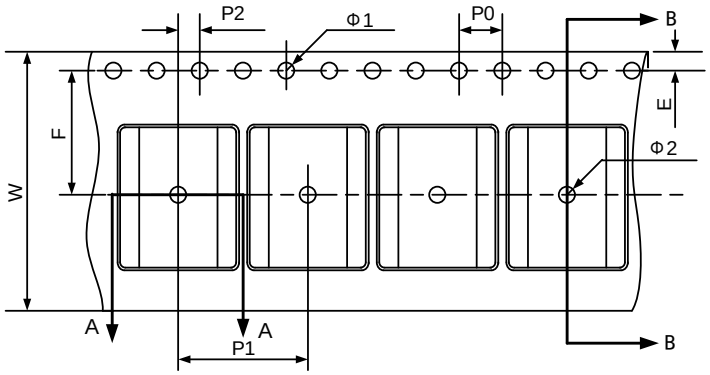
TAPE AND REEL INFORMATION

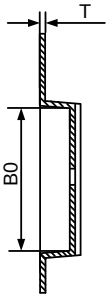
Reel UNIT: mm



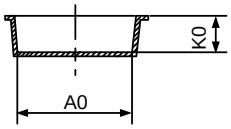
Package	Diameter Φ	Thickness W1	Width W2	W4
QFN3.5X3.5-18	330±2	17.6±2	12.4±2	100±2

Carrier Tape UNIT: mm





SECTION B-B



SECTION A-A

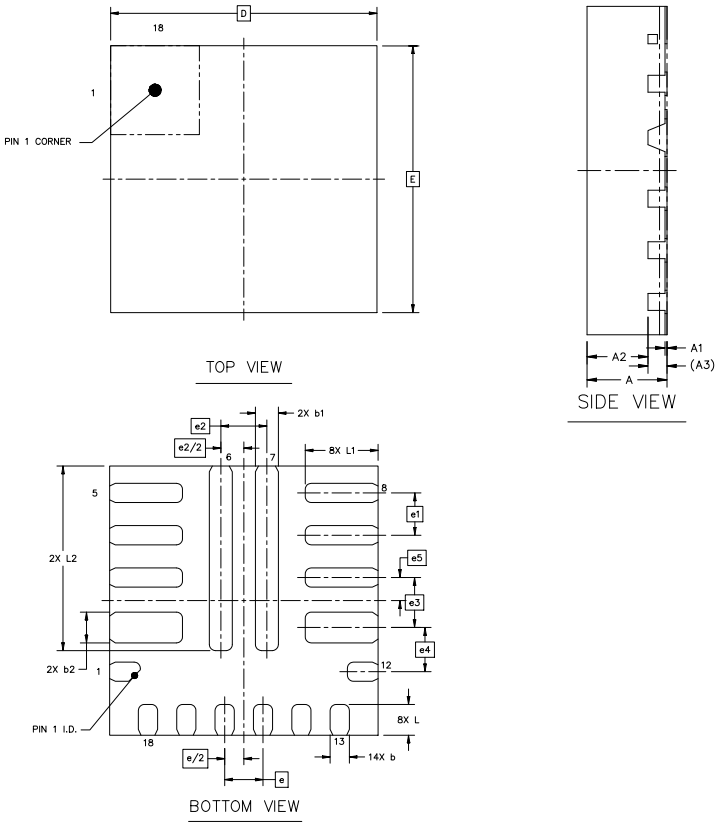
Note :

1) The carrier type is black, and colorless transparent.
2) Carrier camber is within 1mm in 100mm.
3) 10 pocket hole pitch cumulative tolerance:±0.20.
4) All dimensions are in mm.

Package	Tape dimensions (mm）											
	P0	P2	P1	A0	B0	W	T	K0	Φ1	Φ2	E	F
QFN3.5X3.5-18	4.0±0.1	2.0±0.1	8.0±0.1	3.8±0.15	3.8±0.15	12.0±0.3	0.25±0.2	1.05±0.2	1.5±0.10	1.60±0.1	1.75±0.1	5.50±0.10

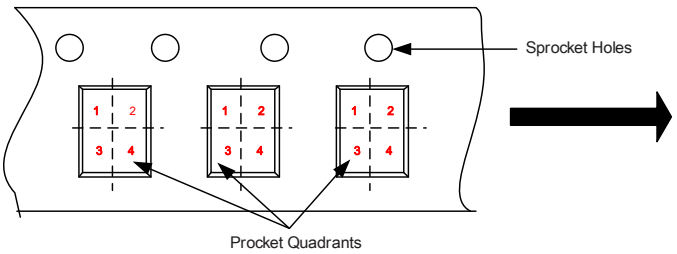
PACKAGE OUTLINE

QFN3.5X3.5-18 UNIT: mm



SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	0.80	0.85	0.90
A1	0.00	0.02	0.05
A2	—	0.65	—
A3	0.203 REF		
b	0.20	0.25	0.30
b1	0.25	0.30	0.35
b2	0.35	0.40	0.45
D	3.40	3.50	3.60
E	3.40	3.50	3.60
e	0.50 BSC		
e1	0.55 BSC		
e2	0.60 BSC		
e3	0.65 BSC		
e4	0.575 BSC		
e5	0.30 BSC		
L	0.30	0.40	0.50
L1	0.85	0.95	1.05
L2	2.30	2.40	2.50

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPAE



Package Type	Pin1 Quadrant
QFN3.5X3.5-18	1

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