

AT24C02CT DATASHEET

Specification Revision History:

Version	Date	Description
V1.0	2019/08	New
V1.1	2021/05	Modify Ordering Information
V1.2	2025/02	Modify Ordering Information
V1.3	2025/03	Add application precautions and overall typesetting.

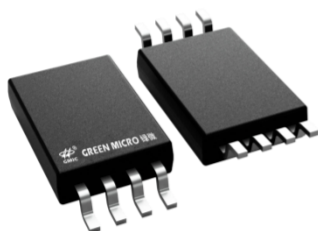
Description

The 24C02 is I2C-compatible Serial EEPROM (Electrically Erasable Programmable Memory) device. It contains a memory array of 2Kbits (256 bytes), which is organized in 8 bytes per page.

Features

- ※ Single Supply Voltage and High Speed
 - Minimum operating voltage down to 1.6V
 - 1 MHz clock from 2.5V to 5.5V
 - 400kHz clock from 1.7V to 5.5V
- ※ Low power CMOS technology
 - Read current 0.2mA(400kHz, typical)
 - Write current 0.8mA(400kHz, typical)
- ※ Schmitt Trigger, Filtered Inputs for Noise Suppression
- ※ Sequential & Random Read Features
- ※ Page Write Modes, Partial Page Writes Allowed
- ※ Write protect of the whole memory array
- ※ Self-timed Write Cycle (5ms maximum)
- ※ High Reliability
 - Endurance: 1 Million Write Cycles
 - Data Retention: 100 Years
 - ESD HBM: 4 kV
 - Latch-up Capability: +/-200mA(25C)
- ※ Package: PDIP8, SOP8, TSSOP8, UDFN8, MSOP8, SOT23-5 and TSOT23-5

The appearance of the product



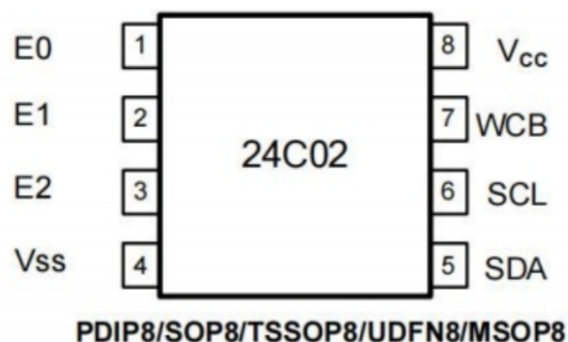
TSSOP-8

Ordering Information

Product Model	Package Type	Marking	Packing	Packing Qty
AT24C02CT	TSSOP-8	24C02 G630	REEL	3000PCS/REEL

Pin Configuration

Pin Configuration



Pin Definition

Pin	Name	Type	Description
1	E0	Input	Slave Address Setting
2	E1	Input	Slave Address Setting
3	E2	Input	Slave Address Setting
4	Vss	Ground	Ground
5	SDA	I/O	Serial Data Input and Serial Data Output
6	SCL	Input	Serial Clock Input
7	WCB	Input	Write Control,Low Enable Write
8	V _{cc}	Power	Power

Pin Descriptions

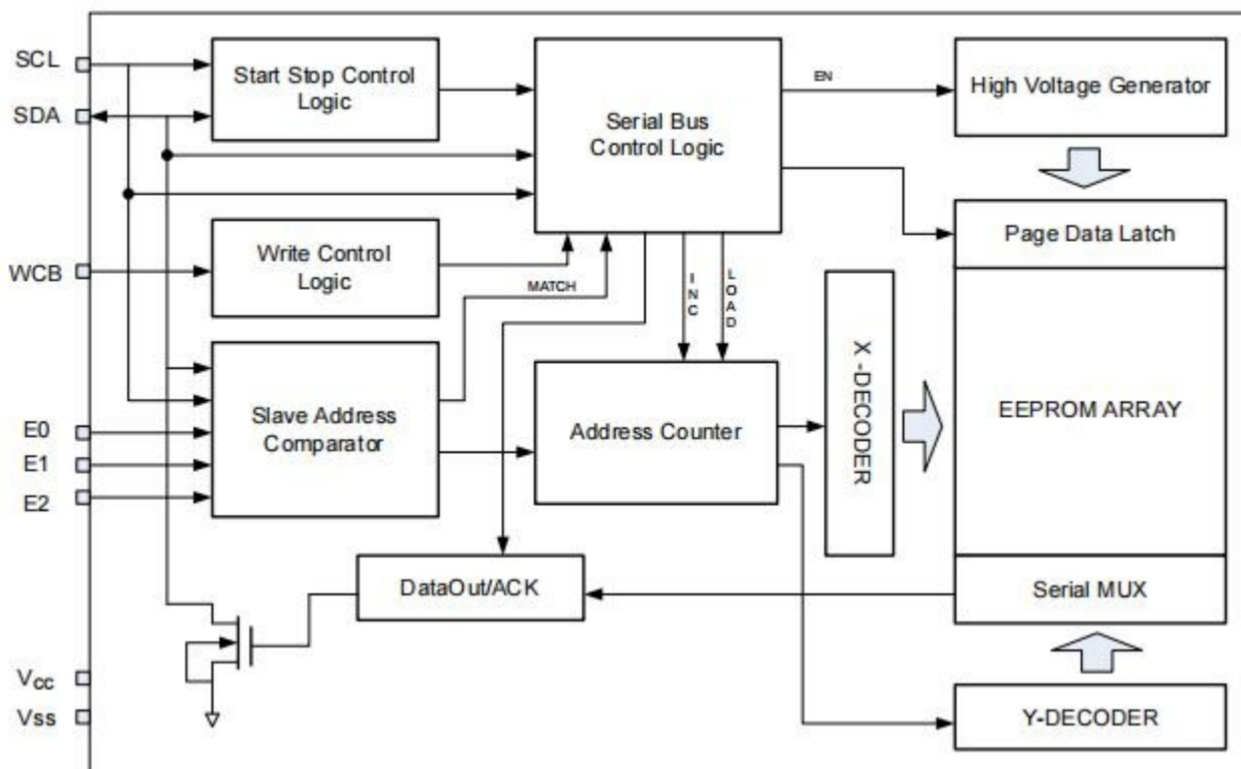
Serial Clock(SCL): The SCL input is used to positive-edge clock data in and negative-edge clock data out of each device.

Serial Data(SDA): The SDA pin is bidirectional for serial data transfer.This pin is open drain driven and may be wire-ORed with any number of other open-drain or open-collector devices.

Device Addresses(E2、 E1、 E0): The E2,E1 and E0 pins are device address inputs. Typically,the E2,E1 and E0 pins are for hardware addressing and a total of 8 devices can be connected on a single bus system.If these pins are left floating,the E2,E1 and E0 pins will be internally pulled down to Vss.

Write Control (WCB): The Write Control input,when WCB is connected directly to Vcc,all write operations to the memory are inhibited.When connected to Vss,allows normal write operations.If the pin is left floating,the WCB pin will be internally pulled down to Vss.

Block Diagram



Electrical Characteristics

Absolute Maximum Ratings^[1]

Symbol	Parameter	Min.	Max.	Unit
T_{STG}	Storage Temperature	-65	150	°C
T_A	Ambient operating temperature	-40	125	°C
V_{CC}	Supply Voltage	-0.5	6.25	V
V_{ID}	Input or output range	-1.0	6.25	V
I_{OL}	DC output current (SDA=0)	-	5	mA

Note:[1]Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operational listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

Pin Capacitance^[1]

Symbol	Parameter	Max.	Units	Test Condition
$C_{I/O}$	Input /Output Capacitance(SDA)	8	pF	$V_{I/O}=V_{SS}$
C_{IN}	Input Capacitance (E0, E1,E2,WCB,SCL)	6	pF	$V_{IN}=V_{SS}$

Note:[1]Test Conditions: $T_A=25^{\circ}C$, $f_{SCL}=1MHz$, $V_{CC}=5.0V$.

DC Characteristics(Unless otherwise specified, $V_{CC}=1.7V$ to $5.5V$, $T_A=-40^{\circ}C$ to $125^{\circ}C$)

Symbol	Parameter	Min.	Typ.	Max.	Unit	Test Condition
V_{CC}	Supply Voltage	1.6	-	5.5	V	
		1.7	-	5.5	V	
I_{sb}	Standby Current		-	1.0	μA	$V_{CC}=3.3V$
		-	-	3.0	μA	$V_{CC}=5.5V$
I_{CC1}	Supply Current	-	0.2	0.4	mA	$V_{CC}=5.5V$, Read at 400khz
I_{CC2}	Supply Current	-	0.8	1.6	mA	$V_{CC}=5.5V$ Write at 400khz
I_{LI}	Input Leakage Current	-	0.10	1.0	μA	$V_{IN}=V_{CC}$ or V_{SS}
I_{LO}	Output Leakage Current	-	0.05	1.0	μA	$V_{OUT}=V_{CC}$ or V_{SS}
V_{IL}	Input Low Level	-0.6		$0.3V_{CC}$	V	
V_{IH}	Input High Level	$0.7V_{CC}$	-	$V_{CC}+0.5$	V	
V_{OL1}	Output Low Level $V_{CC}=1.7V(SDA)$			0.2	V	$I_{OL}=1.5\text{ mA}$
V_{OL2}	Output Low Level $V_{CC}=3.0V(SDA)$	-	-	0.4	V	$I_{OL}=2.1\text{ mA}$

AC Characteristics

(Unless otherwise specified, $V_{CC}=1.7V$ to $5.5V$, $T_A=-40^{\circ}C$ to $125^{\circ}C$, $C_L=100pF$,Test Conditions are listed in Notes^[2])

Symbol	Parameter	$1.7 \leq V_{CC} \leq 5.5$			$2.5 \leq V_{CC} \leq 5.5$			Units
		Min.	Typ.	Max.	Min.	Typ.	Max.	
f_{SCL}	Clock Frequency,SCL	-	-	400	-		1000	kHz
t_{LOW}	Clock Pulse Width Low	1.3	-	-	0.4	-	-	μs
t_{HIGH}	Clock Pulse Width High	0.6	-	-	0.4	-	-	μs
t_{AA}	Clock Low to Data Out Valid	0.05	-	0.9	0.05		0.55	μs
t_I	Noise Suppression Time	-	-	0.1	-	-	0.05	μs
t_{BUF}	Time the bus must be free before a new transmission can start	1.3	-	-	0.5	-	-	μs
$t_{HD,STA}$	Start Hold Time	0.6	-	-	0.25	-		μs
$t_{SU,STA}$	Start Setup Time	0.6	-	-	0.25	-	-	μs
$t_{HD,DAT}$	Data In Hold Time	0	-	-	0		-	μs
$t_{SU,DAT}$	Data In Setup Time	0.1	-	-	0.1	-		μs
t_R	Inputs Rise Time ^[1]		-	0.3		-	0.3	μs
t_F	Inputs Fall Time ^[1]		-	0.3			0.1	μs
$t_{SU,STO}$	Stop Setup Time	0.6			0.25	-		μs
t_{DH}	Data Out Hold Time	0.05	-	-	0.05		-	μs
$t_{SU,WCB}$	WCB pin Setup Time	1.2	-	-	0.6	-	-	μs
$t_{HD,WCB}$	WCB pin Hold Time	1.2	-	-	0.6		-	μs
t_{WR}	Write Cycle Time	-	-	5	-	-	5	ms

Notes: [1] This parameter is ensured by characterization not 100% tested

[2] AC measurement conditions:

◇ R_L (connects to V_{CC}):1.3k(2.5V,5.5V),10k(1.7V)

- ◇ Input pulse voltages: $0.3V_{CC}$ to $0.7V_{CC}$
- ◇ Input rise and fall times: $\leq 50\text{ns}$
- ◇ Input and output timing reference voltages: $0.5V_{CC}$

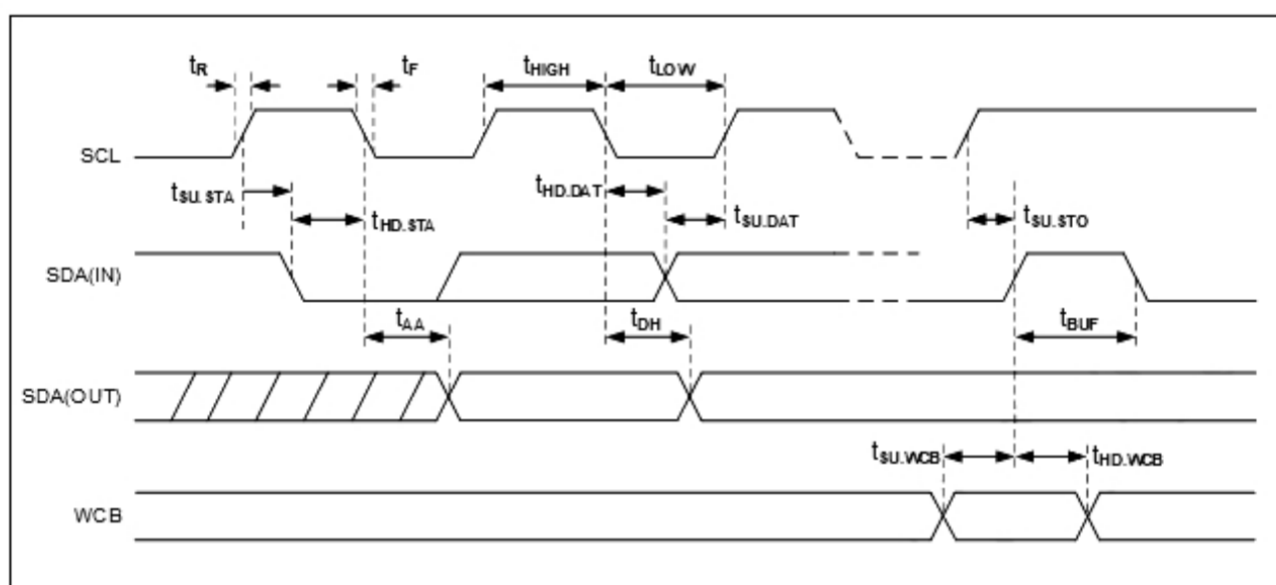
Reliability Characteristic^[1]

Symbol	Parameter	Min.	Typ.	Max.	Unit
EDR ^[2]	Endurance	1,000,000			Write cycles
DRET	Data retention	100			Years

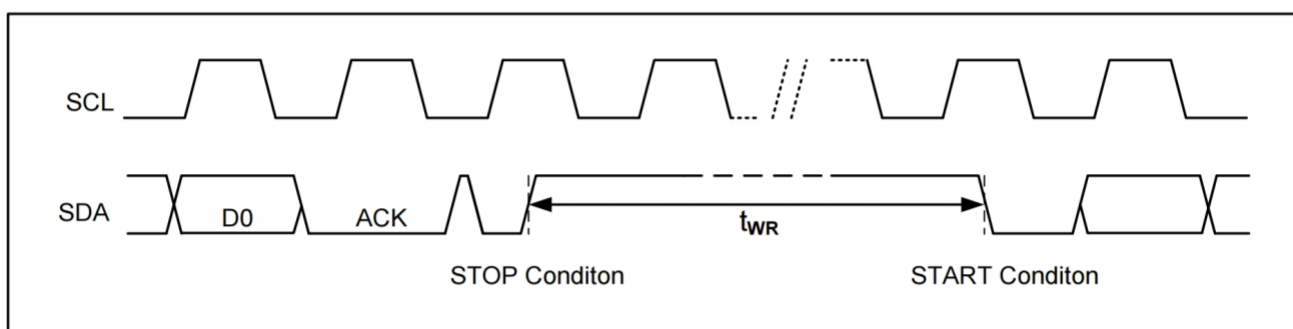
Note: [1] This parameter is ensured by characterization and is not 100% tested

[2] Under the condition: 25°C , 3.3V , Page mode

Bus Timing (Figure ①)



Write Cycle Timing (Figure ②)



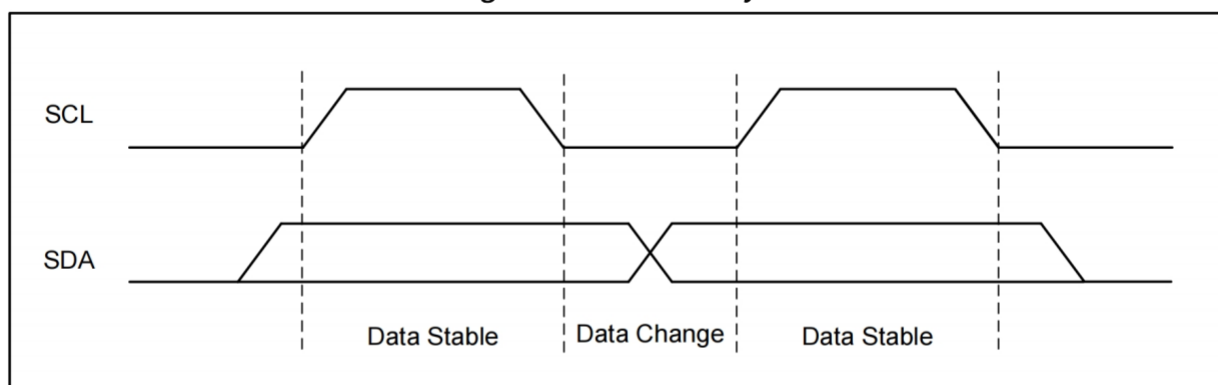
Note: [1] The write cycle time t_{WR} is the time from a valid stop condition of a write sequence to the end of the internal clear/write cycle.

Device Operation

Data Input

The SDA pin is normally pulled high with an external device. Data on the SDA pin may change only during SCL low time periods (see to Figure 4-1). Data changes during SCL high periods will indicate a start or stop condition as defined below.

Figure ③ Data Validity



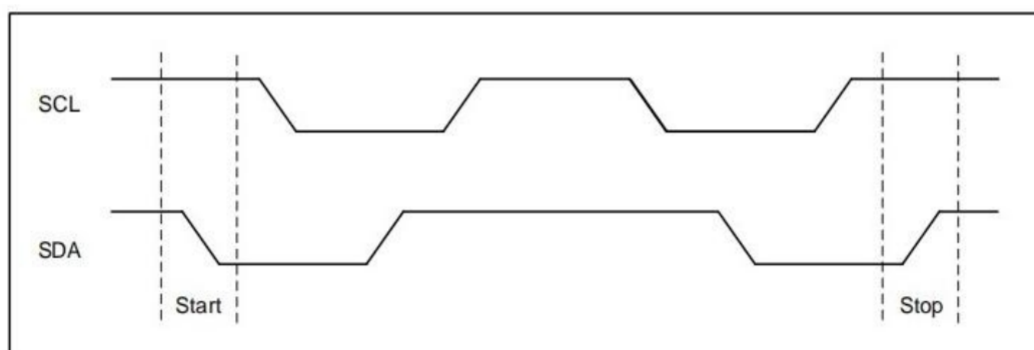
Start Condition

A high-to-low transition of SDA with SCL high is a start condition which must precede any other command (see to Figure ②).

Stop Condition

A low-to-high transition of SDA with SCL high is a stop condition. After a read sequence, the stop command will place the 24C02 in a standby power mode (see Figure ②).

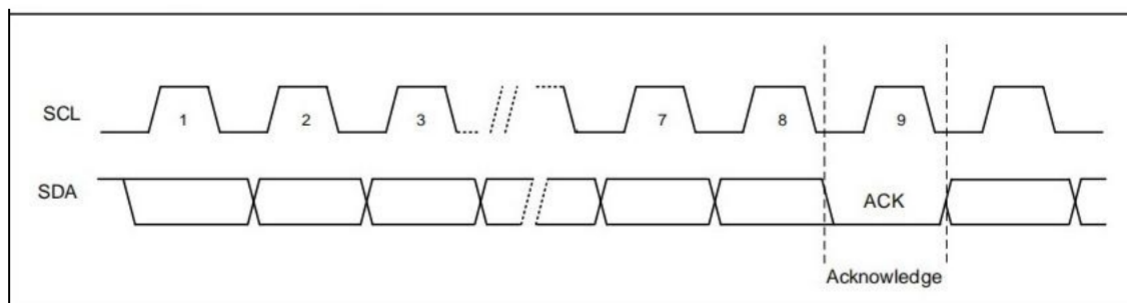
Start and Stop Definition



Acknowledge(ACK)

All addresses and data words are serially transmitted to and from the 24C02 in 8-bit words. The 24C02 sends a “0” to acknowledge that it has received each word. This happens during the ninth clock cycle.

Output Acknowledge (Figure ④)



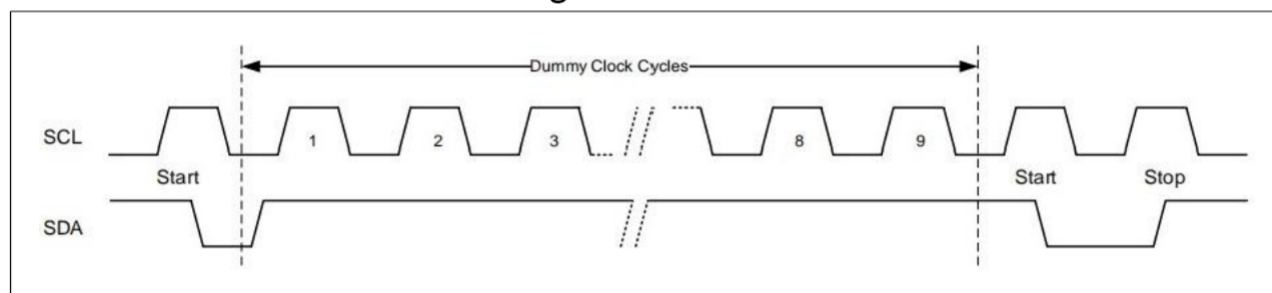
Standby Mode

The 24C02 features a low-power standby mode which is enabled: (a) after a fresh power up, (b) after receiving a STOP bit in read mode, and (c) after completing a self-time internal programming operation.

Soft Reset

After an interruption in protocol, power loss or system reset, any two-wire part can be reset by following these steps: (a) Create a start condition, (b) Clock nine cycles, and (c) create another start bit followed by stop bit condition, as shown below. The device is ready for the next communication after the above steps have been completed.

Figure ⑤ Soft Reset



Device Addressing

The 24C02 requires an 8-bit device address word following a start condition to enable the chip for a read or write operation (see table below). The device address word consists of a mandatory one-zero sequence for the first four most-significant bits, as shown.

Table Device Address

Access area	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Normal Area	1	0	1	0	E2	E1	E0	RN

Table Word Address

Data	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Normal Area	A7	A6	A5	A4	A3	A2	A1	A0

The E2, E1 and E0 device address bits to allow as many as eight devices on the same bus. These bits must compare to their corresponding hardwired input pins.

The E2, E1 and E0 pins use an internal proprietary circuit that biases them to a logic low condition if the pins are floating.

The eighth bit of the device address is the read/write operation select bit. A read operation is initiated if this bit is high and a write operation is initiated if this bit is low. Upon a compare of the device address, the Chip will output a zero. If a compare is not made, the device will return to a standby state.

Data Security

24C02 has a hardware data protection scheme that allows the user to write protect the whole memory when the WCB pin is at Vcc.

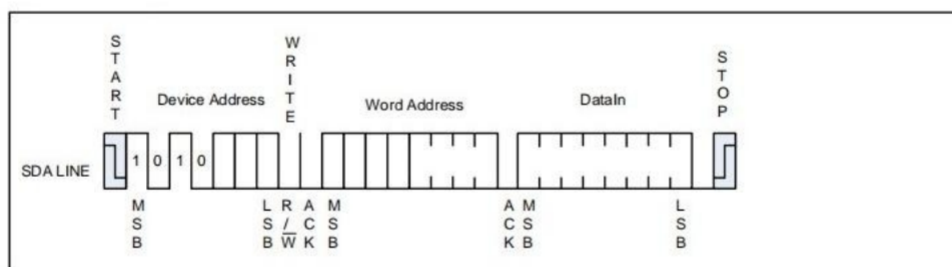
Instructions

Write Operations

Byte Write

A write operation requires an 8-bit data word address following the device address word and acknowledgment. Upon receipt of this address, the 24C02 will again respond with a “0” and then clock in the first 8-bit data word. Following receipt of the 8-bit data word, the 24C02 will output a “0” and the addressing device, such as a micro controller, must terminate the write sequence with a stop condition. And then the 24C02 enters an internally timed write cycle, all inputs are disabled during this write cycle and the 24C02 will not respond until the write is complete (see Figure ③).

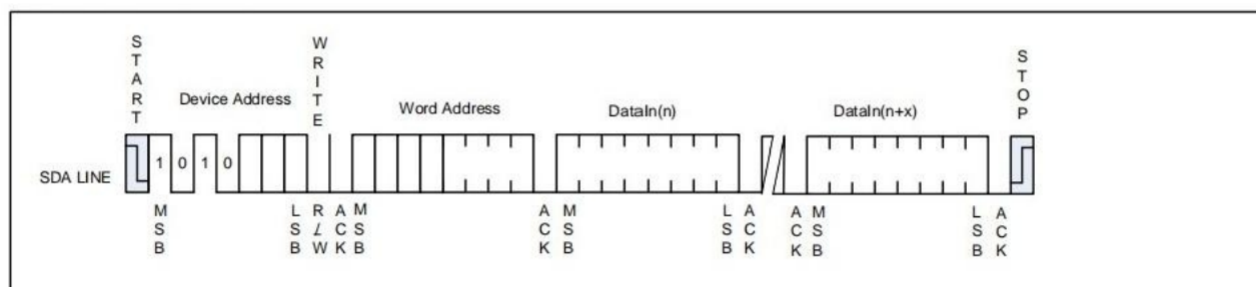
Figure Byte Write



Page Write

A page write is initiated the same as a byte write, but the master does not send a stop condition after the first data word is clocked in. Instead, after the 24C02 acknowledges receipt of the first data word, the master can transmit more data words. The 24C02 will respond with a “0” after each data word received. The microcontroller must terminate the page write sequence with a stop condition.

Figure Page Write



The lower three bits of the data word address are internally incremented following the receipt of each data word. The higher data word address bits are not incremented, retaining the memory page row location. When the word address, internally generated, reaches the page boundary, the following byte is placed at the beginning of the same page. If more than eight data words are transmitted to the 24C02, the data word address will roll-over, and previous data will be overwritten. The address roll-over during write is from the last byte of the current page to the first byte of the same page.

Acknowledge Polling

Once the internally timed write cycle has started and the 24C02 inputs are disabled, acknowledge polling can be initiated. This involves sending a start condition followed by the device address word. The read/write bit is representative of the operation desired. Only if the internal write cycle has completed will the 24C02 respond with a “0”, allowing the read or write sequence to continue.

Read Operations

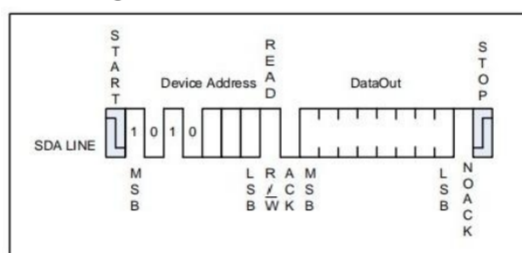
Read operations are initiated the same way as write operations with the exception that the read/write select bit in the device address word is set to “1”. There are three read operations: Current Address Read; Random Address Read and Sequential Read.

Current Address Read

The internal data word address counter maintains the last address accessed during the last read or write operation, incremented by one. This address stays valid between operations as long as the chip power is maintained. The address roll-over during read is from the last byte of the last memory page to the first byte of the first page.

Once the device address with the read/write select bit set to “1” is clocked in and acknowledged by the 24C02, the current address data word is serially clocked out. The micro controller does not respond with an input “0” but does generate a following stop condition (see Figure ④).

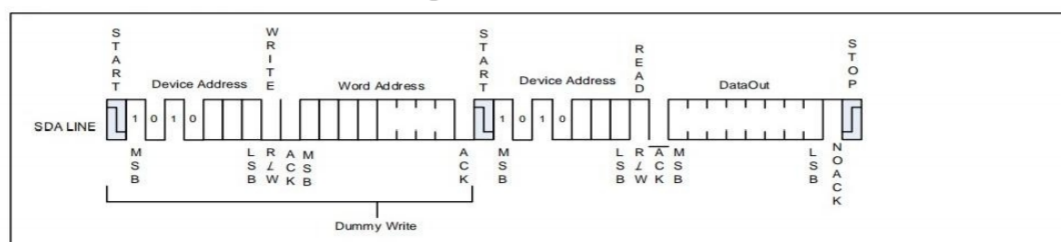
Figure Current Address Read



Random Read

A Random Read requires a "dummy" byte write sequence to load in the data word address. Once the device address word and data word address are clocked in and acknowledged by the 24C02, the micro controller must generate another start condition. The micro controller now initiates a Current Address Read by sending a device address with the read/write select bit high. The 24C02 acknowledges the device address and serially clocks out the data word. The micro controller does not respond with a “0” but does generate a following stop condition (see Figure ⑤).

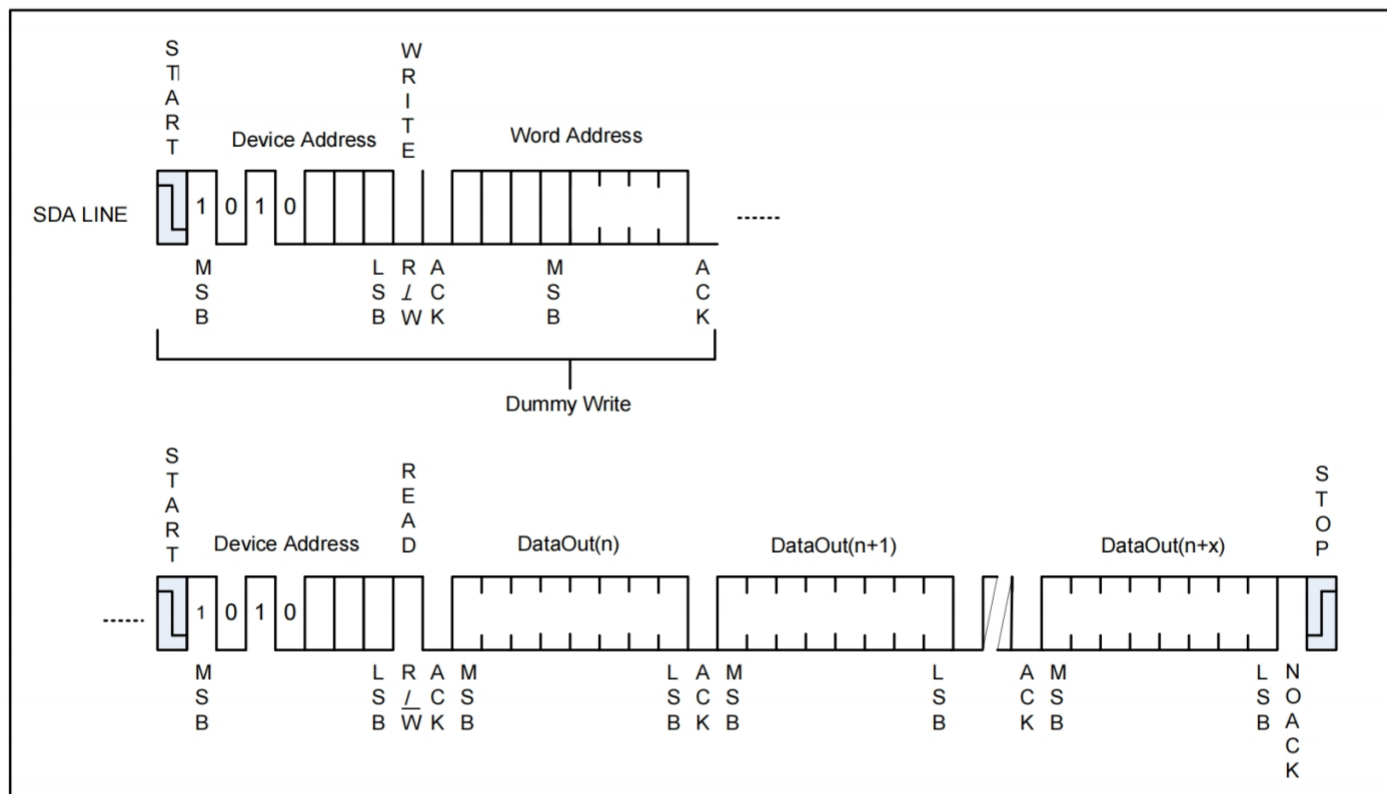
Figure Random Read



Sequential Read

Sequential Reads are initiated by either a Current Address Read or a Random Address Read. After the micro controller receives a data word, it responds with acknowledge. As long as the 24C02 receives acknowledge, it will continue to increment the data word address and serially clock out sequential data words. When the memory address limit is reached, the data word address will roll-over and the Sequential Read will continue. The Sequential Read operation is terminated when the micro controller does not respond with a "0" but does generate a following stop condition

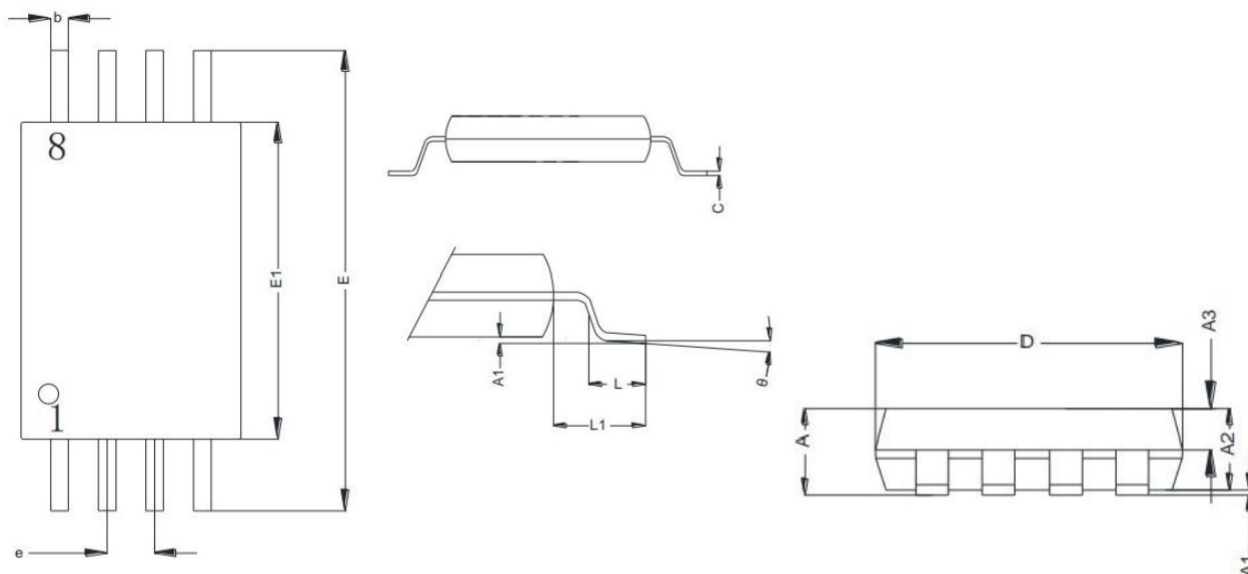
Figure Sequential Read



Outline Dimensions

TSSOP-8

Unit: mm



Symbol	Min	Typ	Max
A			1.200
A1	0.050	-	0.150
A2	0.900		
A3	0.390	0.440	0.490
b	0.200		0.280
C	0.090		0.200
D	2.900	3.000	3.100
E	6.200	6.400	6.600
E1	4.300	4.400	4.500
e		0.650	
L	0.450	-	0.750
L1		1.000	-
θ	0		8°

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