GD5F1GM9UE vs. GD5F1GM7UE

3V 1GBIT SPI NAND FLASH MEMORY

Introduction

This application note introduces the related notices about comparison between GD5F1GM9UE and GD5F1GM7UE. The document only highlights the main similarities and differences. The comparison covers the general features, performance, command sets and device ID. For more detailed information, please refer to the specific datasheets as listed on the chapter of references.

General Features

Operating Condition Comparison

The Operating Condition Comparison Table below lists the common features of GD5F1GM9UE and GD5F1GM7UE.

Table1 Operating Condition Comparison Table

Feature		GD5F1GM9UE	GD5F1GM7UE
Operating Voltage Range		2.7V ~ 3.6V	
SPI mode		x1, x2, x4	
Operating Temperature		-40 to 85 ℃ -40℃~105℃	-40 to 85 ℃ -40℃~105℃
Architecture	Memory Cell Organization	1024 blocks	
	Block size	(128K+8K) bytes	
	Page Size with ECC Off	(2K+128) bytes	
	Page Size with ECC On	(2K+64) bytes	
Standard/Dual/Quad SPI	3V	166MHz	133MHz
For DTR Quad SPI	3V	133MHz	104MHz
Low Power Consumption	maximum active current (CR mode)	50mA	N/A
Feature		**GD5F1GM9UE**	**GD5F1GM7UE**
Read CASN Page		Support	N/A
Page read time（ maximum ）		150us	120us

Internal ECC		8bits/528byte	8bits/528byte
OTP Region Size		20K-Byte	20K-Byte
OTP Region Address		Page 02H-0BH	Page 02H-0BH
Advanced Feature for NAND	Factory good block	Block0~Block255	Block 0
	Continuous Read	Support	N/A
	Cache Read（31h/30h/3Fh）	Support	N/A
	Bad Block Management-(A1H)	Support	N/A
	Read Bad Block Link Table(A5H)	Support	N/A
	Auto Load Next Page(AL bit)	Support	N/A
	Data Learning Pattern DLP	Support	N/A
Package	WSON8(8*6mm)	Support	Support
	WSON8(6*5mm)	Support	Support
	TFBGA24(5*5Ball Array)	Support	Support

Performance Comparison

The comparison table of main parameters is shown as table2.

Table2 Performance Comparison Table

(T=-40°C~85°C/105℃, VCC= 2.7~3.6V)

Parameters		GD5F1GM9UE				GD5F1GM7UE			
		GigaDevice				GigaDevice			
Item	Description	Min	Typ.	Max.	Unit.	Min.	Typ.	Max.	Unit.
DC Parameters									
I_{CC2}	Operating Current (Read) In Normal Read CLK=0.1VCC / 0.9VCC at 166MHz, Q=Open(*1,*2,*4 I/O)	-	15	30	mA	/	/	/	/
I_{CC2}	Operating Current (Read) In Continuous Read CLK=0.1VCC / 0.9VCC at 166MHz, Q=Open (*1, *2, *4 I/O)	-	35	50	mA	/	/	/	/
I_{CC2}	Operating Current (Read) CLK=0.1VCC / 0.9VCC at 133MHz, Q=Open(*1,*2,*4 I/O)	/	/	/	/	-	15	30	mA
I_{CC2}	Operating Current (Read) In Continuous Read CLK=0.1VCC / 0.9VCC at 133MHz, Q=Open(*1,*2,*4 I/O)	-	30	50	mA	/	/	/	/
AC Parameters									
Item	Description	Min	Typ.	Max.	Unit.	Min.	Typ.	Max.	Unit.
FC1	Serial Clock Frequency	-	-	166	MHz	-	-	133	MHz
FC_DTR	Serial Clock Frequency for DTR	-	-	133	MHz	-	-	104	MHz
tCH	Serial Clock High Time	2.7	-	-	ns	3.375	-	-	ns
tCL	Serial Clock Low Time	2.7	-	-	ns	3.375	-	-	ns
tSLCH	CS# Active Setup Time	5	-	-	ns	5	-	-	ns
tSHSL/tCS	CS# High Time	15	-	-	ns	20	-	-	ns
tSHQZ	Output Disable Time	-	-	10	ns			20	ns
tCLQX	Output Hold Time	1	-	-	ns	2	-	-	ns
tCHQX	Output Hold Time (DTR Only)	1	-	-	ns	2			ns

tHLCH	Hold# Low SetupTime (relative to Clock)	4	-	-	ns	5	-	-	ns
tHHCH	Hold#High SetupTime (relative to Clock)	4	-	-	ns	5	-	-	ns
tCHHL	Hold# High Hold Time (relative to Clock)	2	-	-	ns	5	-	-	ns
tCHHH	Hold# Low Hold Time (relative to Clock)	2	-	-	ns	5	-	-	ns
tHHQX	Hold# High To Low-Z Out	-	-	10	ns	-	-	15	ns
tCLQV	Clock Low To Output Valid**(**10pf**)**	-	-	6	ns	-	-	-	ns
tCLQV	Clock Low To Output Valid**(**30pf)	-	-	7	ns	-	-	7	ns
tCHQV	Clock High To Output Valid (DTR Only) **(**10pf)	-	-	6	ns	-	-	-	ns
tCHQV	Clock High To Output Valid (DTR Only) **(**30pf**)**	-	-	7	ns	-	-	7	ns
tQSV	Clock transient to DQS valid time	Align to 30pF tCLQV			ns	/	/	/	/
tDQSQ	SIO Valid Skew Related to DQS (TFBGA24, 12pF)	-	-	0.7	ns	/	/	/	/
tQHS	SIO Hold Skew Factor (TFBGA24, 12pF)	-	-	0.7	ns	/	/	/	/

Performance and Timming

Item	Description	Min	Typ.	Max.	Unit.	Min.	Typ.	Max.	Unit.
tRD_ECC	Read From Array with ECC	-	50	150	us	-	50	120	us
Fast RD_ECC	Read From Array with ECC (AL=1)	-	30	80	us	/	/	/	/
tCBSYR	Cache busy time for Cache Read	-	5	25	us	/	/	/	/
tCBSYR_ECC	Cache busy time for Cache Read with ECC	-	30	80	us	/	/	/	/

Command Sets Comparison

Main differences of command set are listed below. And for more details, please refer to the referenced Datasheet

Table3 Commands Set (Except Read Command in CR mode) of GD5F1GM9

Command Name	Byte 1	Byte 2	Byte 3	Byte 4	Byte 5	Byte 6	Byte 7
Cache Read Sequential	31h						
Cache Read Random	30h	A23-A16	A15-A8	A7-A0			
Cache Read Random	13h	A23-A16	A15-A8	A7-A0	31h		
Cache Read End	3Fh						
Last ECC failure Page Address	A9h	Dummy	D7-D0	D7-D0			
ECC Status Read	7Ch	Dummy	D7-D0				
Write Auto power-on Page	A2h	A23-A16	A15-A8	A7-A0			
Bad Block Management(Swap Blocks)	A1h	LBA	LBA	PBA	PBA		
Read Bad Block Link Table	A5h	Dummy	LBA0	LBA0	PBA0	PBA0	LBA1
Read From Cache with 4-Byte Address	0Ch	A15-A8	A7-A0	Dummy x3	D7-D0		
Read From Cache Dual Output with 4-Byte Address	3Ch	A15-A8	A7-A0	Dummy x3	(D7-D0) x2		
Read From Cache Quad Output with 4-Byte Address	6Ch	A15-A8	A7-A0	Dummy x3	(D7-D0) x4		
Read From Cache Dual IO with 4-Byte Address	BCh	A15-A8	A7-A0	Dummy x3	(D7-D0) x2		
Read From Cache Quad IO with 4-Byte Address	ECh	A15-A8	A7-A0	Dummy x5	(D7-D0) x4		
DTR Read From Cache Quad IO	EDh	A15-A8	A7-A0	Dummy x8	(D7-D0) x4		

Table4 Read Command in CR Mode1 (NR Mode=0, CRDC=0) of GD5F1GM9

Command Name	Byte 1	Byte 2	Byte 3	Byte 4	Byte 5	Byte 6	Byte 7
Read From Cache (NR Mode=0, CRDC=0)	03h	Dummy x3	(D7-D0)				
Fast Read From Cache (NR Mode=0, CRDC=0)	0Bh	Dummy x4	(D7-D0)				
Read From Cache with 4-Byte Address	0Ch	Dummy x5	(D7-D0)				
Read From Cache x 2(NR Mode=0, CRDC=0)	3Bh	Dummy x4	(D7-D0) x2				
Read From Cache x2 with 4-Byte Address	3Ch	Dummy x5	(D7-D0) x2				
Read From Cache x 4 (NR Mode=0, CRDC=0)	6Bh	Dummy x4	(D7-D0) x4				
Read From Cache x4 with 4-Byte Address	6Ch	Dummy x5	(D7-D0) x4				
Read From Cache Dual IO (NR Mode=0, CRDC=0)	BBh	Dummy x4	(D7-D0) x2				
Read From Cache Dual IO with 4-Byte Address	BCh	Dummy x5	(D7-D0) x2				
Read From Cache Quad IO (NR Mode=0, CRDC=0)	EBh	Dummy x6	(D7-D0) x4				
Read From Cache Quad IO with 4-Byte Address	ECh	Dummy x7	(D7-D0) x4				
DTR Read From Cache Quad IO (NR Mode=0, CRDC=0)	EDh	Dummy x11	(D7-D0) x4				
DTR Read From Cache Quad IO with 4-Byte Address(NR Mode=0, CRDC=0)	EEh	Dummy x12	(D7-D0) x4				

Table5 Read Command in CR Mode2 (NR Mode=0, CRDC=1) of GD5F1GM9

Command Name	Byte 1	Byte 2	Byte 3	Byte 4	Byte 5	Byte 6	Byte 7
Read From Cache (NR Mode=0, CRDC=1)	03h	Dummy x3	(D7-D0)				
Fast Read From Cache (NR Mode=0, CRDC=1)	0Bh	Dummy x3	(D7-D0)				
Read From Cache with 4-Byte Address	0Ch	Dummy x5	(D7-D0)				
Read From Cache x 2(NR Mode=0, CRDC=1)	3Bh	Dummy x3	(D7-D0) x2				

Read From Cache x2 with 4-Byte Address	3Ch	Dummy x5	(D7-D0) x2				
Read From Cache x 4 (NR Mode=0, CRDC=1)	6Bh	Dummy x3	(D7-D0) x4				
Read From Cache x4 with 4-Byte Address	6Ch	Dummy x5	(D7-D0) x4				
Read From Cache Quad Output with 4-Byte Address (NR Mode=0, CRDC=1)	BBh	Dummy x3	(D7-D0) x2				
Read From Cache Dual IO with 4-Byte Address	BCh	Dummy x5	(D7-D0) x2				
Read From Cache Dual IO with 4-Byte Address(NR Mode=0, CRDC=1)	EBh	Dummy x4	(D7-D0) x4				
Read From Cache Quad IO with 4-Byte Address	ECh	Dummy x7	(D7-D0) x4				
Read From Cache Quad IO with 4-Byte Address(NR Mode=0, CRDC=1)	EDh	Dummy x10	(D7-D0) x4				
DTR Read From Cache Quad IO with 4-Byte Address(NR Mode=0, CRDC=1)	EEh	Dummy x12	(D7-D0) x4				

Table6 Different Read ID Commands of GD5F1GM7 and GD5F1GM9

Command Name	Byte 1	Byte 2	Byte 3	Byte 4	Byte 5	Byte 6	Byte 7
Read ID(GD5F1GM7)	9Fh	Dummy	MID	DID			
Read ID(GD5F1GM9)	9Fh	Dummy	MID	DID1	DID2		

Features Sets Comparison

The features table of GD5F1GM9UE and GD5F1GM7UE are shown as table5 and table6. For more details, please refer to the referenced Datasheet.

Table 7 Features Table of GD5F1GM9

Register	Addr.	7	6	5	4	3	2	1	0
Protection	A0h	BRWD	Reserved	BP2	BP1	BP0	INV	CMP	Reserved
Feature	B0h	OTP_PRT	OTP_EN	Reserved	ECC_EN	NR	Reserved	Reserved	QE
Status	C0h	Reserved	BBLS	ECCS1	ECCS0	P_FAIL	E_FAIL	WEL	OIP
Feature	D0h	Reserved	DS_S1	DS_S0	Reserved	DLP-EN	DC	Reserved	Reserved
Status	F0h	Reserved	Reserved	ECCSE1	ECCSE0	BPS	Reserved	Reserved	CBSY
Feature	60h	Reserved	Reserved	Reserved	Reserved	BPL	CRDC	AL	Reserved*
Feature	10h	BFT3	BFT2	BFT1	BFT0	Reserved	Reserved	Reserved	Reserved

Table8 Features Table of GD5F1GM7

Register	Addr.	7	6	5	4	3	2	1	0
Protection	A0h	BRWD	Reserved	BP2	BP1	BP0	INV	CMP	Reserved
Feature	B0h	OTP_PRT	OTP_EN	Reserved	ECC_EN	BPL	Reserved	Reserved	QE
Status	C0h	Reserved	Reserved	ECCS1	ECCS0	P_FAIL	E_FAIL	WEL	OIP
Feature	D0H	Reserved	DS_S1	DS_S0	Reserved	Reserved	Reserved	Reserved	Reserved
Status	F0h	Reserved	Reserved	ECCSE1	ECCSE0	BPS	Reserved	Reserved	Reserved

Normal Read and Continuous Read Operation

Only the GD5F1GM9UE provides two different modes for read operations, Normal Read Mode (NR=1) and Continuous Read Mode (NR=0). For more details, please refer to the referenced Datasheet.

Table9 Normal Read & Continuous Read Data Out Structure

NR	ECC_EN	Read Mode	Internal ECC Status	Data Output Structure
1	0	Normal Read	NA	2048+128
1	1	Normal Read(Default)	Page based	2048+128
0	0	Continuous Read	NA	2048
0	1	Continuous Read	Page based	2048

Table10 Normal Read & Continuous Read Mode Function

NR	Read Mode	Cache Read Operation	Auto Load Next Page Feature(AL bit)
1(Default)	Normal Read	Available	Available
0	Continuous	NA	NA

Read CASN Page

Only the GD5F1GM9 support the CASN page function, The Read CASN Page function retrieves the data structure that describes the chip's organization, features, timing and other behavioral parameters. This data structure enables the host processor to automatically recognize the SPI-NAND Flash configuration of a device. The whole data structure is repeated at least three times. For more details, please refer to the referenced Datasheet.

Bad Block Management (A1H) and Read Bad Block Link Table(A5H)

Only the GD5F1GM9 support the Bad Block Management (A1H) and Read Bad Block Link Table(A5H). For more details, please refer to the referenced Datasheet(chapter 15.1 and 15.2).

Other new difference of GD5F1GM9

Only the GD5F1GM9 support : Write power-on Page Address(A2h)、Read ECC Warning Page Address(A9h) and Read ECC Status Command (7Ch). For more details, please refer to the referenced Datasheet(chapter 16、17 and 18).

Read ID

Table11 READ ID Table of GD5F1GM9

Part No	MID	DID1	DID2
GD5F1GM9UE	C8h	91h	01h

Table12 READ ID Table of GD5F1GM7

Part No	MID	DID1
GD5F1GM7UE	C8h	91h

REFERENCE

Datasheet	Location	Date Issued	Versions
GD5F1GM9	GigaDevice Website	March 28, 2025	Rev 1.0
GD5F1GM7	GigaDevice Website	July 11, 2024	Rev 1.5

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