钍地半导体
Tudi Semiconductor

Product Specification

TUDI-AD7715

3 V/5 V, 16-Bit, Sigma-Delta ADC

网址 www.sztdbdt.com

用芯智造·卓越品质

semiconductor device manufacturer

- Design
- research and development
- production
- and sales

Features

- á Charge-balancing ADC
- á 16-bits no missing codes
- á 0.003% nonlinearity
- á Programmable gain front end
- á Gains of 1, 2, 32 and 128
- á Differential input capability
- á Three-wire serial interface
- á Ability to buffer the analog input
- á 3 V (AD7715-3) or 5 V (AD7715-5) operation
- á In power-off mode, the maximum current is 8 μA
- á Low-pass filter with programmable output update

16-lead SMD/PDIP/TSSOP

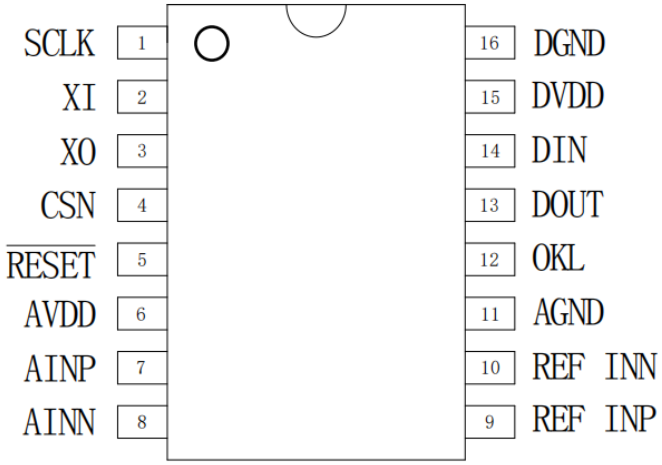


Figure 1. Pin Diagram

Description

The AD7715 is a complete low-frequency measurement application analog front end. This device can accept low-level input directly from sensors or transducers and output a serial digital word. Sigma-delta conversion technology is used to achieve performance up to 16 bits with no missing codes. The signal is applied to a proprietary programmable gain front end based on an analog modulator. The modulator output is processed by an on-chip digital filter. The first pole this digital filter can be programmed through an on-chip control register, allowing adjustment of the filter cutoff frequency and the output update rate.

The AD7715 has differential inputs and a differential reference input. It is powered from a single supply (3 V or 5 V). It can handle unipolar input signal ranges including 0 mV 20 mV, 0 mV to 80 mV, 0 V to 1.25 V, and 0 V to 2.5. It can also handle bipolar input signal ranges including ±20 mV, ±80 mV, ±1.25 V, and ±2.5 V. bipolar ranges are referenced to the negative input of the differential analog inputs. Thus, the AD7715 performs all of the signal conditioning and conversion for single-channel systems.The AD7715 is well suited for use in smart, microcontroller , or DSP-based systems. It has a serial interface that can be configured for three- operation. The gain setting, signal polarity, and update rate selection can be configured in software via the input serial port. The device contains self-calibration and system calibration options to gain and offset errors in the device itself or in the system. The CMOS architecture ensures very low power dissipation, and a low-power mode reduces the standby current to a 10 μA. The device is available in a 16-pin, package (PDIP) package (SOIC_W) and TSSOP package

Pin description

Pin name	Pin number	I/0	Function
SCLK	1	I	Serial clock input
XI	2	I	Clock input,crystal oscillator,or external clock
XO	3	0	Clock out
CSN	4	I	Select the pin,input low level valid
$\overline{\text{RESET}}$	5	I	Reset,low level active
AVDD	6	I	Analog power supply
AINP	7	I	Positive input terminal of differential analog channel
AINN	8	I	Differential analog negative input terminal of channel
REF INP	9	I	Positive input terminal of reference
REF INN	10	I	Negative input terminal of reference
AGND	11	I	Simulated ground
OKL	12	0	AD conversion completed logic output flag
DOUT	13	0	Serial data output terminal
DIN	14	I	Serial data input terminal
DVDD	15	—	Digital power supply
DGND	16	—	Digital ground

NOTE:

Integrated circuits, as static-sensitive devices, can easily generate a large amount of static electricity in dry seasons or dry environments. Electrostatic discharge (D) can damage integrated circuits, and TUDI Semiconductors recommends taking all appropriate preventive measures for integrated circuits. Incorrect soldering operations can lead to ESD damage performance degradation, making the chip unable to work normally.

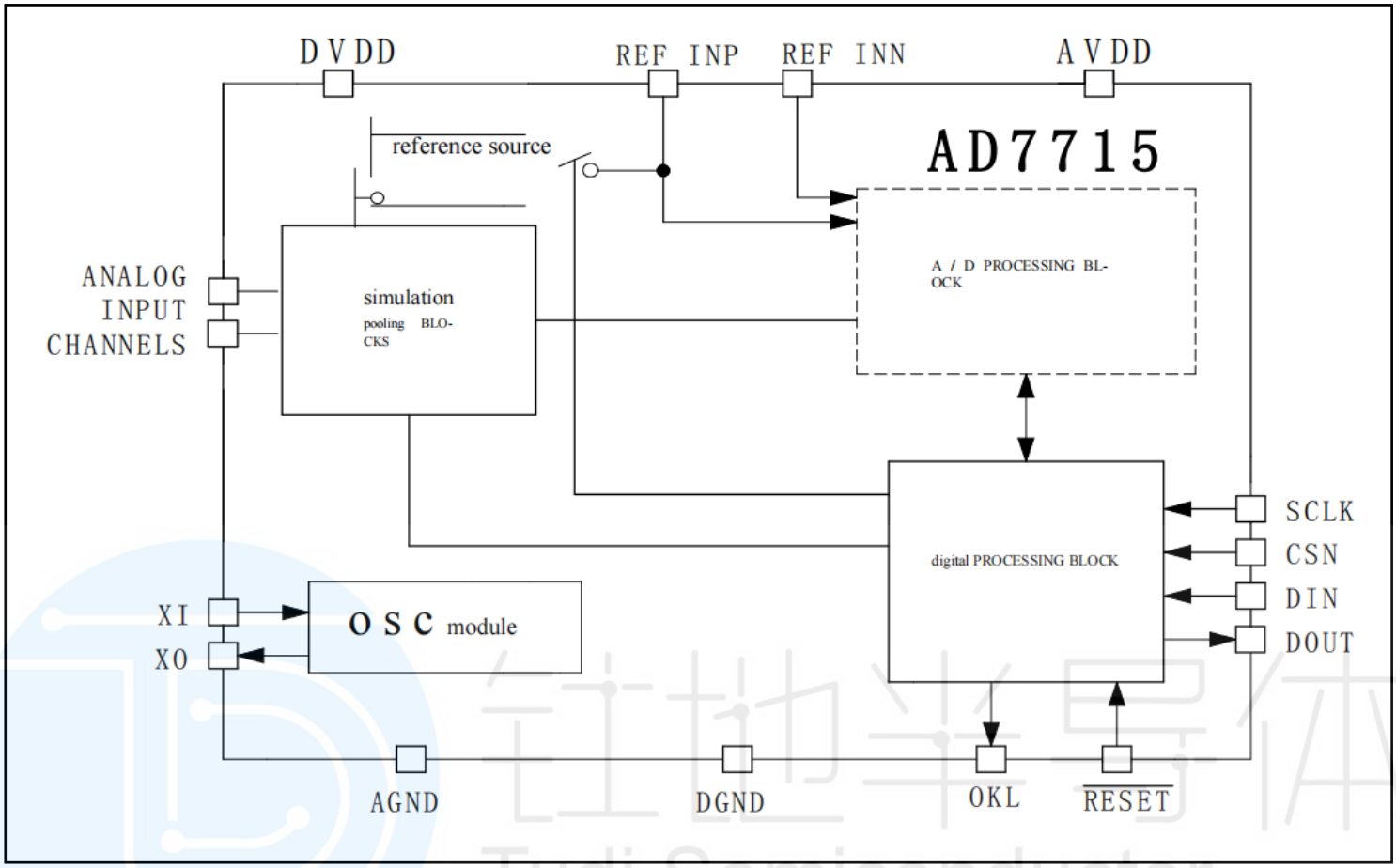


Figure 2.Structure Diagram

Communication interface

AD7715uses serial communication to complete the read/write operation of the register. The serial interface includes five signal interfaces: SCLK, DIN, DOUT, OKL and CSN. The data transmission sequence is high bit first. DIN: Data input port, where data is written during the clock rising edge.

DOUT: Data output port, outputs data on the clock's falling edge.

SCLK: Serial clock input for read and write operations.

OKL: An indicator signal that signals whether the ADC result register data is ready for update. A low level indicates the ADC data has been converted and can be read from the ADC result register. A high level indicates the ADC is in the process of conversion or updating, and the data cannot be read.

CSN: The selected signal. The register can only be read or written when CSN is first pulled low to enable it. After the operation, CSN must be pulled high

Time sequence waveform diagram

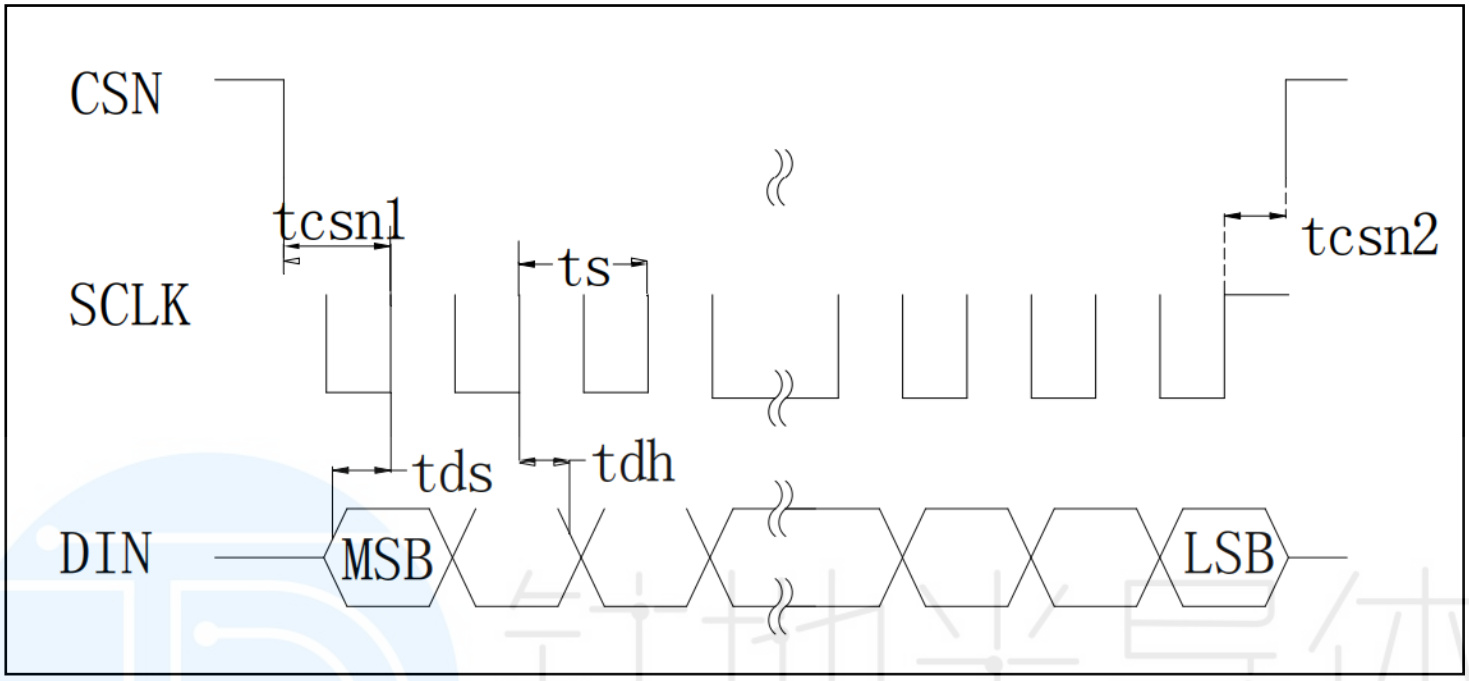


Figure 3 Write Sequence

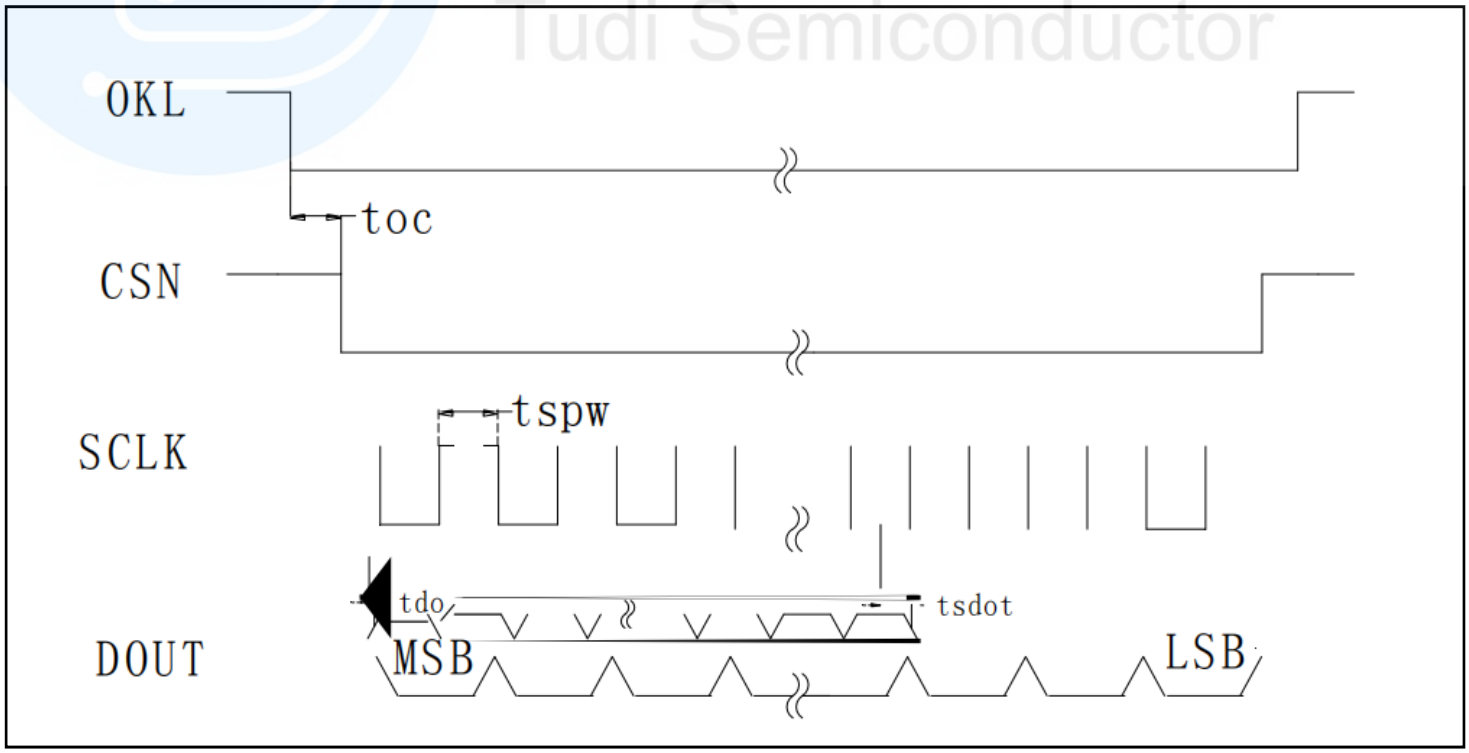


Figure 4 Reading Sequence

Temporal characteristic

Parameter name	Parameter Symbol	Test condition	Least value	Represetative value	Crest value	Unit
Master clock frequency	fCLKIN	—	400		2500	kHz
Master clock low level time	Tlow	tCIKIN=1/ fcIKIN	0.4*tcLKIN			ns
Master clock high level time	Thigh		0.4*tcIKIN			ns
OKL high pulse	$t_。$			500*tcLKIN		ns
$\overline{\text{RESET}}$ pulse width	t_R		100			ns
Read write sequence						
CSN↓→SLCK First rising edge	Tcsnl		120			ns
Slck↓→DIN valid sampling interval	tdo	VD=5V	0	—	80	ns
		Vm=3V	0	—	100	ns
SCLK个→CSN ↑time	Tcsn2		0			ns
Sclk ↑bus withdrawal time	tsout	Vm=5V	10		60	ns
		V=3V			100	ns
DIN valid→SCLK ↑acquisition time	tds		30			ns
DIN valid→SCLK ↑hold time	tdh		20			ns
OKL↓→CSN ↓time	toc		0			ns
Clock pulse width high(low)level	tspw		100			ns

Register Description

MSB	B7	0/OKL	The chip retains the bit.The default is "0".Write "0"to write,do not write "1".			
	B6	ZERO	Ensure correct operation.This field must be zero.Otherwise,the device operation will not be specified.			
	B5	RSAD1	Register address bit		00:Communication register 01:Configure the register 10:Test Register 11:ADC result register	
	B4	RSAD0				
	B3	R/WL	Read/Write select bit:"0"indicates write operation,"1"indicates read operation.			
	B2	PD	Write "1"for power-off mode.Write"0"for normal operation mode.			
	Gain configuration		1	2	32	128
	B1	PGA_1	0	0	1	1
LSB	B0	PGA_1	0	1	0	1

Table 1 Communication Register 8-Bit Description Power-on Reset State: 00 Hex

MSB	B7	MDH	Work mode selection bit: 00:Normal working mode 01:For self-calibration 10:Zero Point Offset System Correction 11:System calibration for gain coefficient							
	B6	MDL								
	OSC clock		1MHz				2.4576MHz			
	Update rate		20Hz	25Hz	100Hz	200 Hz	50 Hz	60Hz	250 Hz	500 Hz
	Filter-3dB cutoff Frequency		5.24Hz	6.55Hz	26.2 Hz	52.4 Hz	13.1 Hz	15.7 Hz	65.5 Hz	131 Hz
	B5	OSC	0	0	0	0	1	1	1	1
	B4	DRH	0	0	1	1	0	0	1	1
	B3	DRL	0	1	0	工	0	1	0	1
	B2	U/BL	Unipolar mode:Output OxFFFFH when"1"is applied with FSR,where ZERO=0x0000H and-FSR=0x0000H.Bipolar mode:Output OxFFFFH when "0"is applied with FSR,where ZERO=0x8000H and-FSR=0x0000H.							
	B1	BUFEN	Enable the input buffer."0"disables it,while "1"enables it.The internal buffer is short-circuited.							
LSB	B0	SYNC	Filter synchronization defaults to 0.If"1"is set,it resets both the modulator and digital filter.It collects analog input samples from a known time point until system synchronization is achieved.							

Table 2 Configuration Register 8-Bit Description Power-Up/Reset State: 28 Hex

The AD7715contains four registers, with the communication register being the primary focus. All operations on other registers must first affect the communication register. If the chip is reset after sending more than 32 pulses during a high-level DIN write operation, it will reset.

ADC result register is a 16-bit read-only register used to store the latest conversion results . The high bits are read first.Power on / reset state: 0000 Hex.

Test register is an 8-bit register used to test the device. Users are advised not to modify it arbitrarily. (Automatically set to all 0s during power-on or reset).Power-on/Reset state: 00 Hex

Application Circuit

The basic circuit diagram of the AD7715(Figure 5) shows an analog voltage of +5V/3V, with the precise +2.5V/1.225V reference voltage serving as the device's reference. For digital signals, the device operates in three-wire mode, where CSN is grounded.

The quartz crystal provides the primary clock source. The resistance R is 1MΩ, and the capacitance values of C1 and C2 typically range from 30pF to 50pF.

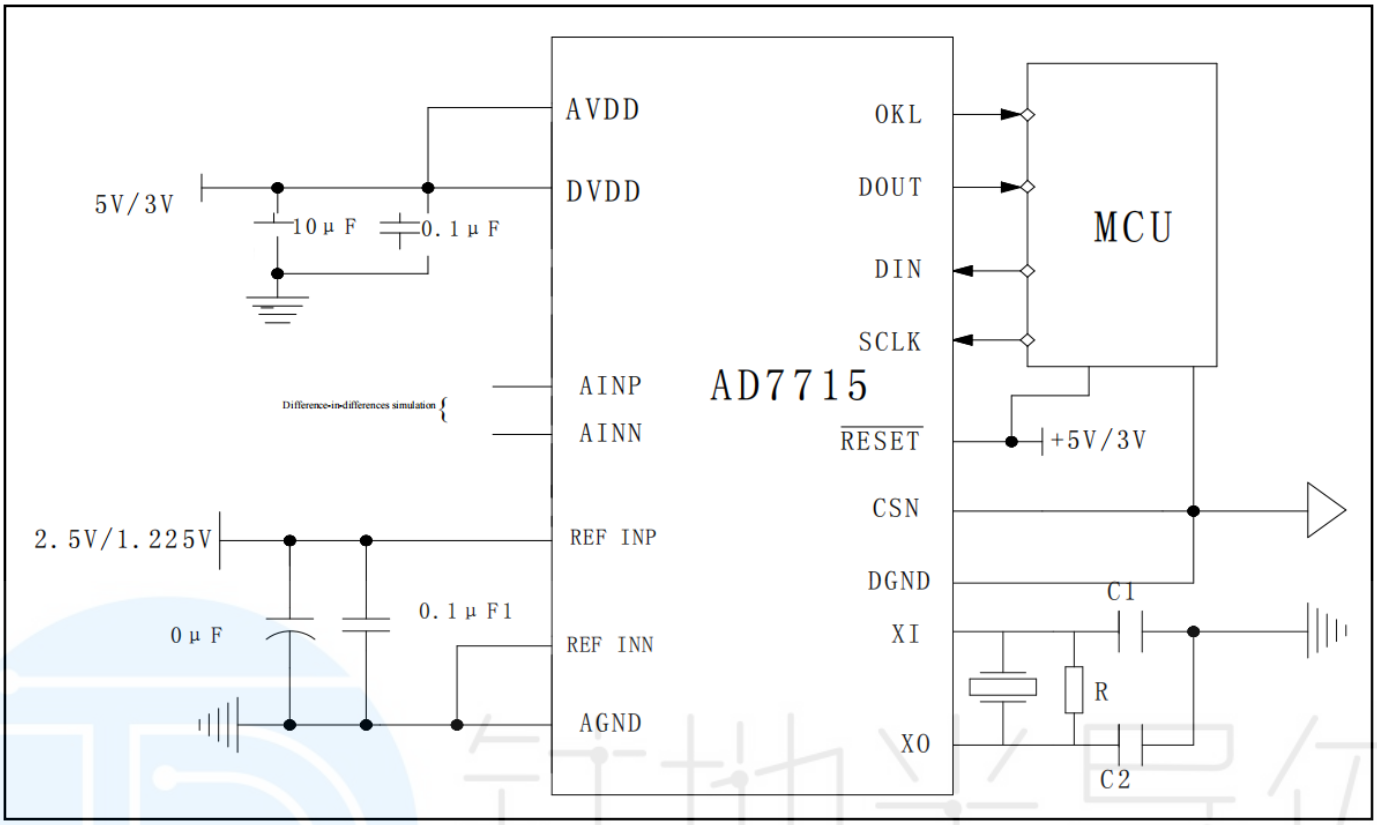


Figure 5: Circuit Diagram of AD7715

Reset and power-off mode

The reset input circuit resets all logic, digital filters and analog modulators, while setting all on-chip registers to their default state. The reset is performed by pulling the $\overline{\text{RESET}}$ pin low or sending the $\overline{\text{RESET}}$=0 command.
The PD bit in the communication register allows users to set the device to power-down mode for reduced power consumption. After exiting power-down mode, the device returns to normal operation with all registers retaining their pre-power-down state, eliminating the need for reconfiguration.

External Reference Voltage

REFINP and REFINN provide differential reference voltage functions for AD7715. When operating at 5V/3V supply voltages, the reference voltage is set to +2.5V/1.225V. If the reference voltage drops below 1V, the device may still function but experiences increased output noise, resulting in performance degradation. Therefore, it is essential to maintain REFINP> REFINN to ensure proper device operation.

Error Correction

When environmental temperature, operating voltage, selected gain, filter notch, or single/ bipolar input range changes, the device must be calibrated to ensure accurate analog-to-digital conversion. The AD7715 offers multiple calibration options programmable via the MDH and MDL bits in the configuration register. This calibration effectively eliminates bias and gain errors in the device.

self-correcting

When the auto-correct command is issued, the chip performs zero offset and gain coefficient corrections through the designated channel and set gain in the communication register. During zero offset correction, the specified input channel is automatically short-circuited (zero input). For gain coefficient correction, the specified input channel connects to the internal Vref voltage at the selected gain (full-scale). Throughout the correction process, the OKL remains high. When the OKL drops, it indicates the correction is complete, and the system automatically reverts to normal operation mode, i.e., MDH MDL=00 state.

system calibration

The system correction can correct the bias error and gain error of the chip and the system, because the system correction must be input signal after the input signal.
To Correct Zero Offset Error, the Input Must Be Set to a Differential Voltage of 0V, and the MDH and MDL Registers Must Be Configured to Write (1,0). The chip calculates the offset error of the system and gives compensation in the following work.
To Correct Gain Coefficient Errors, a Full Positive Input Voltage Must Be Applied, and the MDH and MDL Registers Must Be Set to (1,1).
The gain error correction is started. The gain error value of the system is calculated by the chip , and the compensation is given in the following work

Output Noise

Table 3, 5 show the output noise reference values generated when the analog input is short-circuited, for the device operating in buffer mode non-buffer mode, respectively, VDD = 5V, VDD = 3V, VREF = 2.5V/1.225V and the selectable update frequency at the -3dB frequency. Table 4, 6 show the resolution, respectively, for VDD = 5V, VDD = V. The resolution expressed by these numbers is given in effective number of bits.

	OSC frequency (MHz)	First-order Butterworth filter and O/P data rate(Hz)	—3 dB frequency(Hz)	Output noise level(μV)			
				Gain			
				1	2	32	128
BUFFEN=0	2.4576	50	13.1	4.1	2.1	0.66	0.6
	2.4576	60	15.72	5.1	2.5	0.7	0.62
	2.4576	250	65.5	110	49	3.6	1.7
	2.4576	500	131	550	285	22	4.7
	1	20	5.24	4.1	2.1	0.66	0.6
	1	25	6.55	5.1	2.5	0.7	0.62
	1	100	26.2	110	49	3.6	1.7
	1	200	52.4	550	285	22	4.7

Table 3 Relationship Between Output Noise, Gain, and Update Rate (5V Voltage)

	OSC frequency (MHz)	First-order Butterworth filter and O/P data rate(Hz)	—3 dB frequency(Hz)	Resolution (bits)			
				Gain			
				1	2	32	128
BUFFEN=0	2.4576	50	13.1	16	16	16	14
	2.4576	60	15.72	16	16	14	13
	2.4576	250	65.5	13	13	13	12
	2.4576	500	131	10	10	10	10
	1	20	5.24	16	16	16	14
	1	25	6.55	16	16	14	13
	1	100	26.2	13	13	13	12
	1	200	52.4	10	10	10	10

Table 4 Relationship Between Resolution, Gain, and Update Rate (at 5V Voltage)

	OSC frequency (MHz)	First-order Butterworth filter and O/P data rate(Hz)	—3 dB frequency(Hz)	Output noise level(μV)			
				Gain			
				1	2	32	128
BUFFEN=0	2.4576	50	13.1	3.8	2.4	1.0	0.9
	2.4576	60	15.72	5.1	2.9	1.0	0.9
	2.4576	250	65.5	50	25	2.6	2.0
	2.4576	500	131	270	135	9.7	3.3
	1	20	5.24	3.8	2.4	1.0	0.9
	1	25	6.55	5.1	2.9	1.0	0.9
	1	100	26.2	50	25	2.6	2.0
	1	200	52.4	270	135	9.7	3.3

Table 5 Relationship Between Output Noise, Gain, and Update Rate (at 3V Voltage)

	OSC frequency (MHz)	First-order Butterworth filter and O/P data rate(Hz)	—3 dB frequency(Hz)	Resolution(bits)			
				Gain			
				1	2	32	128
BUFFEN=0	2.4576	50	13.1	16	16	13	12
	2.4576	60	15.72	16	16	13	12
	2.4576	250	65.5	13	13	12	11
	2.4576	500	131	10	10	10	10
	1	20	5.24	16	16	13	12
	1	25	6.55	16	16	13	12
	1	100	26.2	13	13	12	11
	1	200	52.4	10	10	10	10

Table 6 Relationship Between Resolution, Gain, and Update Rate (at 3V Voltage)

Limiting Parameters (TA = +25 ° C, unless otherwise specified)

Parameter name	Parameter Symbol	Extreme	Unit
Logic power supply voltage	VDD	-0.3V ~ 7	V
Analog input voltage	Vin	-0.3 ~ VDD +0.3	V
Digital input voltage			
Digital output voltage	Vout	-0.3 ~ VDD +0.3	V
Operating temperature range	Topr	-40 ~ 85	℃
Storage temperature range	Tstg	-65 ~ 150	℃
Junction temperature	Tj	150	℃
Static electricity ESD	Human Body Model(HBM)	4000	V

Electric characteristics

VDD =+3V or +5V, REF INP=+1.225V or +2.5V; REF INN=GND, XI=2.4576MHz,TA =25, unless otherwise specified)

Parameter name	Test condition	Least value	Representative value	Crest value	Unit
Resolution ratio	Ensure the filter notch is below 60Hz		16		Bits
Integral nonlinearity			0	±0.003	%of FSR
Monopolar drift			0.5		μV/℃
Bipolar zero drift	PGA=1-4		0.5		μV/℃
	PGA=8-128		0.1		μV/℃
Full-scale drift			0.5		μV/℃
Gain error drift			0.5		ppm of FSR/℃
Bipolar negative full-scale error		0	±0.001	±0.003	%of FSR/℃
Bipolar negative full-scale drift			1		μV/℃

Electric characteristics(continuation)

VDD =+3V or +5V, REF INP=+1.225V or +2.5V; REF INN=GND, XI=2.4576MHz,TA =25, unless otherwise specified)

Parameter name	Test condition	Least value	Representative value	Crest value	Unit
AIN Absolute/Common Mode Voltage	BUFEN=0	-0.03		VDD+0.03	V
	BUFEN=1	0.05		VDD-1.5	V
AIN input currenton				1	nA
AIN acquisition capacitor				10	pF
AIN differential voltage	Unipolar input	0		VREp/GAIN	
	Bipolar input	-VRP/GAIN		VRBp/GAIN	
AIN stable sampling rate	Gain 1-4	GAIN×fcLKIK/64			
	Gain 8-128	fcLKx/8			
REFINP—REFINN difference	VDD=3V,Vref=1.225V	1		1.75	V
	VDD=5V,Vref=2.5V	1		3.5	
REF INN Input stable sampling rate			fcKIx/64		
Input voltage(excluding SCLK and XI)					
VIL	V=5V			0.8	V
	V=3V			0.4	V
VIH		2.0			V
Schmidt trigger input SCLK					
V+	V=5V	1.4		3	V
Vr		0.8		1.4	
V_1+—V_1_		0.4		0.8	
VT+	V=3V	1		2.5	
Vr_		0.4		1.1	
V+Vr_		0.375		0.8	
XI					
Input low level	V=5V			0.8	V
Input high level		3.5			
Input low level	V=3V			0.4	
Input high level		2.5			
Data output encoding	Unipolarity	Binary system			
	Bipolar	Biased binary code			

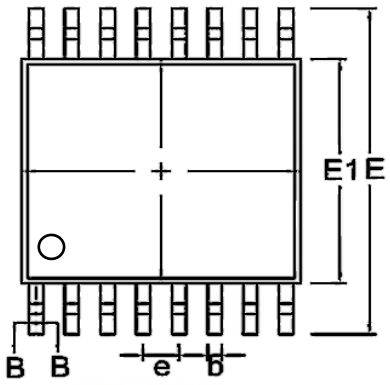
Power Parameter Characteristics

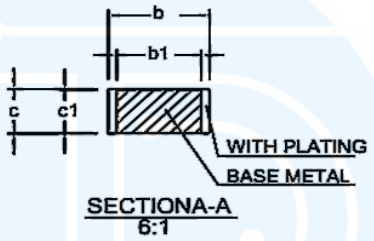
Parameter name	Test condition			Least value	Representative value	Crest value	Unit
	BUFEN	fcKIN(MHZ)	Gain				
When the power supply voltage is 3V,the digital IO interface or control port is grounded or connected to VDD(XI and OSCDIS=1)							
Source current	0	1	1-128			0.32	mA
	1	1	1-128			0.6	
	0	2.4576	1-4			0.4	
	0	2.4576	8-128			0.6	
	1	2.4576	1-4			0.7	
	1	2.4576	8-128			1.1	
When the power supply voltage is 5V,the digital IO interface or control port is grounded or connected to VDD(XI and OSCDIS=1)							
Source current	0	1	1-128			0.45	mA
	1	1	1-128			0.7	
	0	2.4576	1-4			0.6	
	0	2.4576	8-128			0.85	
	1	2.4576	1-4			0.9	
	1	2.4576	8-128			1.3	
Dropout mode current	V=5V,XI=0V /Vp ·					16	uA
	V=3V,XI=0V/V.					8	
Power supply rejection ratio	Supply voltage		Gain		86		dB
	VDD=3V		1				
	VDD=3V		2		78		
	VDD=3V		4		85		
	VDD=3V		8-128		93		
	VDD=5V		1		90		
	VDD=5V		2		78		
	VDD=5V		4		84		
	VDD=5V		8-128		91		

Order information

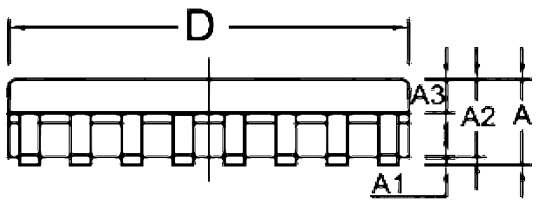
Order Number	Package	Package Quantity	Marking On The park	Temperature	Operating Voltage
AD7715ARZ-3REEL-TUDI	SMD16	Tape,Reel,2000	AD7715ARZ-3	- 40°C to 85°C	3V
AD7715ARUZ-3REEL-TUDI	TSSOP16	Tape,Reel,2000	AD7715ARUZ-3		
AD7715ANZ-3-TUDI	DIP16	Tube,25,A box of 1000	AD7715ANZ-3		
AD7715ARZ-5REEL-TUDI	SMD16	Tape,Reel,2000	AD7715ARZ-5		5V
AD7715ARUZ-5REEL-TUDI	TSSOP16	Tape,Reel,2000	AD7715ARUZ-5		
AD7715ANZ-5-TUDI	DIP16	Tube,25,A box of 1000	AD7715ANZ-5		

Package TSSOP16

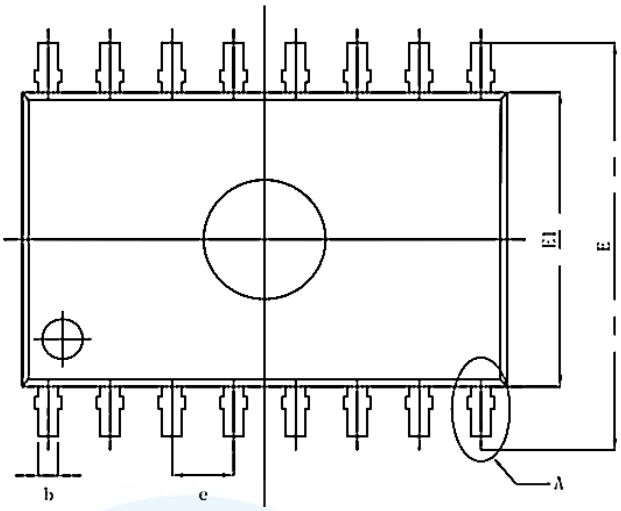


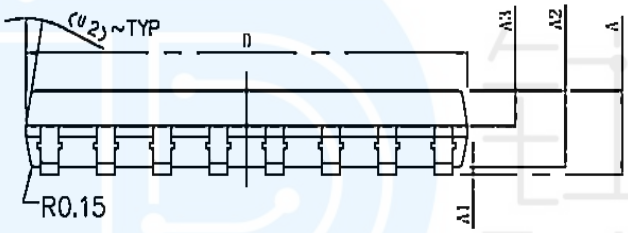


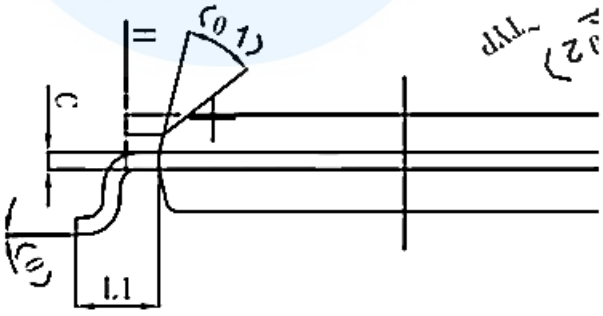
SIZE / SYMBOL	MIN./mm	TYP./mm	MAX./mm
A	--	--	1.20
A1	0.05		0.15
A2	0.90	1.00	1.05
b	0.20	--	0.30
b1	0.19	0.22	0.25
C	0.110	0.127	0.145
cl	0.12	0.13	0.14
D	4.86	4.96	5.06
E	6.20	6.40	6.60
E1	4.30	4.40	4.50
e	0.65BSC		
L	0.45	0.60	0.75
L1	1.00BSC		
	0°	--	8°

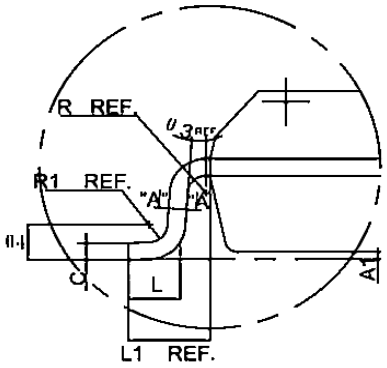


Package SMD16



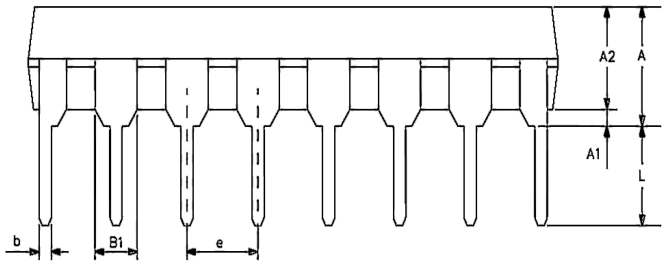


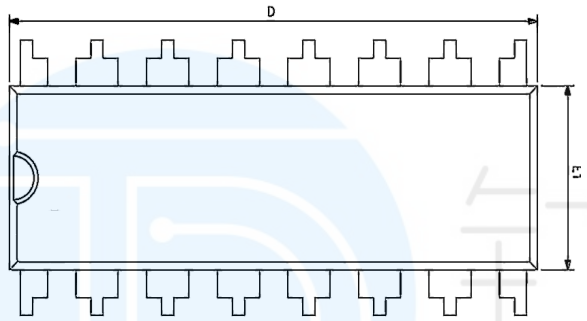


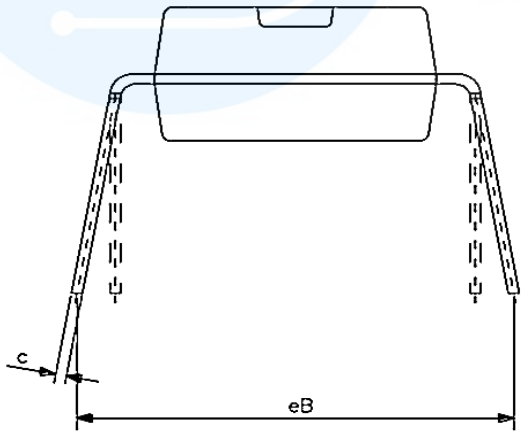


SIZE / SYMBOL	MIN./mm	MAX./mm
A	_	2.65
A1	0.10	0.30
A2	2.25	2.35
A3	0.97	1.07
D	10.10	10.50
E	10.26	10.60
E1	7.30	7.70
e	1.27BSC	
L	0.55	0.85
L1	1.4BSC	
H	0.345	0.365
R	0.20TYP	
R1	0.30TYP	
θ	0°	8°
θ1	45° TYP	
02	12° TYP	
03	0°	8°
04	0°	10°

Package DIP16







SIZE / SYMBOL	MIN./mm	MAX./mm
A2	3.20	3.60
A1	0.51	___
A	3.60	5.33
L	3.00	3.60
b	0.36	0.56
B1	1.52	
D	18.80	19.94
E1	6.20	6.60
e	2.54	
C	0.20	0.36
eB	7.62	9.30
R	0.20TYP	
R1	0.30TYP	
θ	0°	8°
θ1	45°TYP	
02	12°TYP	
03	0°	8°
04	0°	10°

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