

HMP5N150H6G

1500V N-Channel Planar Power MOSFET

Product features/产品特点

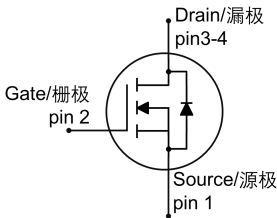
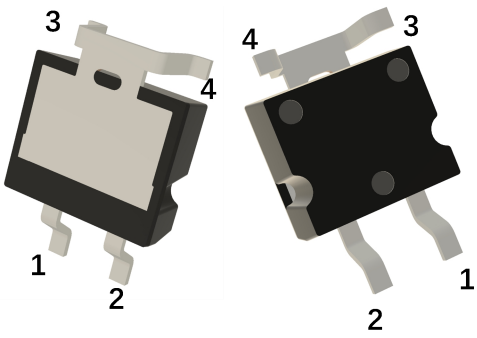
- Top side cooling technology
顶部散热技术
- Low Thermal Resistance
低热阻
- Fast Recovery Body Diode
快恢复体二极管
- Low Gate Charge Minimizes Switching Loss
低栅极电荷，有效降低开关损耗
- 100% UIS Tested
100% UIS测试
- Halogen free, RoHS compliant
无卤，符合RoHS

Applications/应用领域

- Adaptor
电源适配器
- Charger
充电器
- Switch Mode Power Supply
开关电源

Key performance parameters/关键性能参数

Parameter	Value	Unit
V_{DS}	1500	V
$R_{DS(on),typ}$	4.1	Ω
I_D	5	A



Package parameters/封装信息

Type/型号	Package/封装	Marking/标识	Packaging method/包装方式
HMP5N150H6G	TSC263-4L	HMP5N150G	800pcs-Tape&Reel/卷带包装(单卷800颗)

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1. Maximum ratings at $T_{vj}=25^{\circ}\text{C}$, unless otherwise specified.

最大额定值 默认 $T_{vj}=25^{\circ}\text{C}$ 除非另有说明

Table 1 Maximum ratings/最大额定值

Parameter 参数	Symbol 符号	Test conditions 测试条件	Value 值	Unit 单位
Drain-source voltage 漏极-源极电压	V_{DSS}	$T_{vj}\geq 25^{\circ}\text{C}$	1500	V
Maximum gate source voltage 栅源最大电压	$V_{GS,MAX}$		± 30	V
Drain current 连续漏极电流	I_D	$T_C=25^{\circ}\text{C}$ ¹	5	A
Peak drain current ² 峰值漏极电流	I_{DM}	$T_C=25^{\circ}\text{C}$	20	A
Continuous diode current ¹ 连续二极管电流	I_S		5	A
Peak diode current ² 峰值二极管电流	I_{SM}	$T_C=25^{\circ}\text{C}$	20	A
Avalanche energy, single pulse 单脉冲雪崩能量	E_{AS}	Single Pulse Avalanche Energy, $L=30\text{mH}$	450	mJ
Power dissipation 总耗散功率	P_{tot}	$T_C=25^{\circ}\text{C}$	735	W

1. Limited by $T_{vj}(\text{max})$ /受限于最大结温

2. Pulse width t_p limited by $T_{vj}(\text{max})$ /脉宽受限于最大结温



2. Thermal characteristics

热特性

Table 2 Thermal characteristics/热特性

Parameter 参数	Symbol 符号	Test conditions 测试条件	Value/值			Unit 单位
			Min.	Typ.	Max.	
Storage Temperature 存储温度	T_{stg}		-55		150	°C
Operating junction Temperature 工作结温	T_{vj}		-55		150	°C
Thermal resistance, junction-case 结-壳热阻	$R_{th(j-c)}$				0.17	°C/W
Thermal resistance, junction-ambient 结-环境热阻	$R_{th(j-a)}$			29		°C/W
Soldering temperature, reflow solderin 焊接温度, 回流焊	T_{sold}	reflow MSL1			260	°C



3. Electrical characteristics at $T_{vj}=25^{\circ}\text{C}$, unless otherwise specified.

电气特性 默认 $T_{vj}=25^{\circ}\text{C}$ 除非另有说明

Table 3 Static characteristics/静态特性

Parameter 参数	Symbol 符号	Test conditions 测试条件	Value/值			Unit 单位
			Min.	Typ.	Max.	
Drain-source breakdown voltage 漏源击穿电压	$V_{(BR)DSS}$	$I_D=250\mu\text{A}, V_{GS}=0\text{V}$	1500			V
Gate threshold voltage 门极开启阈值电压	$V_{GS(th)}$	$I_D=250\mu\text{A}, V_{DS}=V_{GS}$	2.5	3.5	4.5	V
Drain-source on-state resistance 漏极-源极导通电阻	$R_{DS(on)}$	$I_D=2.5\text{A}, V_{GS}=10\text{V}$		4.1	6.0	Ω
Zero gate voltage drain current 集电极-发射极漏电	I_{DSS}	$V_{DS}=1500\text{V}, V_{GS}=0\text{V}$			5	μA
Gate to source Leakage current 门极-源极漏电流	I_{GSS}	$V_{DS}=0\text{V}, V_{GS}=30\text{V}$			100	nA
		$V_{DS}=0\text{V}, V_{GS}=-30\text{V}$	-100			
Forward transconductance 正向跨导	g_{fs}	$I_D=1.5\text{A}, V_{DS}=15\text{V}$		3.1		S
Integrated gate resistor 内部门极电阻	R_G	$f=1\text{MHz}$		1.8		Ω

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Table 4 Dynamic characteristics/动态特性

Parameter 参数	Symbol 符号	Test conditions 测试条件	Value/值			Unit 单位
			Min.	Typ.	Max.	
Input capacitance 输入电容	C_{iss}	$V_{DS}=25V$, $V_{GS}=0V$, $f=1MHz$		2400		pF
Output capacitance 输出电容	C_{oss}			120		
Reverse transfer capacitance 反向传输电容	C_{rss}			8.6		
Total gate charge 总栅极电荷	$Q_{G(tot)}$	$V_{DD}=750V$, $I_D=5A$, $V_{GS}=0/10V$		52		nC
Gate source charge 栅-源极电荷	Q_{GS}			11		
Gate-drain charge 栅-漏极电荷	Q_{GD}			19		
Turn-on delay time 开启延迟时间	$t_{d(on)}$	$V_{DD}=750V$, $I_D=3A$, $V_{GS}=0/10V$, $R_{G(ext)}=4.7\Omega$		23		ns
Rise time 上升时间	t_r			25		
Turn-off delay time 关闭延迟时间	$t_{d(off)}$			32		
Fall time 下降时间	t_f			30		

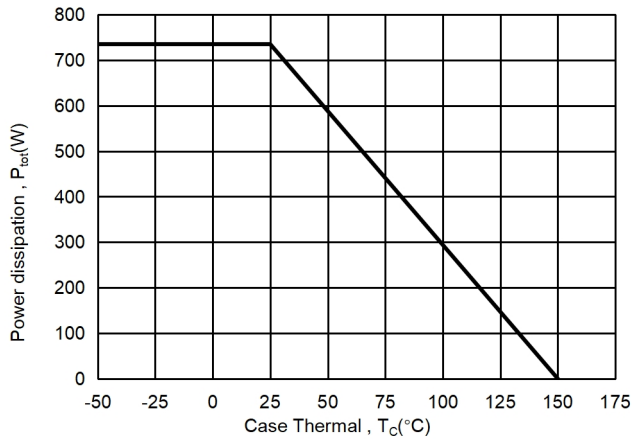
Table 5 Reverse diode characteristics/体二极管反向特性

Parameter 参数	Symbol 符号	Test conditions 测试条件	Value/值			Unit 单位
			Min.	Typ.	Max.	
Drain-source reverse voltage 体二极管正向压降	V_{SD}	$I_S=5A, V_{GS}=0V$		0.8	1.5	V
Body diode reverse recovery time 反向恢复时间	t_{rr}	$I_S=5A$, $di_S/dt=-100A/\mu s$		170		ns
Body diode reverse recovery charge 反向恢复电荷	Q_{rr}			0.6		μC

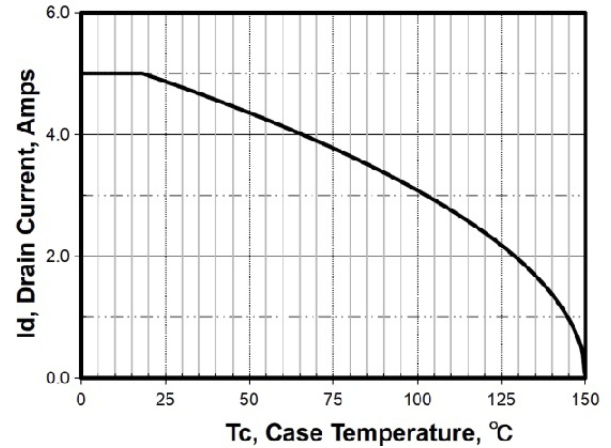
4. Electrical characteristics diagrams

电气特性图表

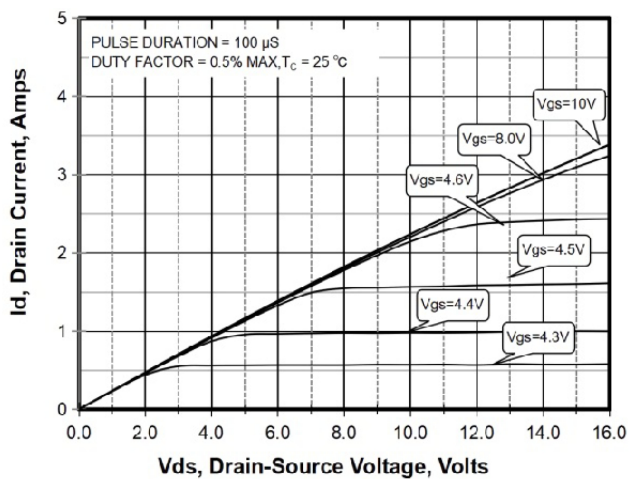
Power dissipation/耗散功率



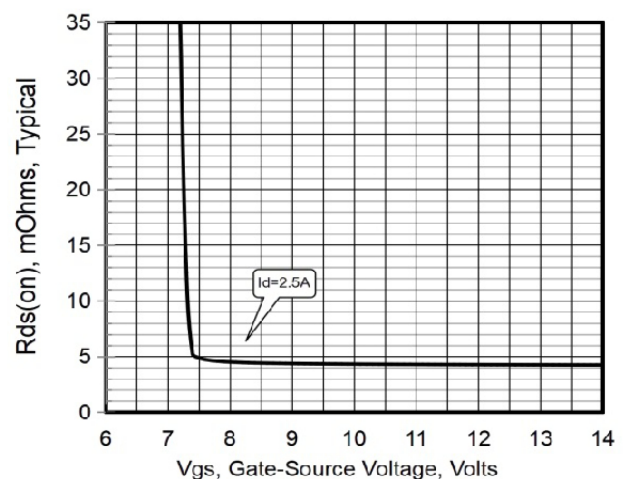
Max.Continuous drain current/最大漏极电流与壳温



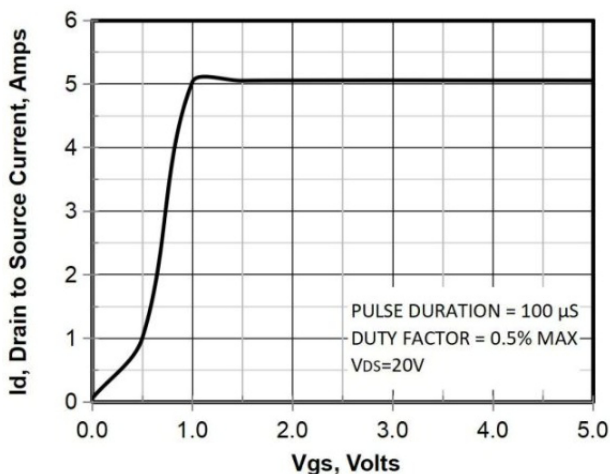
Typ.Output characteristic/典型输出特性



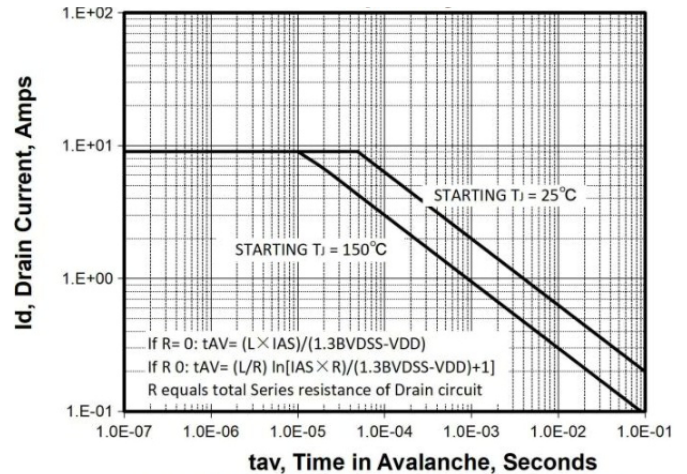
Typ.Drain-source on-state resistance/典型漏源导通电阻



Typ.Transfer characteristic/典型传输特性



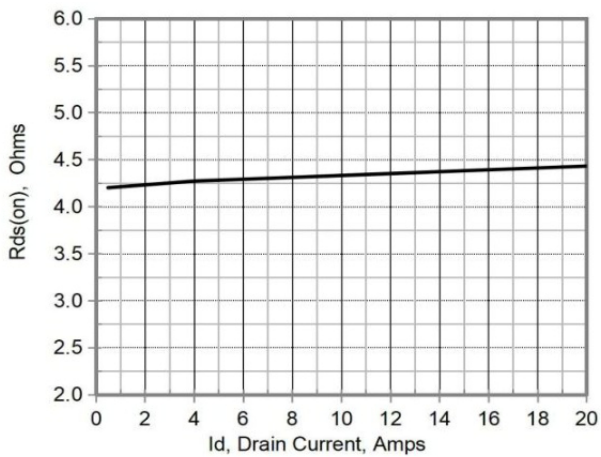
Unclamped Inductive Switching Capability/非钳位感性开关能力



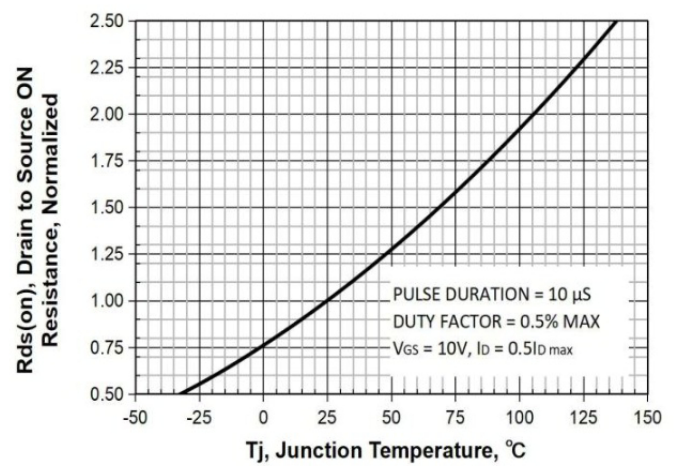
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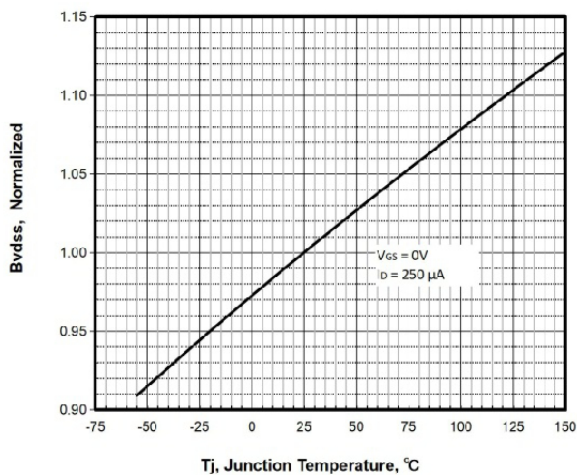
Typ.Drain-source on-state resistance/典型漏源导通电阻



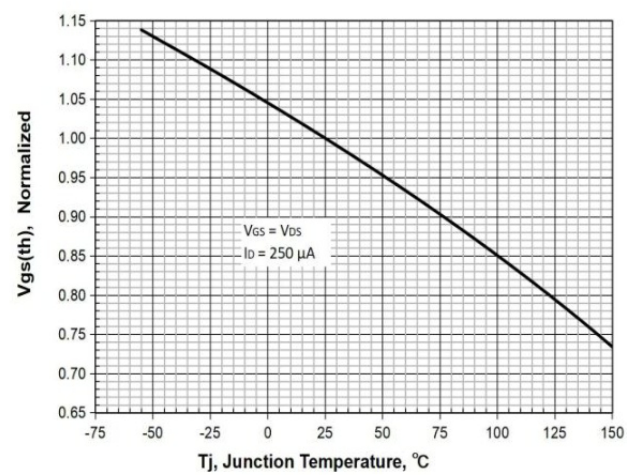
Typ.Drain-source on-state resistance/典型漏源导通电阻



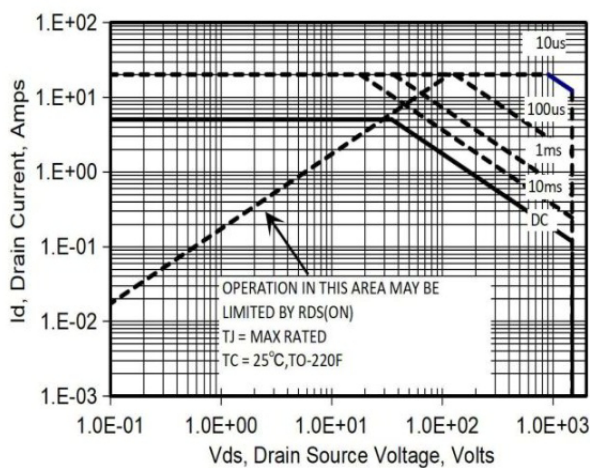
$V_{(BR)DSS}$ vs junction temperature/漏源击穿电压与结温特性



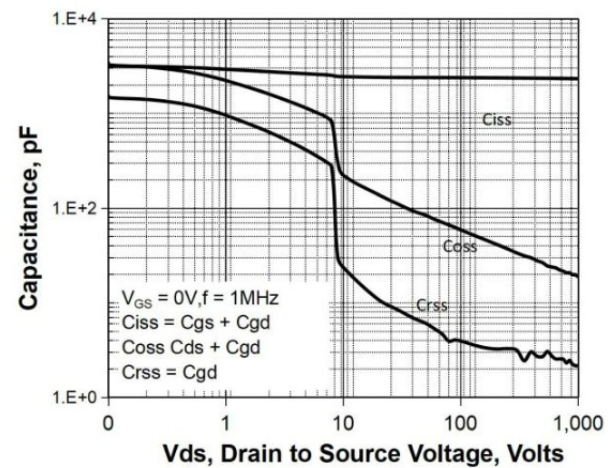
Typ.Gate threshold voltage/门级阈值电压结温特性



Safe operating area/安全工作区



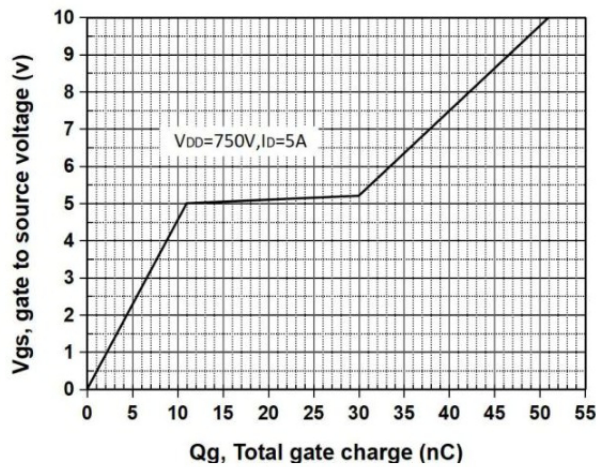
Typ.Capacitances characteristic/典型电容特性



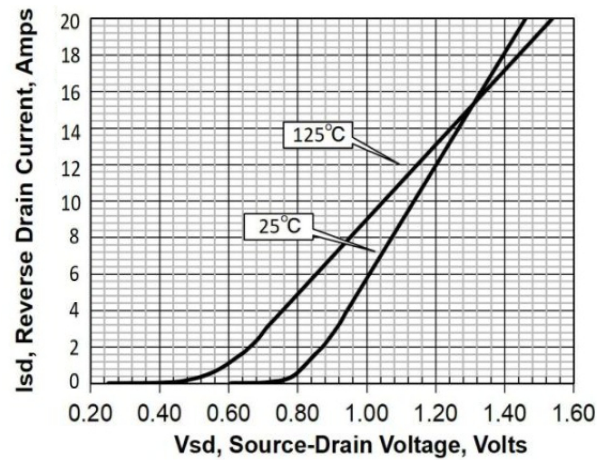
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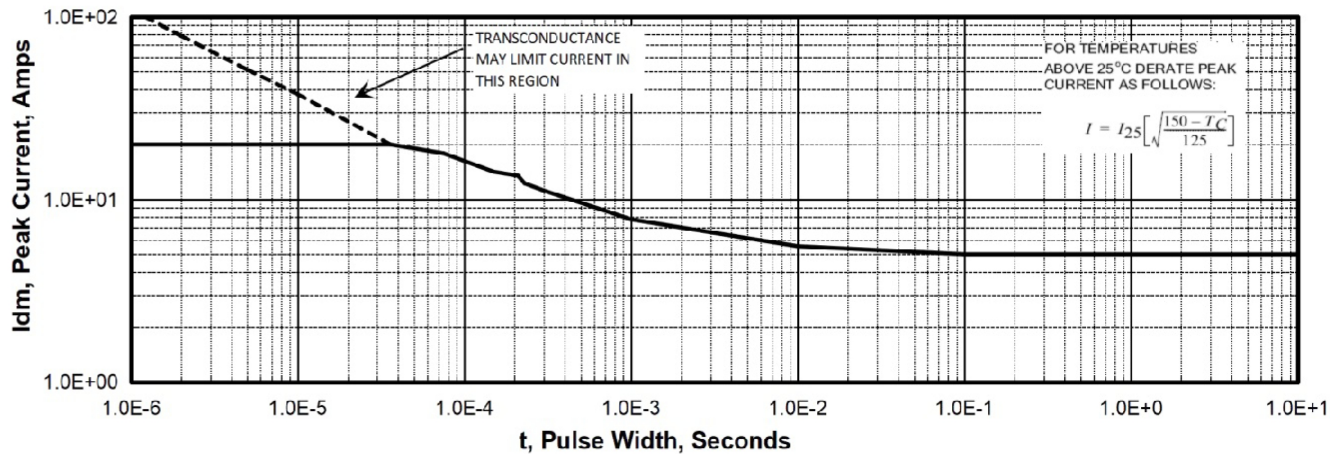
Typ.Gate charge/典型门级电荷



Typ.Reverse drain current characteristics/典型二极管特性



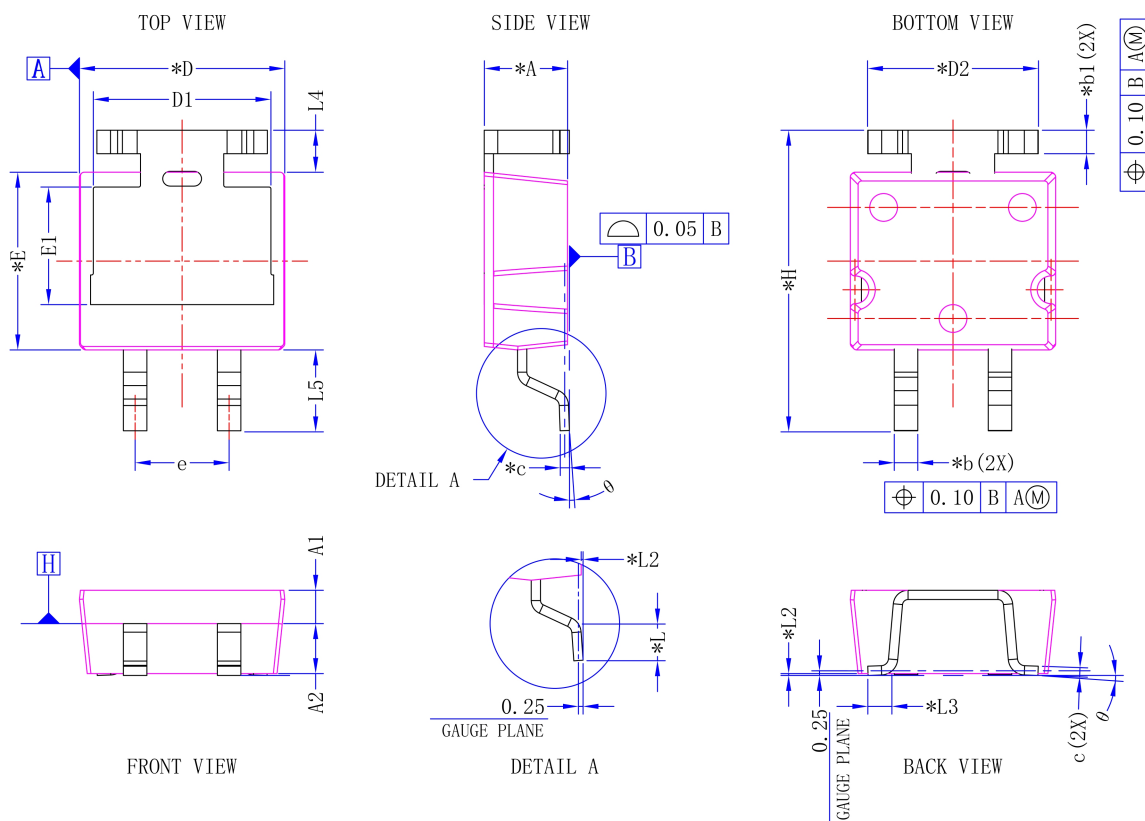
Peak Current Capability/峰值电流能力



5. Package outline

封装外形

Figure 1. Outline TSC263-4L, dimensions in mm/ TSC263-4L外形尺寸 (毫米)



NOTES:

- ALL DIMENSIONS ARE IN MILLIMETER. ANGLES ARE IN DEGREE.
- DIMENSION "D" DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSIONS. INTERLEAD FLASH SHALL NOT EXCEED 0.150 MM PER SIDE. DIMENSION "E" DOES NOT INCLUDE MOLD FLASH, GATE BURRS, THE GATE BURRS SHALL NOT EXCEED 0.15MM.
- DIMENSIONS D AND E ARE DETERMINED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY EXCLUSIVE OF MOLD FLASH, TIE BAR BURRS, GATE BURRS AND INTERLEAD FLASH, BUT INCLUDING ANY MISMATCH BETWEEN THE TOP AND BOTTOM OF THE PLASTIC BODY.

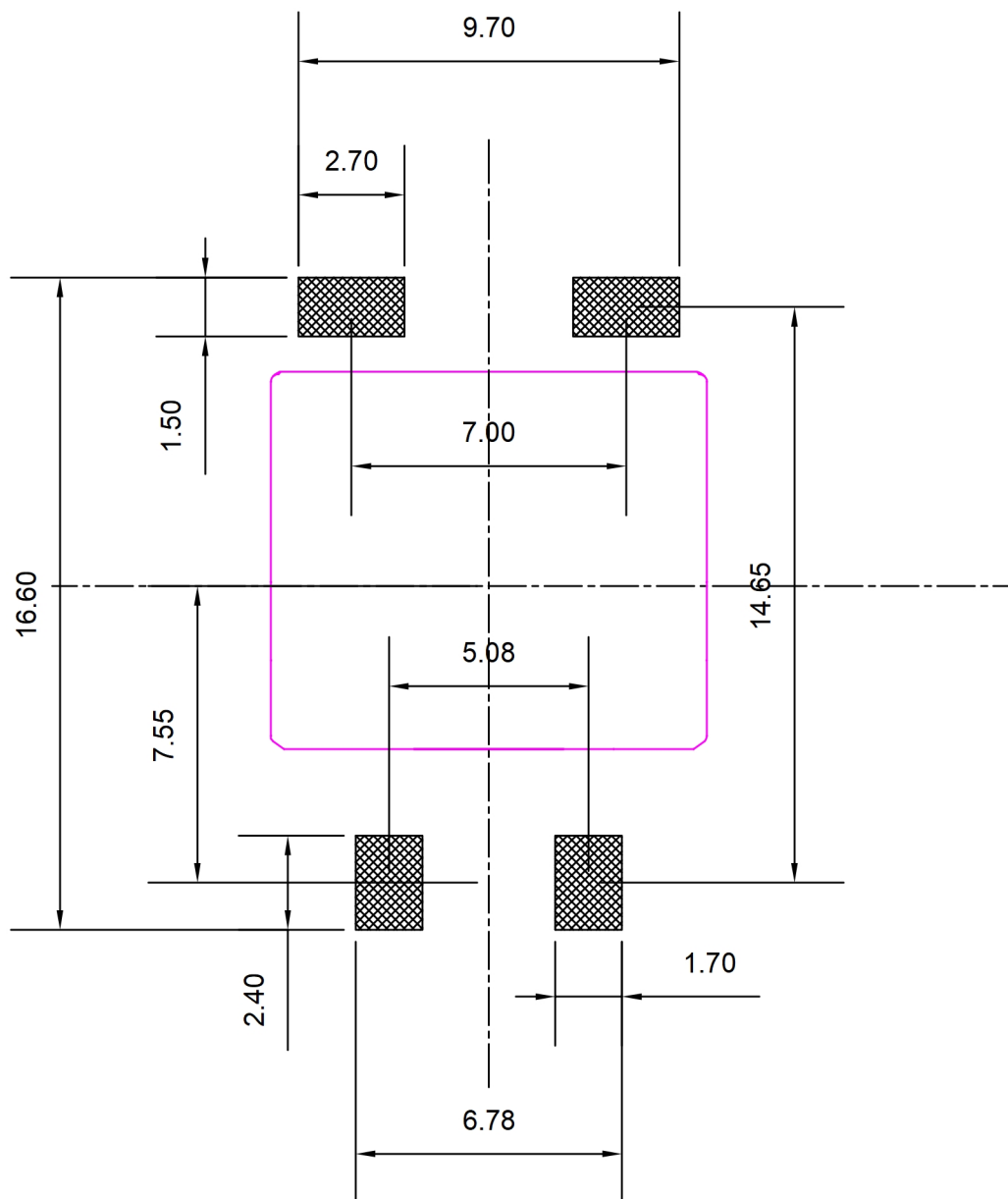
注:

- 所有尺寸均以毫米为单位。角度以度为单位。
- 尺寸 D 不包括引脚间飞边或突出物。引脚间飞边在每侧不得超过0.15mm。尺寸 E 不包括模具飞边、浇口残余物，浇口残余物不得超过0.15mm。
- 尺寸 D、E 是在塑胶本体的最外极限确定的，不包括模具飞边、连接条残余、浇口残余和引脚间飞边，但包括塑胶本体顶部和底部之间可能存在的任何不匹配或错位。

6. Recommended Land Pattern

推荐焊盘尺寸

Figure 2. TSC263-4L Effective Solderable Area for Reflow Soldering/ TSC263-4L 回流焊接有效可焊面积



solder land/焊盘区域

----- Package Reference Centerline/封装参考中心线

dimensions in mm/单位为毫米

注:
所示焊盘尺寸仅供参考。为确保最佳散热性能及焊接质量, 建议根据实际应用中的 PCB 板材、层数及散热设计对焊盘进行优化调整
The land pattern dimensions provided are for reference only. To achieve optimal thermal performance, actual design adjustments should be considered based on the specific PCB materials, layer stack-up, and thermal dissipation requirements.



7. Revision history
修订历史

Table 6 Date and version number/日期与版本号

Date日期	Revision版本	Changes更改内容
2026-07-11	Rev. G 1.0	Target Datasheet (目标规格书)

8. Matters needing attention
注意事项

Appendix 1. Important Technical Guidance, Application Policy, and Copyright Notice/重要技术指南、应用规范与版权声明

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