NOVOSENSE

NSI822x
High Reliability Dual-Channel Digital Isolators
Datasheet (EN) 2.0

Product Overview

The NSI822x devices are high reliability dual-channel digital isolators. The NSI822x device is safety certified by UL1577 support 5kVrms insulation withstand voltage, while providing high electromagnetic immunity and low emissions at low power consumption. The data rate of the NSI822x is up to 150Mbps, and the common-mode transient immunity (CMTI) is up to 250kV/μs. The NSI822x device provides digital channel direction configuration and the default output level configuration when the input power is lost. Wide supply voltage of the NSI822x device support to connect with most digital interface directly, easy to do the level shift. High system level EMC performance enhance reliability and stability of use.

Key Features

- Up to 5000V_{rms} Insulation voltage
- Data rate: DC to 150Mbps
- Power supply voltage: 2.5V to 5.5V
- High CMTI: 250kV/μs
- Chip level ESD: HBM: ±8kV
- Robust EMC Reinforced Dual-Channel Digital Isolators for SOW8 wide body
- Default output high level or low level option
- Isolation surge voltage: >10kV
- Low power consumption: 1.5mA/ch (1 Mbps)
- Low propagation delay: <18ns
- Operation temperature: -55℃~125℃
- RoHS-compliant packages:
  SOP8 narrow body
  SOW8 wide body

Safety Regulatory Approvals

- UL recognition: up to 5000V_{rms} for 1 minute per UL1577
- CQC certification per GB4943.1
- CSA component notice 5A
- DIN EN IEC 60747-17 (VDE 0884-17)

Applications

- Industrial automation system
- Isolated SPI, RS232, RS485
- General-purpose multichannel isolation
- Motor control

Device Information

Part Number	Package	Body Size
NSI822xNx-DSPR	SOP8	4.90mm × 3.90mm
NSI822xCx-DSPR	SOP8	4.90mm × 3.90mm
NSI822xWx-DSWVR	SOW8	5.85mm × 7.50mm
NSI822xCx-DSWVR	SOW8	5.85mm × 7.50mm

Functional Block Diagrams

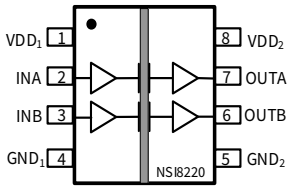

Figure 1.1 NSI8220 Block Diagram

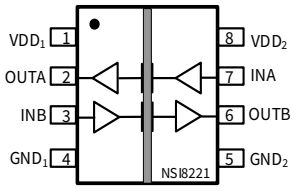

Figure 1.2 NSI8221 Block Diagram

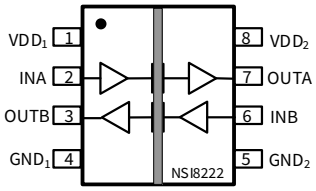

Figure 1.3 NSI8222 Block Diagram

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1. Pin Configuration and Functions

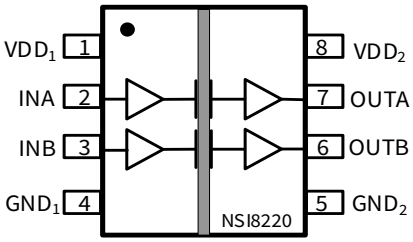


Figure 1.1 NSI8220 Package

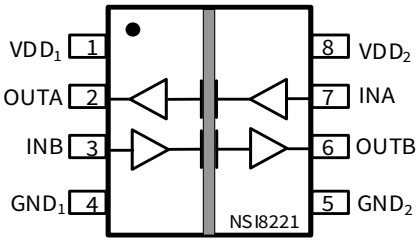


Figure 1.2 NSI8221 Package

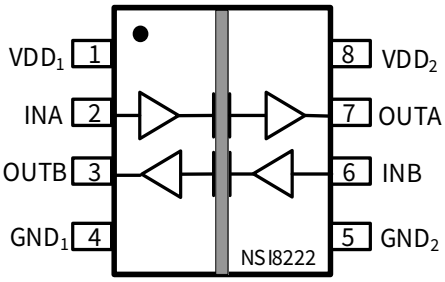


Figure 1.3 NSI8222 Package

Table1.1 NSI822x Pin Configuration and Description

NSI8220W PIN NO.	*NSI8221W PIN NO.*	*NSI8222W PIN NO.*	*SYMBOL*	*FUNCTION*
1	1	1	VDD1	Power Supply for Isolator Side 1
2	7	2	INA	Logic Input A
3	3	6	INB	Logic Input B
4	4	4	GND1	Ground 1, the ground reference for Isolator Side 1
5	5	5	GND2	Ground 2, the ground reference for Isolator Side 2
6	6	3	OUTB	Logic Output B
7	2	7	OUTA	Logic Output A
8	8	8	VDD2	Power Supply for Isolator Side 2

2. Absolute Maximum Ratings

Parameters	Symbol	Min	Typ	Max	Unit	Comments
Power Supply Voltage	VDD1, VDD2	-0.5		6.5	V	
Maximum Input Voltage	V_{INA}, V_{INB}	-0.4		VDD+0.4	V	The maximum voltage must not exceed 6.5V
Maximum Output Voltage	V_{OUTA}, V_{OUTB}	-0.4		VDD+0.4	V	The maximum voltage must not exceed 6.5V
Maximum Input/Output Pulse Voltage	V_{INA}, V_{INB}, V_{OUTA}, V_{OUTB}	-0.8		VDD+0.8	V	Pulse width should be less than 100ns, and the duty cycle should be less than 10%
Output current	Io	-15		15	mA	
Operating Temperature	Topr	-55		125	℃	
Junction Temperature	Tj			150	℃	
Storage Temperature	Tstg	-65		150	℃	

(1) Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under Recommended Operating conditions. Exposure to Absolute Maximum Rated conditions for extended periods may affect device reliability.

(2) Power supply voltage and input/output voltage are respect to the local ground terminal (GND1 or GND2) voltage values.

3. ESD Ratings

Parameters	Ratings	Value	Unit
Electrostatic discharge (ESD)	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001(2)	±8000	V
	Charged device model (CDM), per JEDEC specification JESD22-C101(3)	±2000	V

(1) Though this device features proprietary protection circuitry, proper ESD precautions should be considered to avoid performance degradation of damage due to high energy ESD event. Charged devices and circuit boards may discharge without detection.

(2) Safe manufacturing requires 500-V HBM and standard ESD precautions, per JEDEC document JEP155.

(3) Safe manufacturing requires 250-V CDM and standard ESD precautions, per JEDEC document JEP157.

4. Recommended Operating Conditions

Parameters	Symbol	min	typ	max	unit
Power Supply Voltage	VDD1, VDD2	2.5		5.5	V

Operating Temperature	Topr	-55		125	℃
High Level Input Voltage	VIH	0.7*VDD			V
Low Level Input Voltage	VIL			0.3*VDD	V
Data rate	DR			150	Mbps

5. Thermal Characteristics

Parameters	*Symbol*	*SOP8*	*SOW8*	*Unit*
IC Junction-to-Air Thermal Resistance	$R_{\theta JA}$	137.7	84.3	℃/W
Junction-to-case (top) thermal resistance	$R_{\theta JC(top)}$	54.9	36.3	℃/W
Junction-to-board thermal resistance	$R_{\theta JB}$	71.7	47.0	℃/W
Junction-to-top characterization parameter	Ψ_{JT}	7.6	9.6	℃/W
Junction-to-board characterization parameter	Ψ_{JB}	31.0	29.2	℃/W

6. Specifications

6.1. Electrical Characteristics

(VDD1=2.5V~5.5V, VDD2=2.5V~5.5V, Ta=-55℃ to 125℃. Unless otherwise noted, Typical values are at VDD1 = 5V, VDD2 = 5V, Ta = 25℃)

Parameters	*Symbol*	*Min*	*Typ*	*Max*	*Unit*	*Comments*
Power on Reset	VDD_{POR}	2	2.2	2.4	V	POR threshold as during power-up
	VDD_{HYS}		0.1		V	POR threshold Hysteresis
Rising input switching threshold	V_{IT+}		0.6*VDD	0.7*VDD	V	
Falling input switching threshold	V_{IT-}	0.3*VDD	0.4*VDD		V	
Input threshold voltage hysteresis	$V_{I(HYS)}$		0.2*VDD		V	
High Level Output Voltage	V_{OH}	VDD-0.4			V	I_{OH} ≤ 4mA
Low Level Output Voltage	V_{OL}			0.4	V	I_{OL} ≤ 4mA
Output Impedance	R_{out}		50		ohm	
Input Pull high or low Current	I_{pull}		5	10	μA	

	NSI822x-DSPR					
Start Up Time after POR	trbs		15	30	μs	
Common Mode Transient Immunity	CMTI	±150	±200		kV/μs	See Figure 6.14
	NSI822x-DSWVR					
Start Up Time after POR	trbs		22	32	μs	
Common Mode Transient Immunity	CMTI	±200	±250		kV/μs	See Figure 6.14

6.2. Supply Current Characteristics –5V Supply

(VDD1=5V± 10%, VDD2=5V± 10%, Ta=-55℃ to 125℃. Unless otherwise noted, Typical values are at **VDD1 = 5V, VDD2 = 5V,** Ta = 25℃)

Parameters	*Symbol*	*Min*	*Typ*	*Max*	*Unit*	*Comments*
Supply current	**NSI8220-DSPR**					
	I_{DD1}(Q0)		0.62	0.90	mA	All Input 0V for NSI822xN0 Or All Input at supply for NSI822xN1
	I_{DD2}(Q0)		1.27	1.84	mA	
	I_{DD1}(Q1)		2.3	3.04	mA	All Input at supply for NSI822xN0 Or All Input 0V for NSI822xN1
	I_{DD2}(Q1)		1.31	1.73	mA	
	I_{DD1}(1M)		1.50	1.98	mA	All Input with 1Mbps, C_L=15pF
	I_{DD2}(1M)		1.43	1.89	mA	
	I_{DD1}(10M)		1.57	2.07	mA	All Input with 10Mbps, C_L=15pF
	I_{DD2}(10M)		2.59	3.39	mA	
	I_{DD1}(100M)		2.02	2.72	mA	All Input with 100Mbps, C_L = 15pF
	I_{DD2}(100M)		12.56	16.95	mA	
	NSI8221-DSPR / NSI8222-DSPR					
	I_{DD1}(Q0)		1.07	1.36	mA	All Input 0V for NSI822xN0 Or All Input at supply for NSI822xN1
	I_{DD2}(Q0)		1.07	1.36	mA	
	I_{DD1}(Q1)		1.98	2.59	mA	All Input at supply for NSI822xN0 Or All Input 0V for NSI822xN1
	I_{DD2}(Q1)		1.98	2.59	mA	
	I_{DD1}(1M)		1.59	2.13	mA	All Input with 1Mbps, C_L=15pF
	I_{DD2}(1M)		1.59	2.13	mA	

Parameters	Symbol	Min	Typ	Max	Unit	Comments
	I_{DD1}(10M)		2.12	2.77	mA	All Input with 10Mbps, C_L=15pF
	I_{DD2}(10M)		2.12	2.77	mA	
	I_{DD1}(100M)		7.57	10.06	mA	All Input with 100Mbps, C_L = 15pF
	I_{DD2}(100M)		7.57	10.06	mA	
	NSI8220-DSWVR					
	I_{DD1}(Q0)		0.79	1.24	mA	All Input 0V for NSI822xW0 Or All Input at supply for NSI822xW1
	I_{DD2}(Q0)		1.84	2.44	mA	
	I_{DD1}(Q1)		3.43	4.55	mA	All Input at supply for NSI822xW0 Or All Input 0V for NSI822xW1
	I_{DD2}(Q1)		1.95	2.56	mA	
	I_{DD1}(1M)		2.13	2.80	mA	All Input with 1Mbps, C_L=15pF
	I_{DD2}(1M)		1.91	2.52	mA	
	I_{DD1}(10M)		2.15	2.82	mA	All Input with 10Mbps, C_L=15pF
	I_{DD2}(10M)		3.03	3.65	mA	
	I_{DD1}(100M)		2.61	3.97	mA	All Input with 100Mbps, C_L = 15pF
	I_{DD2}(100M)		13.28	17.53	mA	
	NSI8221-DSWVR / NSI8222-DSWVR					
	I_{DD1}(Q0)		1.55	2.12	mA	All Input 0V for NSI822xW0 Or All Input at supply for NSI822xW1
	I_{DD2}(Q0)		1.55	2.12	mA	
	I_{DD1}(Q1)		2.88	3.83	mA	All Input at supply for NSI822xW0 Or All Input 0V for NSI822xW1
	I_{DD2}(Q1)		2.88	3.83	mA	
	I_{DD1}(1M)		2.28	2.98	mA	All Input with 1Mbps, C_L=15pF
	I_{DD2}(1M)		2.28	2.98	mA	
	I_{DD1}(10M)		2.84	3.77	mA	All Input with 10Mbps, C_L=15pF
	I_{DD2}(10M)		2.84	3.77	mA	
	I_{DD1}(100M)		8.29	10.94	mA	All Input with 100Mbps, C_L = 15pF
	I_{DD2}(100M)		8.29	10.94	mA	

6.3. Supply Current Characteristics –3.3V Supply

(VDD1=3.3V± 10%, VDD2=3.3V± 10%, Ta=-55℃ to 125℃. Unless otherwise noted, Typical values are at **VDD1 = 3.3V, VDD2 = 3.3V,** Ta = 25℃)

Parameters	*Symbol*	*Min*	*Typ*	*Max*	*Unit*	*Comments*
Supply current	**NSI8220-DSPR**					
	I_{DD1}(Q0)		0.61	0.88	mA	All Input 0V for NSI822xN0 Or All Input at supply for NSI822xN1
	I_{DD2}(Q0)		1.24	1.79	mA	
	I_{DD1}(Q1)		2.28	3.01	mA	All Input at supply for NSI822xN0 Or All Input 0V for NSI822xN1
	I_{DD2}(Q1)		1.27	1.67	mA	
	I_{DD1}(1M)		1.45	1.92	mA	All Input with 1Mbps, C_L=15pF
	I_{DD2}(1M)		1.34	1.77	mA	
	I_{DD1}(10M)		1.52	2.01	mA	All Input with 10Mbps, C_L=15pF
	I_{DD2}(10M)		2.18	2.88	mA	
	I_{DD1}(100M)		1.87	2.52	mA	All Input with 100Mbps, C_L = 15pF
	I_{DD2}(100M)		8.76	11.83	mA	
	NSI8221-DSPR / NSI8222-DSPR					
	I_{DD1}(Q0)		1.03	1.34	mA	All Input 0V for NSI822xN0 Or All Input at supply for NSI822xN1
	I_{DD2}(Q0)		1.03	1.34	mA	
	I_{DD1}(Q1)		1.93	2.57	mA	All Input at supply for NSI822xN0 Or All Input 0V for NSI822xN1
	I_{DD2}(Q1)		1.93	2.57	mA	
	I_{DD1}(1M)		1.52	1.99	mA	All Input with 1Mbps, C_L=15pF
	I_{DD2}(1M)		1.52	1.99	mA	
	I_{DD1}(10M)		1.88	2.47	mA	All Input with 10Mbps, C_L=15pF
	I_{DD2}(10M)		1.88	2.47	mA	
	I_{DD1}(100M)		5.46	7.37	mA	All Input with 100Mbps, C_L = 15pF
	I_{DD2}(100M)		5.46	7.37	mA	
	NSI8220-DSWVR					
	I_{DD1}(Q0)		0.77	1.21	mA	All Input 0V for NSI822xW0 Or All Input at supply for NSI822xW1
	I_{DD2}(Q0)		1.80	2.43	mA	
	I_{DD1}(Q1)		3.39	4.54	mA	

Parameters	Symbol	Min	Typ	Max	Unit	Comments
	I_{DD2}(Q1)		1.91	2.51	mA	All Input at supply for NSI822xW0 Or All Input 0V for NSI822xW1
	I_{DD1}(1M)		2.10	2.76	mA	All Input with 1Mbps, C_L=15pF
	I_{DD2}(1M)		1.87	2.46	mA	
	I_{DD1}(10M)		2.15	2.86	mA	All Input with 10Mbps, C_L=15pF
	I_{DD2}(10M)		2.61	3.50	mA	
	I_{DD1}(100M)		2.57	3.44	mA	All Input with 100Mbps, C_L = 15pF
	I_{DD2}(100M)		9.39	12.58	mA	
	NSI8221-DSWVR / NSI8222-DSWVR					
	I_{DD1}(Q0)		1.50	1.98	mA	All Input 0V for NSI822xW0 Or All Input at supply for NSI822xW1
	I_{DD2}(Q0)		1.50	1.98	mA	
	I_{DD1}(Q1)		2.82	3.78	mA	All Input at supply for NSI822xW0 Or All Input 0V for NSI822xW1
	I_{DD2}(Q1)		2.82	3.78	mA	
	I_{DD1}(1M)		2.20	2.94	mA	All Input with 1Mbps, C_L=15pF
	I_{DD2}(1M)		2.20	2.94	mA	
	I_{DD1}(10M)		2.57	3.44	mA	All Input with 10Mbps, C_L=15pF
	I_{DD2}(10M)		2.57	3.44	mA	
	I_{DD1}(100M)		6.11	8.25	mA	All Input with 100Mbps, C_L = 15pF
	I_{DD2}(100M)		6.11	8.25	mA	

6.4. Supply Current Characteristics–2.5V Supply

(VDD1=2.5V± 10%, VDD2=2.5V± 10%, Ta=-55℃ to 125℃. Unless otherwise noted, Typical values are at **VDD1 = 2.5V, VDD2 = 2.5V,** Ta = 25℃)

Parameters	*Symbol*	*Min*	*Typ*	*Max*	*Unit*	*Comments*
Supply current	**NSI8220-DSPR**					
	I_{DD1}(Q0)		0.59	0.85	mA	All Input 0V for NSI822xN0 Or All Input at supply for NSI822xN1
	I_{DD2}(Q0)		1.21	1.74	mA	
	I_{DD1}(Q1)		2.24	2.94	mA	All Input at supply for NSI822xN0 Or All Input 0V for NSI822xN1
	I_{DD2}(Q1)		1.25	1.68	mA	
	I_{DD1}(1M)		1.42	1.88	mA	All Input with 1Mbps, C_L=15pF
	I_{DD2}(1M)		1.29	1.72	mA	
	I_{DD1}(10M)		1.50	1.97	mA	All Input with 10Mbps, C_L=15pF
	I_{DD2}(10M)		1.99	2.67	mA	
	I_{DD1}(100M)		1.81	2.44	mA	All Input with 100Mbps, C_L = 15pF
	I_{DD2}(100M)		7.23	9.76	mA	
	NSI8221-DSPR / NSI8222-DSPR					
	I_{DD1}(Q0)		1.00	1.33	mA	All Input 0V for NSI822xN0 Or All Input at supply for NSI822xN1
	I_{DD2}(Q0)		1.00	1.33	mA	
	I_{DD1}(Q1)		1.90	2.55	mA	All Input at supply for NSI822xN0 Or All Input 0V for NSI822xN1
	I_{DD2}(Q1)		1.90	2.55	mA	
	I_{DD1}(1M)		1.48	1.94	mA	All Input with 1Mbps, C_L=15pF
	I_{DD2}(1M)		1.48	1.94	mA	
	I_{DD1}(10M)		1.76	2.32	mA	All Input with 10Mbps, C_L=15pF
	I_{DD2}(10M)		1.76	2.32	mA	
	I_{DD1}(100M)		4.50	5.99	mA	All Input with 100Mbps, C_L = 15pF
	I_{DD2}(100M)		4.50	5.99	mA	
	NSI8220-DSWVR					
	I_{DD1}(Q0)		0.75	1.19	mA	All Input 0V for NSI822xW0 Or All Input at supply for NSI822xW1
	I_{DD2}(Q0)		1.77	2.37	mA	
	I_{DD1}(Q1)		3.34	4.41	mA	

Parameters	Symbol	Min	Typ	Max	Unit	Comments
	I_{DD2}(Q1)		1.88	2.51	mA	All Input at supply for NSI822xW0 Or All Input 0V for NSI822xW1
	I_{DD1}(1M)		2.06	2.72	mA	All Input with 1Mbps, C_L=15pF
	I_{DD2}(1M)		1.84	2.44	mA	
	I_{DD1}(10M)		2.11	2.78	mA	All Input with 10Mbps, C_L=15pF
	I_{DD2}(10M)		2.40	3.21	mA	
	I_{DD1}(100M)		2.52	3.30	mA	All Input with 100Mbps, C_L = 15pF
	I_{DD2}(100M)		7.57	9.98	mA	
	NSI8221-DSWVR / NSI8222-DSWVR					
	I_{DD1}(Q0)		1.46	1.93	mA	All Input 0V for NSI822xW0 Or All Input at supply for NSI822xW1
	I_{DD2}(Q0)		1.46	1.93	mA	
	I_{DD1}(Q1)		2.76	3.67	mA	All Input at supply for NSI822xW0 Or All Input 0V for NSI822xW1
	I_{DD2}(Q1)		2.76	3.67	mA	
	I_{DD1}(1M)		2.14	2.85	mA	All Input with 1Mbps, C_L=15pF
	I_{DD2}(1M)		2.14	2.85	mA	
	I_{DD1}(10M)		2.42	3.22	mA	All Input with 10Mbps, C_L=15pF
	I_{DD2}(10M)		2.42	3.22	mA	
	I_{DD1}(100M)		5.14	6.81	mA	All Input with 100Mbps, C_L = 15pF
	I_{DD2}(100M)		5.14	6.81	mA	

6.5. Switching Characteristics - 5V Supply

(VDD1=5V± 10%, VDD2=5V± 10%, Ta=-55℃ to 125℃. Unless otherwise noted, Typical values are at **VDD1 = 5V, VDD2 = 5V,** Ta = 25℃)

Parameters	Symbol	Min	Typ	Max	Unit	Comments
	NSI822x-DSPR					
Data Rate	DR	0		150	Mbps	
Minimum Pulse Width	PW			5.0	ns	
Propagation Delay	t_{PLH}		9.9	18	ns	See Figure 6.13 , C_L = 15pF
	t_{PHL}		8.7	18	ns	See Figure 6.13 , C_L = 15pF
	NSI822x-DSWVR					
Data Rate	DR	0		100	Mbps	
Minimum Pulse Width	PW			8.3	ns	
Propagation Delay	t_{PLH}		12.5	18	ns	See Figure 6.13 , C_L = 15pF
	t_{PHL}		12.1	18	ns	See Figure 6.13 , C_L = 15pF
	NSI822x-DSPR / NSI822x-DSWVR					
Pulse Width Distortion $\lvert t_{PHL} - t_{PLH} \rvert$	PWD			5.0	ns	See Figure 6.13 , C_L = 15pF
Rising Time	t_r			5.0	ns	See Figure 6.13 , C_L = 15pF
Falling Time	t_f			5.0	ns	See Figure 6.13 , C_L = 15pF
Peak Eye Diagram Jitter	t_{JIT}(PK)		2.5		ns	
Channel-to-Channel Delay Skew	t_{SK}(c2c)			2.5	ns	
Part-to-Part Delay Skew	t_{SK}(p2p)			5.0	ns	

6.6. Switching Characteristics - 3.3V Supply

(VDD1=3.3V± 10%, VDD2=3.3V± 10%, Ta=-55℃ to 125℃. Unless otherwise noted, Typical values are at **VDD1 = 3.3V, VDD2 = 3.3V,** Ta = 25℃)

Parameters	Symbol	Min	Typ	Max	Unit	Comments
	NSI822x-DSPR					
Data Rate	DR	0		150	Mbps	
Minimum Pulse Width	PW			5.0	ns	

Propagation Delay	t_{PLH}		10.8	19	ns	See Figure 6.13 , C_L = 15pF
	t_{PHL}		9.6	19	ns	See Figure 6.13 , C_L = 15pF
	NSI822x-DSWVR					
Data Rate	DR	0		100	Mbps	
Minimum Pulse Width	PW			8.3	ns	
Propagation Delay	t_{PLH}		13.0	19	ns	See Figure 6.13 , C_L = 15pF
	t_{PHL}		12.5	19	ns	See Figure 6.13 , C_L = 15pF
	NSI822x-DSPR / NSI822x-DSWVR					
Pulse Width Distortion $\lvert t_{PHL} - t_{PLH} \rvert$	PWD			5.0	ns	See Figure 6.13 , C_L = 15pF
Rising Time	t_r			5.0	ns	See Figure 6.13 , C_L = 15pF
Falling Time	t_f			5.0	ns	See Figure 6.13 , C_L = 15pF
Peak Eye Diagram Jitter	t_{JIT}(PK)		2.5		ns	
Channel-to-Channel Delay Skew	t_{SK}(c2c)			2.5	ns	
Part-to-Part Delay Skew	t_{SK}(p2p)			5.0	ns	

6.7. Switching Characteristics - 2.5V Supply

(VDD1=2.5V± 10%, VDD2=2.5V± 10%, Ta=-55℃ to 125℃. Unless otherwise noted, Typical values are at **VDD1 = 2.5V, VDD2 = 2.5V,** Ta = 25℃)

Parameters	*Symbol*	*Min*	*Typ*	*Max*	*Unit*	*Comments*
	NSI822x-DSPR					
Data Rate	DR	0		150	Mbps	
Minimum Pulse Width	PW			5.0	ns	
Propagation Delay	t_{PLH}		12.0	20	ns	See Figure 6.13 , C_L = 15pF
	t_{PHL}		11.0	20	ns	See Figure 6.13 , C_L = 15pF
	NSI822x-DSWVR					
Data Rate	DR	0		100	Mbps	
Minimum Pulse Width	PW			8.3	ns	
Propagation Delay	t_{PLH}		14.2	20	ns	See Figure 6.13 , C_L = 15pF
	t_{PHL}		13.5	20	ns	See Figure 6.13 , C_L = 15pF
	NSI822x-DSPR / NSI822x-DSWVR					

Pulse Width Distortion $\lvert t_{PHL} - t_{PLH} \rvert$	PWD			5.0	ns	See Figure 6.13 , C_L = 15pF
Rising Time	t_r			5.0	ns	See Figure 6.13 , C_L = 15pF
Falling Time	t_f			5.0	ns	See Figure 6.13 , C_L = 15pF
Peak Eye Diagram Jitter	t_{JIT}(PK)		2.5		ns	
Channel-to-Channel Delay Skew	t_{SK}(c2c)			2.5	ns	
Part-to-Part Delay Skew	t_{SK}(p2p)			5.0	ns	

6.8. Typical Performance Characteristics

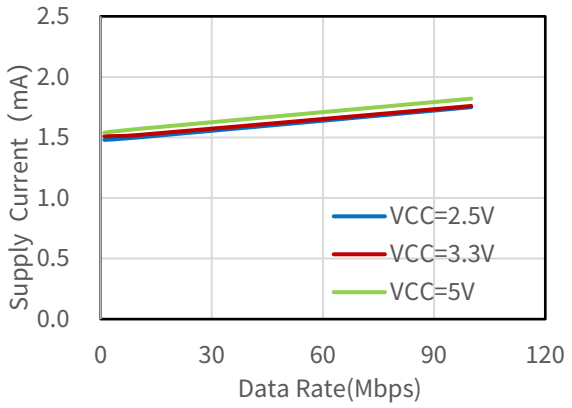


Figure 6.1 NSI8220-DSPR VDD1 Supply Current vs Data Rate

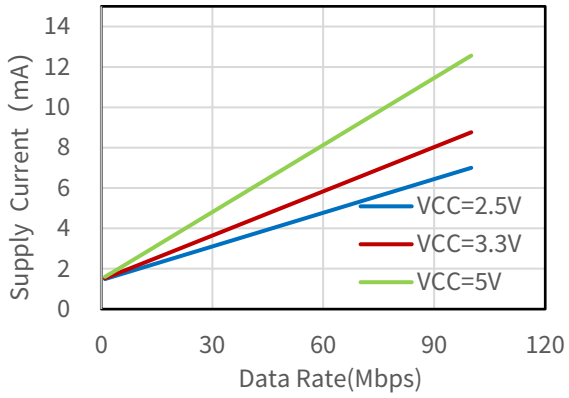


Figure 6.2 NSI8220-DSPR VDD2 Supply Current vs Data Rate

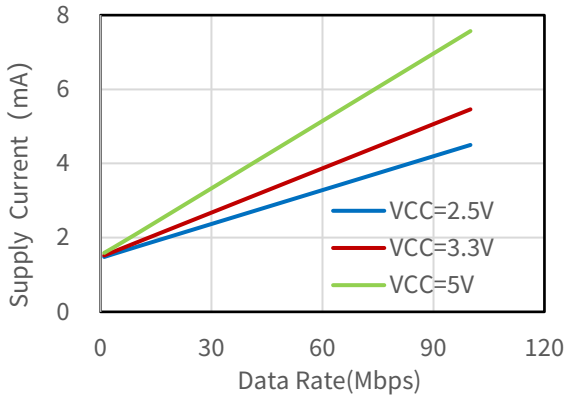


Figure 6.3 NSI8221-DSPR / NSI8222-DSPR
VDD1 Supply Current vs Data Rate

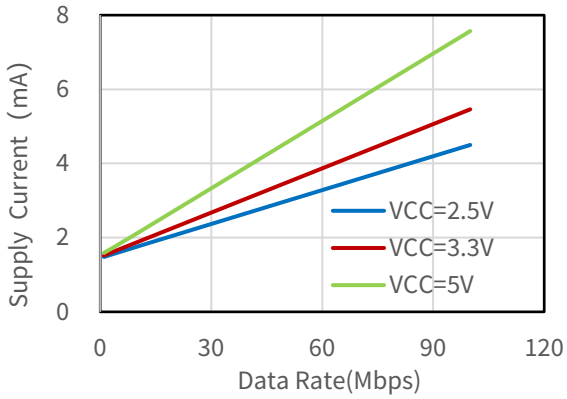


Figure 6.4 NSI8221-DSPR / NSI8222-DSPR
VDD2 Supply Current vs Data Rate

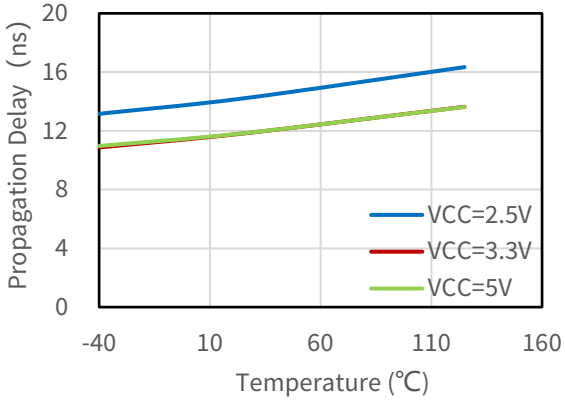


Figure 6.5 NSI822x-DSPR Rising Edge
Propagation Delay Vs Temp

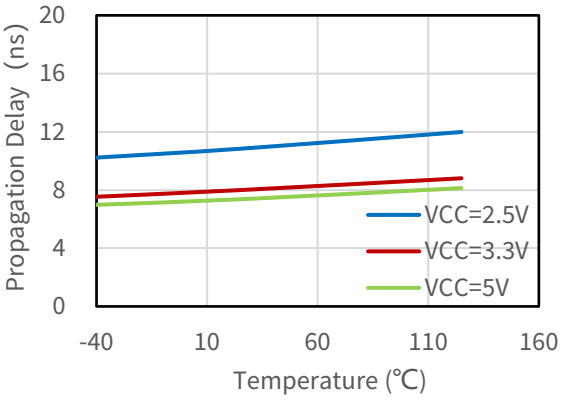


Figure 6.6 NSI822x-DSPR Falling Edge
Propagation Delay Vs Temp

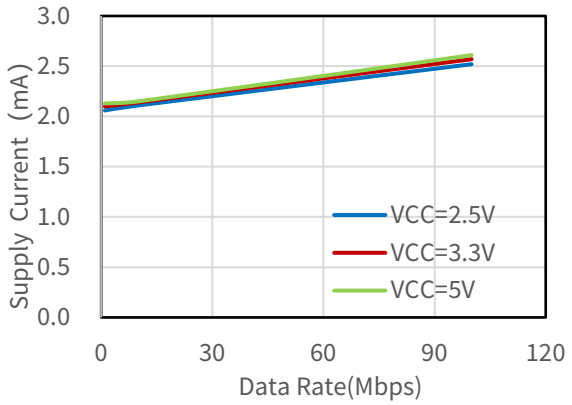


Figure 6.7 NSI8220-DSWVR VDD1 Supply Current vs Data Rate

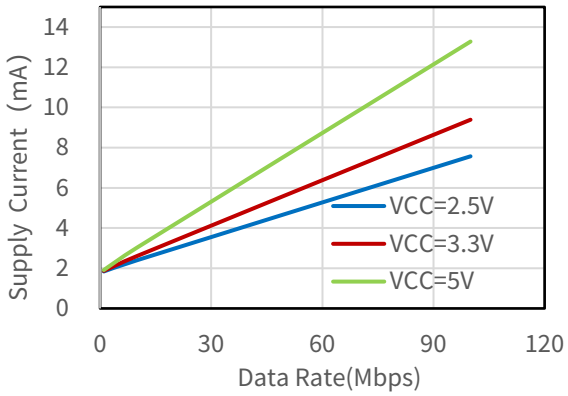


Figure 6.8 NSI8220-DSWVR VDD2 Supply Current vs Data Rate

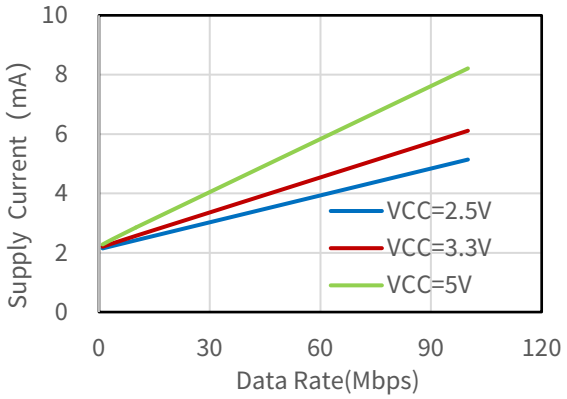


Figure 6.9 NSI8221-DSWVR / NSI8222-DSWVR
VDD1 Supply Current vs Data Rate

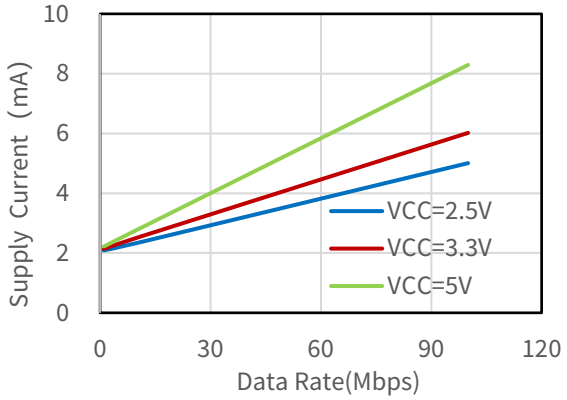


Figure 6.10 NSI8221-DSWVR / NSI8222-DSWVR
VDD2 Supply Current vs Data Rate

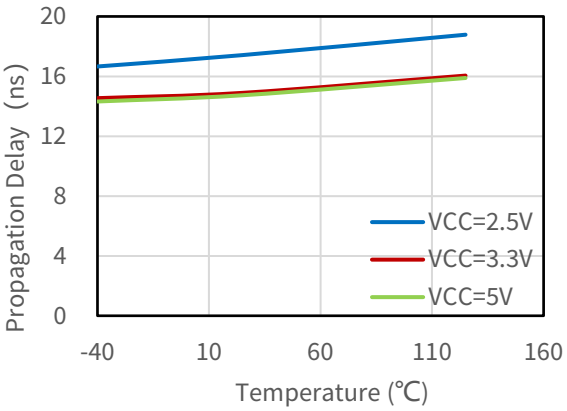


Figure 6.11 NSI822x-DSWVR Rising Edge
Propagation Delay Vs Temp

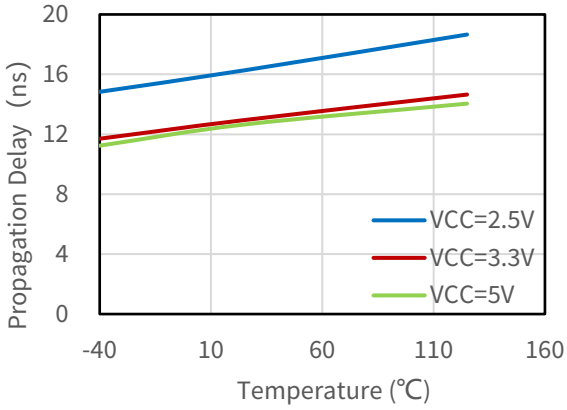
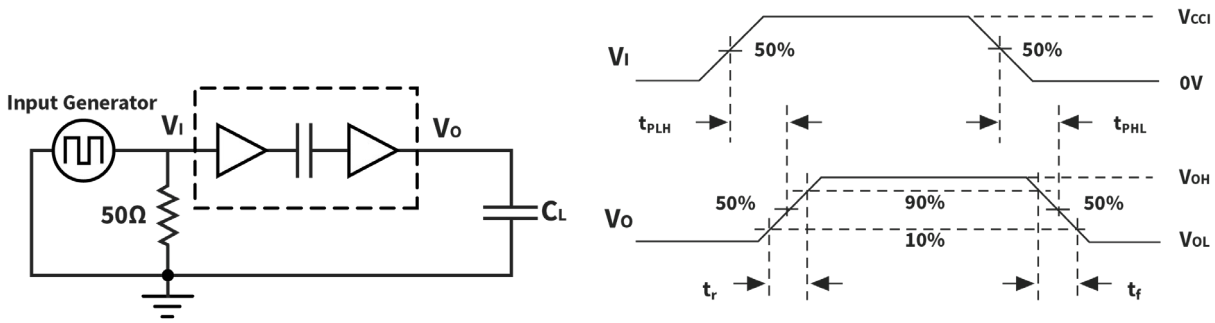


Figure 6.12 NSI822x-DSWVR Falling Edge
Propagation Delay Vs Temp

6.9. Parameter Measurement Information



(1) Input Generator Characteristics : PRR ≤ 50kHz, tr ≤ 3ns, tf ≤ 3ns, Duty cycle = 50%, Zo = 50 Ω.

Figure 6.13 Switching Characteristics Test Circuit and Waveform

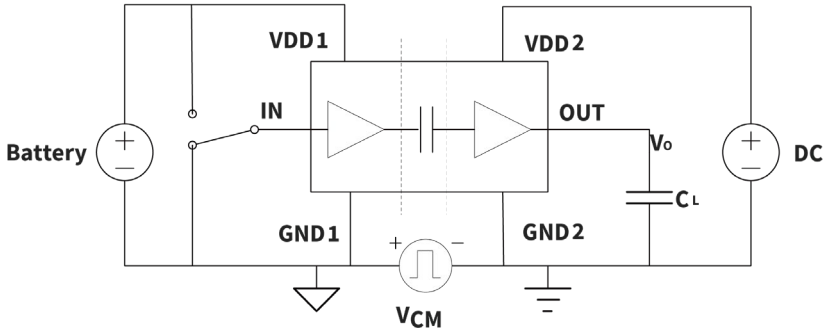


Figure 6.14 Common-Mode Transient Immunity Test Circuit

7. High Voltage Feature Description

7.1. Insulation and Safety Related Specifications

Parameters	*Symbol*	*Value*		*Unit*	*Comments*
		SOP8	*SOW8*		
Minimum External Clearance	CLR	4.0	8.0	mm	IEC 60664-1:2007
Minimum External Creepage	CPG	4.0	8.0	mm	IEC 60664-1:2007
Distance Through Insulation	DTI	10	24	um	
Tracking Resistance (Comparative Tracking Index)	CTI	>600	>600	V	DIN EN 60112 (VDE 0303-11); IEC 60112
Material Group		I	I		IEC 60664-1

Description	Test Condition	Value	
		SOP8	SOW8
Overvoltage Category per IEC60664-1	For Rated Mains Voltage ≤ 150Vrms	Ⅰ to Ⅳ	Ⅰ to Ⅳ
	For Rated Mains Voltage ≤ 300Vrms	Ⅰ to Ⅲ	Ⅰ to Ⅳ
	For Rated Mains Voltage ≤ 600Vrms	Ⅰ to Ⅱ	Ⅰ to Ⅳ
	For Rated Mains Voltage ≤ 1000Vrms	Ⅰ	Ⅰ to Ⅲ
Climatic Classification		40/125/21	40/125/21
Pollution Degree per DIN VDE 0110,		2	2

7.2. Insulation Characteristics

Description	Test Condition	Symbol	Value		Unit
			SOP8	SOW8	
Maximum repetitive isolation voltage		V_{IORM}	565	2121	V_{PEAK}
Maximum Working Isolation Voltage	AC voltage	V_{IOWM}	400	1500	V_{RMS}
	DC voltage		565	2121	V_{DC}
Apparent Charge	Method a, after Input/output safety test subgroup 2/3, $V_{ini}=V_{IOTM}$, t_{ini} = 60s , $V_{pd(m)}=1.2*V_{IORM}$, t_m=10s.	q_{pd}		<5	pC
	Method a, after environmental tests subgroup 1, $V_{ini}=V_{IOTM}$, t_{ini}=60s ,$V_{pd(m)}=1.6*V_{IORM}$, t_m=10s				pC
	Method b, routine test (100% production) and preconditioning (type test);$V_{ini}=1.2*V_{IOTM}$, t_{ini}=1s $V_{pd\ (m)}=1.875*V_{IORM}$, t_m=1s （method b1） or $V_{pd(m)}=V_{ini}$, $t_m=t_{ini}$(method b2)				pC
	Method a, after Input/output safety test subgroup 2/3, $V_{ini}=V_{IOTM}$, t_{ini} = 60s ,	q_{pd}	<5		pC

Description	Test Condition	Symbol	Value		Unit
			SOP8	SOW8	
	$V_{pd(m)}$=1.2*V_{IORM}, t_m=10s.				
	Method a, after environmental tests subgroup 1, V_{ini}=V_{IOTM}, t_{ini}=60s ,$V_{pd(m)}$=1.3*V_{IORM}, t_m=10s				pC
	Method b, routine test (100% production) and preconditioning (type test);V_{ini}=1.2*V_{IOTM}, t_{ini}=1s $V_{pd\ (m)}$=1.5*V_{IORM}, t_m=1s （method b1） or $V_{pd(m)}$=Vini, t_m=t_{ini}(method b2)				pC
Maximum transient isolation voltage	t = 60 sec	V_{IOTM}	5300	8000	V_{PEAK}
Maximum impulse voltage	Tested in air, 1.2/50μs waveform per IEC62368-1	V_{IMP}	5384	6250	V_{PEAK}
Maximum Surge Isolation Voltage	Test method per IEC60065,1.2/50μs waveform, V_{IOSM}≥V_{IMP} × 1.3	V_{IOSM}	7000	10000	V_{PEAK}
Isolation resistance	V_{IO} =500V, T_{amb}=25℃	R_{IO}	>10^{12}	>10^{12}	Ω
	V_{IO} =500V, 100℃ ≤ T_{amb} ≤ 125℃		>10^{11}	>10^{11}	Ω
	V_{IO} =500V, T_{amb}=T_s		>10^{9}	>10^{9}	Ω
Isolation capacitance	f = 1MHz	C_{IO}	0.6	0.6	pF
Withstand Isolation Voltage	V_{TEST} = V_{ISO}, t = 60s (qualification), V_{TEST} = 1.2 × V_{ISO}, t = 1s (100% production test)	V_{ISO}	3750	5000	V_{RMS}

7.3. Safety-Limiting Values

Basic isolation safety-limiting values as outlined in VDE-0884-17 of NSI822x-DSPR SOP8(150mil)

Description	Test Condition	Symbol	Value	Unit
Safety Supply Power	$R_{θJA}$ = 137.7 ℃/W[1)], T_J = 150 ℃, T_A = 25 ℃		908	mW
Safety Supply Current	$R_{θJA}$ = 137.7 ℃/W[1)], V_I = 5.5 V, T_J = 150 ℃, T_A = 25 ℃		165	mA
Safety Temperature[2)]		T_S	150	°C

1) Calculate with the junction-to-air thermal resistance, $R_{\theta JA}$, of SOP8(150mil) package (***Thermal Information Table***) which is that of a device installed on a low effective thermal conductivity test board (1s) according to JESD51-3.
2) The maximum safety temperature has the same value as the maximum junction temperature (T_J) specified for the device.

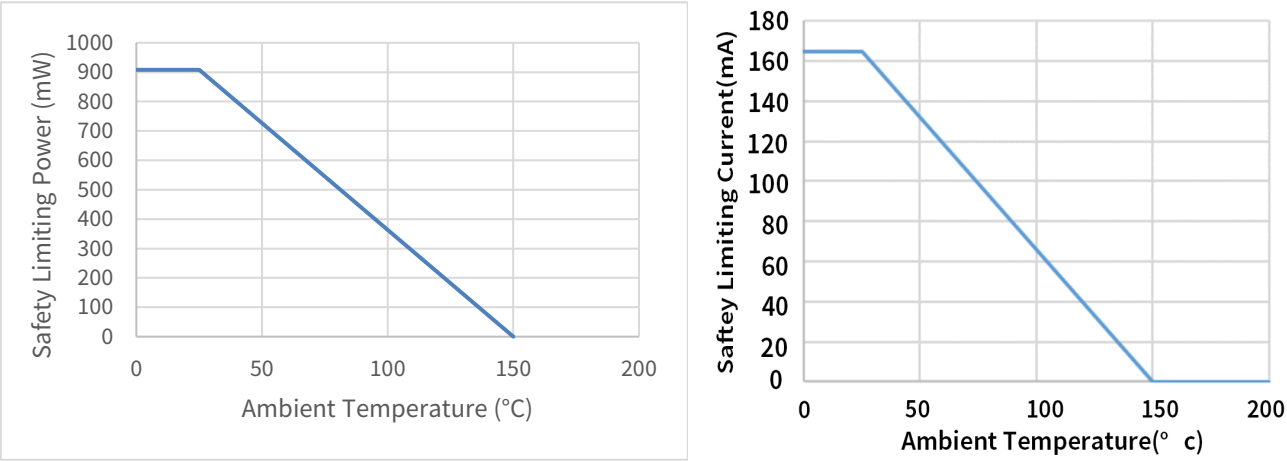


Figure 7.1 NSI822x-DSPR Thermal Derating Curve, Dependence of Safety Limiting Values with Case Temperature per DIN VDE V 0884-17

Reinforced isolation safety-limiting values as outlined in VDE-0884-17 of NSI822x-DSWVR SOW8(300mil)

Description	*Test Condition*	*Symbol*	*Value*	*Unit*
Safety Supply Power	$R_{\theta JA}$ = 84.3 ℃/W[1)], V_I = 5.5 V, T_J = 150 ℃, T_A = 25 ℃		1483	mW
Safety Supply Current	$R_{\theta JA}$ = 84.3 ℃/W[1)], T_J = 150 ℃, T_A = 25 ℃		269.6	mA
Safety Temperature[2)]		T_S	150	°C

1) Calculate with the junction-to-air thermal resistance, $R_{\theta JA}$, of SOW8(300mil) package (***Thermal Information Table***) which is that of a device installed on a low effective thermal conductivity test board (1s) according to JESD51-3.
2) The maximum safety temperature has the same value as the maximum junction temperature (T_J) specified for the device.

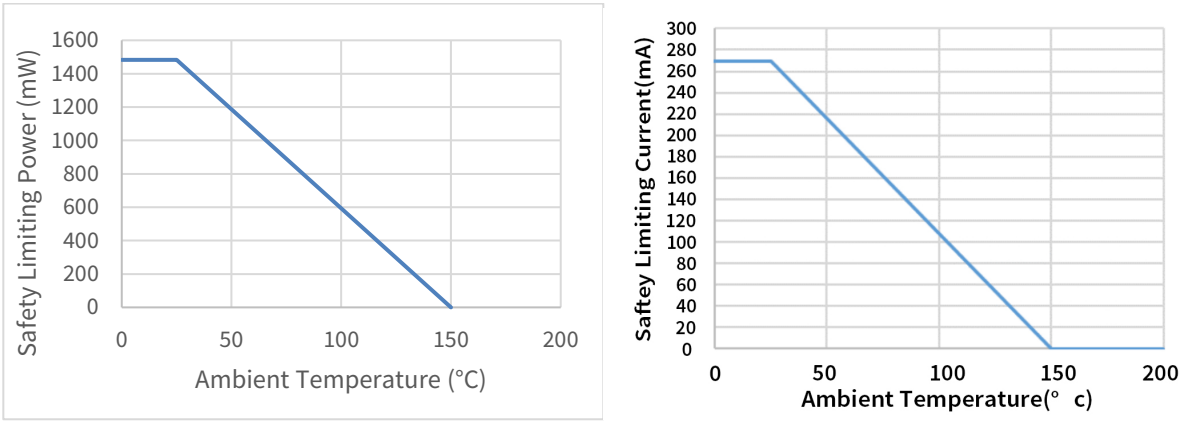


Figure 7.2 NSI822x-DSWVR Thermal Derating Curve, Dependence of Safety Limiting Values with Case Temperature per DIN VDE V 0884-17

7.4. Regulatory Information

The NSI822x-DSPR are approved by the organizations listed in table.

UL		VDE	CQC	TUV
UL 1577 Component Recognition Program	Approved under CSA Component Acceptance Notice 5A	DIN EN IEC 60747-17 (VDE 0884-17)	Certified according to GB4943.1	Certified According to EN IEC 62368-1
Single Protection, 3750V_{rms} Isolation voltage	Single Protection, 3750V_{rms} Isolation voltage	Basic Insulation V_{IORM}=565Vpeak V_{IOTM}=5300Vpeak V_{IOSM}=7000Vpeak	Basic insulation	3000Vrms for 1min
E500602	E500602	40050121	CQC20001264940	R50574061

The NSI822x-DSWVR are approved by the organizations listed in table.

UL		VDE	CQC	TUV
UL 1577 Component Recognition Program	Approved under CSA Component Acceptance Notice 5A	DIN EN IEC 60747-17 (VDE 0884-17)	Certified according to GB4943.1	Certified According to EN IEC 62368-1
Single Protection, 5000V_{rms} Isolation voltage	Single Protection, 5000V_{rms} Isolation voltage	Reinforced Insulation V_{IORM}=2121Vpeak V_{IOTM}=8000Vpeak V_{IOSM}=10000Vpeak	Reinforced insulation	5000Vrms for 1min
E500602	E500602	40052820	CQC20001264938	R50574061

8. Function Description

8.1. Overview

The NSI822x is a Dual-channel digital isolator based on a capacitive isolation barrier technique. The digital signal is modulated with RF carrier generated by the internal oscillator at the Transmitter side. Then it is transferred through the capacitive isolation barrier and demodulated at the Receiver side.

The NSI822x devices are high reliability dual-channel digital isolator. The NSI822x device is safety certified by UL1577 support 5kV$_{rms}$ insulation withstand voltage, while providing high electromagnetic immunity and low emissions at low power consumption. The data rate of the NSI822x is up to 150Mbps, and the common-mode transient immunity (CMTI) is up to 250kV/μs. The NSI822x device provides digital channel direction configuration and the default output level configuration when the input power is lost. Wide supply voltage of the NSI822x device support to connect with most digital interface directly, easy to do the level shift. High system level EMC performance enhance reliability and stability of use.

The NSI822x has a default output status when VDD$_{IN}$ is unready and VDD$_{OUT}$ is ready as shown in Table 8.1, which helps for diagnosis when power is missing at the transmitter side. The output B follows the same status with the input A within 60μs after powering up.

Table 8.1 Output status vs. power status

***Input*[1]**	***VDD$_{IN}$ status***	***VDD$_{OUT}$ status***	***Output***	***Comment***
H	Ready	Ready	H	Normal operation.
L	Ready	Ready	L	
X	Unready	Ready	L(NSI822xx0) H(NSI822xx1)	The output follows the same status with the input within 60μs after input side VDD$_{IN}$ is powered on.
X	Ready	Unready	Undetermined	The output follows the same status with the input within 60μs after output side VDD$_{OUT}$ is powered on.

Note: H=Logic high; L=Logic low; X=Logic low or logic high; Z=High impedance.

VDD$_{IN}$ is input side power; VDD$_{OUT}$ is output side power.

(1) There is a protection diode between the input and the VDD$_{IN}$. When the VDD$_{IN}$ is floating, the strong drive signal through the input pin will put the VDD$_{IN}$ in an indeterminate state.

8.2. OOK Modulation

NSI822x is based on a capacitive isolation barrier technique and the digital signal is modulated with RF carrier generated by the internal oscillator at the transmitter side, as shown in Figure 8.1, then it is transferred through the capacitive isolation barrier and demodulated at the receiver side. The modulation uses OOK modulation technique with key benefits of high noise immunity and low radiation EMI.

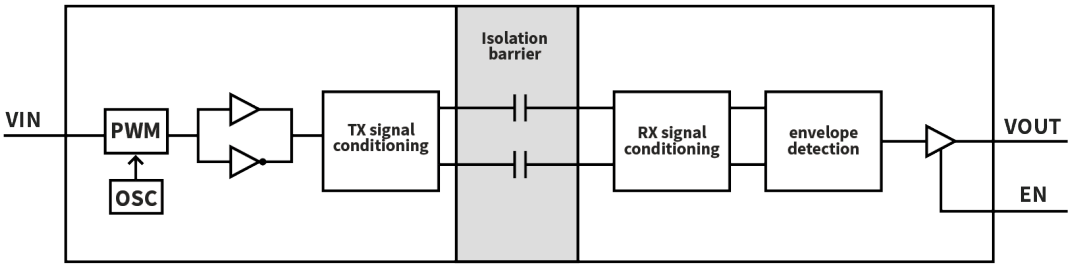


Figure 8.1 Single Channel Function Block Diagram

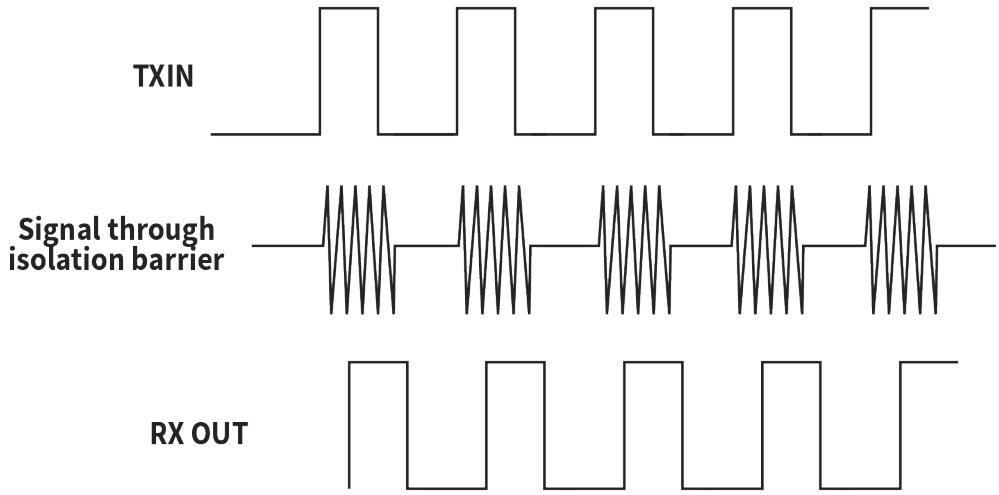


Figure 8.2 OOK Modulation

9. Application Note

9.1. Typical Application Circuit

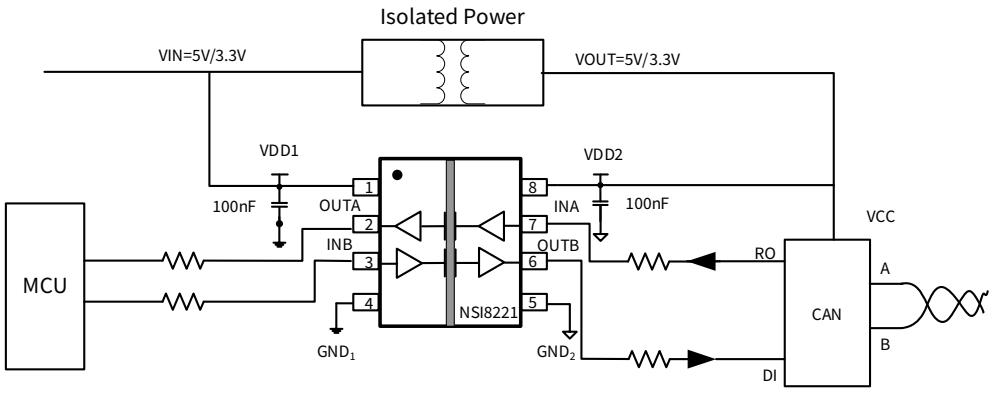


Figure9.1 Typical SCH for ISO CAN Interface

9.2. PCB Layout

The NSI822x requires a 0.1 μF bypass capacitor between VDD1 and GND1, VDD2 and GND2. The capacitor should be placed as close as possible to the package. Figure 9.2 to Figure 9.3 show the recommended PCB layout, make sure the space under the chip should keep free from planes, traces, pads and via. To enhance the robustness of a design, the user may also include resistors (50–300 Ω) in series with the inputs and outputs if the system is excessively noisy. The series resistors also improve the system reliability such as latch-up immunity.

The typical output impedance of an isolator driver channel is approximately 50 Ω, ±40%. When driving loads where transmission line effects will be a factor, output pins should be appropriately terminated with controlled impedance PCB traces.

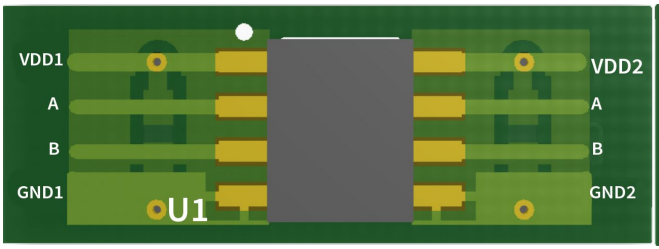


Figure 9.2 Recommended PCB Layout — Top Layer

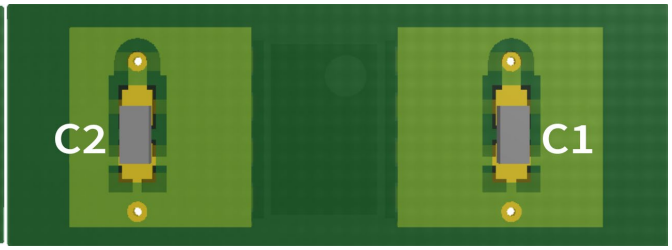


Figure 9.3 Recommended PCB Layout — Bottom Layer

9.3. High Speed Performance

Figure 9.4 shows the eye diagram of NSI822x at 50Mbps data rate output. The result shows a typical measurement on NSI822x with low jitter and wide open eye characteristics.

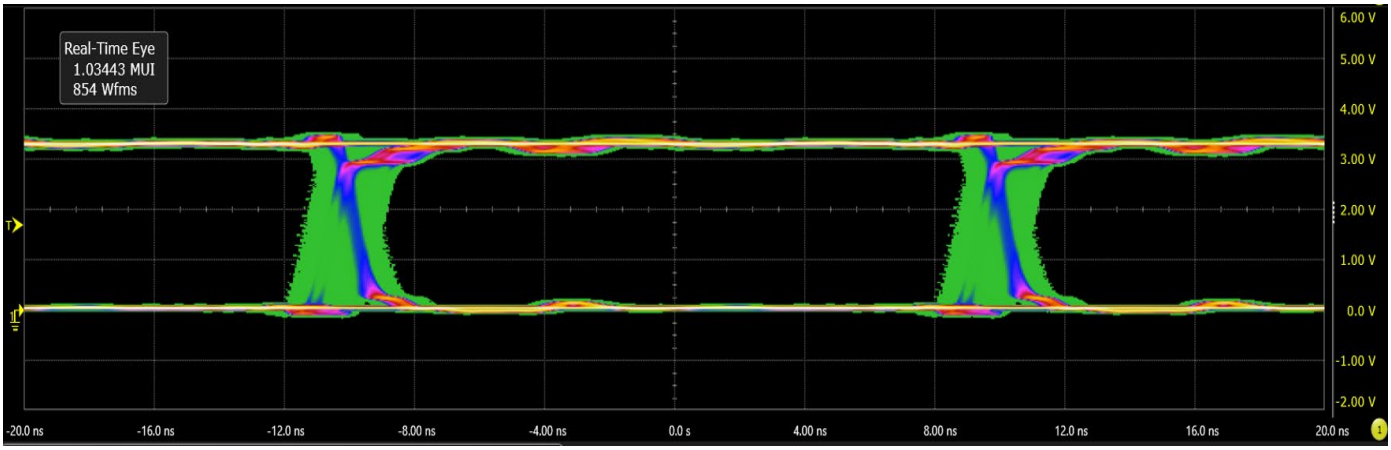
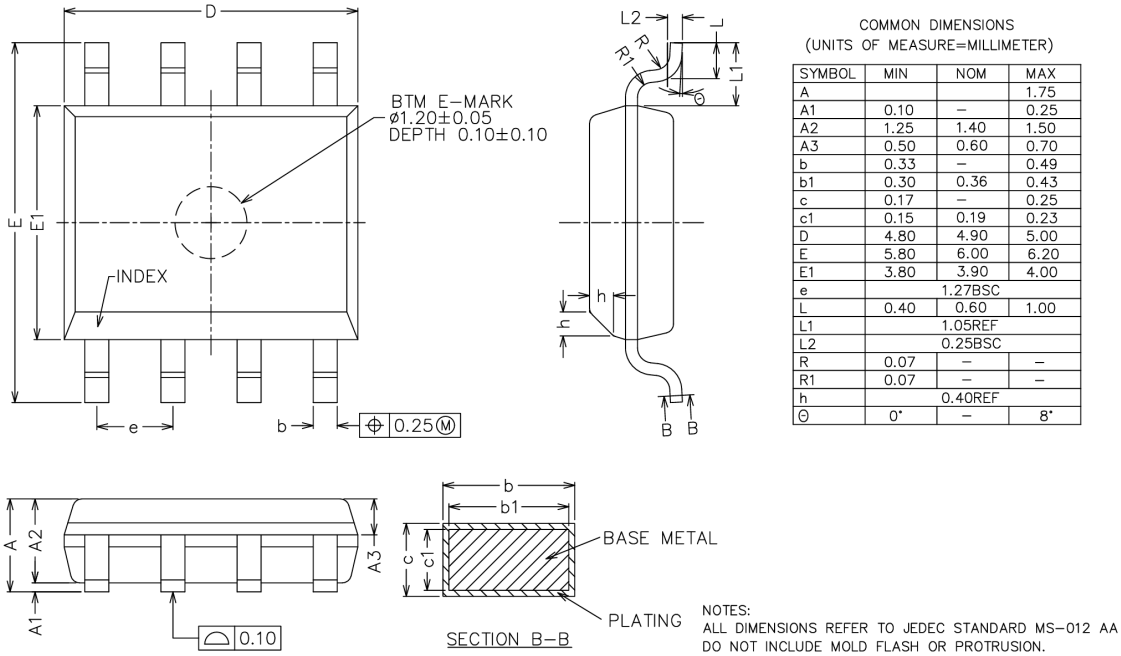


Figure9.4 Eye Diagram at 50Mbps PRBS 2^{16}-1, 2.5V and 25℃

10. Package Information

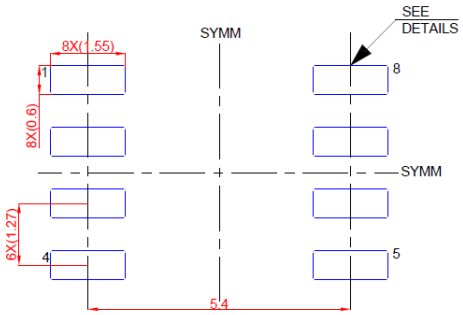


COMMON DIMENSIONS
(UNITS OF MEASURE=MILLIMETER)

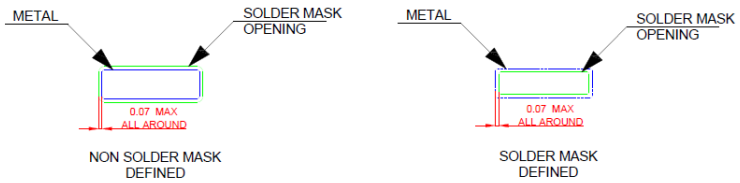
SYMBOL	MIN	NOM	MAX
A			1.75
A1	0.10	–	0.25
A2	1.25	1.40	1.50
A3	0.50	0.60	0.70
b	0.33	–	0.49
b1	0.30	0.36	0.43
c	0.17	–	0.25
c1	0.15	0.19	0.23
D	4.80	4.90	5.00
E	5.80	6.00	6.20
E1	3.80	3.90	4.00
e		1.27BSC	
L	0.40	0.60	1.00
L1		1.05REF	
L2		0.25BSC	
R	0.07	–	–
R1	0.07	–	–
h		0.40REF	
θ	0°	–	8°

NOTE: This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.

Figure 10.1 SOP8 Package Shape and Dimension in millimeters

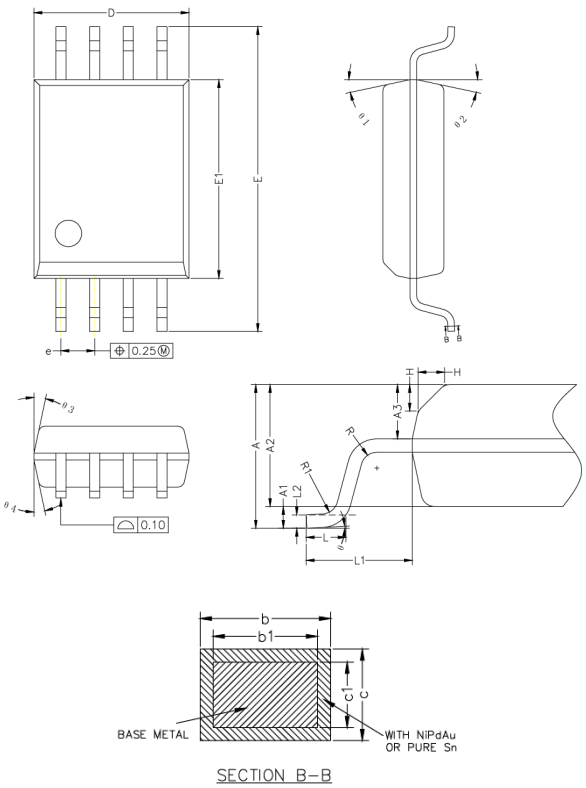


LAND PATTERN EXAMPLE(mm)



SOLDER MASK DETAILS

Figure 10.2 SOP8 Package Board Layout Example



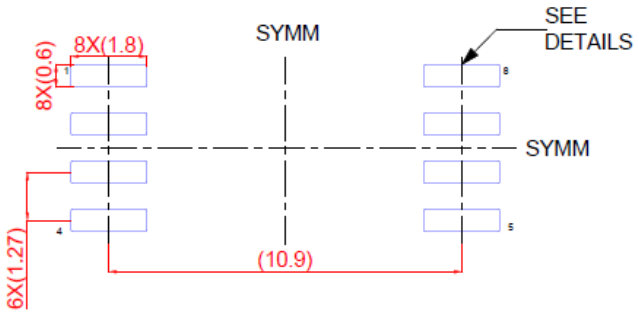
COMMON DIMENSIONS
(UNITS OF MEASURE=MILLIMETER)

SYMBOL		MIN	NOM	MAX
A		–	–	2.85
A1		0.31	0.41	0.51
A2		2.20	2.30	2.40
A3		0.97	1.02	1.07
b	PURE Sn	0.33	–	0.47
	NiPdAu	0.31	–	0.51
b1		0.29	–	0.43
c	PURE Sn	0.22	–	0.35
	NiPdAu	0.13	–	0.33
c1		0.11	–	0.31
D		5.75	5.85	5.95
E		11.25	11.50	11.75
E1		7.40	7.50	7.60
e			1.27BSC	
H			0.50REF	
L		0.50	–	1.00
L1			2.00REF	
L2			0.25BSC	
R			0.07REF	
R1			0.07REF	
θ		0°	–	8°
θ 1			12°REF	
θ 2			12°REF	
θ 3			12°REF	
θ 4			12°REF	

NOTES:
1. ALL DIMENSIONS DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS.

NOTE: This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.

Figure 10.3 SOW8 Package Shape and Dimension in millimeters



LAND PATTERN EXAMPLE(mm)
9.1 mm NOMINAL
CLEARANCE/CREEPAGE

SOLDER MASK DETAILS

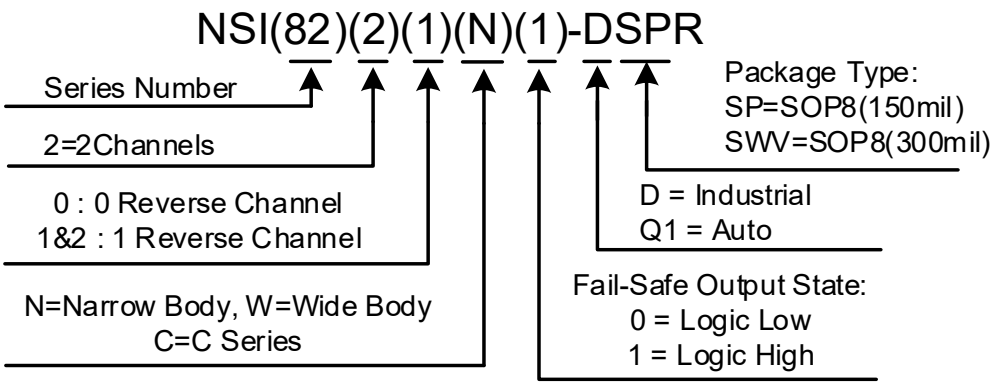
Figure 10.4 SOW8 Package Board Layout Example

11. Order Information

Part Number	Isolation Rating (kV)	Number of side 1 inputs	Number of side 2 inputs	Max Data Rate (Mbps)	Default Output State	Temperature	MSL	Package Type	Package Drawing	SPQ
NSI8220N0-DSPR	3.75	2	0	150	Low	-55 to 125℃	3	SOP8 (150mil)	SOP8	2500
NSI8220N1-DSPR	3.75	2	0	150	High	-55 to 125℃	3	SOP8 (150mil)	SOP8	2500
NSI8221N0-DSPR	3.75	1	1	150	Low	-55 to 125℃	3	SOP8 (150mil)	SOP8	2500
NSI8221N1-DSPR	3.75	1	1	150	High	-55 to 125℃	3	SOP8 (150mil)	SOP8	2500
NSI8222N0-DSPR	3.75	1	1	150	Low	-55 to 125℃	3	SOP8 (150mil)	SOP8	2500
NSI8222N1-DSPR	3.75	1	1	150	High	-55 to 125℃	3	SOP8 (150mil)	SOP8	2500
NSI8220C0-DSPR	3.75	2	0	150	Low	-55 to 125℃	3	SOP8 (150mil)	SOP8	2500
NSI8220C1-DSPR	3.75	2	0	150	High	-55 to 125℃	3	SOP8 (150mil)	SOP8	2500
NSI8221C0-DSPR	3.75	1	1	150	Low	-55 to 125℃	3	SOP8 (150mil)	SOP8	2500
NSI8221C1-DSPR	3.75	1	1	150	High	-55 to 125℃	3	SOP8 (150mil)	SOP8	2500
NSI8222C0-DSPR	3.75	1	1	150	Low	-55 to 125℃	3	SOP8 (150mil)	SOP8	2500
NSI8222C1-DSPR	3.75	1	1	150	High	-55 to 125℃	3	SOP8 (150mil)	SOP8	2500
NSI8220W0-DSWVR	5	2	0	100	Low	-55 to 125℃	3	SOW8 (300mil)	SOW8	1000
NSI8220W1-DSWVR	5	2	0	100	High	-55 to 125℃	3	SOW8 (300mil)	SOW8	1000
NSI8221W0-DSWVR	5	1	1	100	Low	-55 to 125℃	3	SOW8 (300mil)	SOW8	1000
NSI8221W1-DSWVR	5	1	1	100	High	-55 to 125℃	3	SOW8 (300mil)	SOW8	1000
NSI8222W0-DSWVR	5	1	1	100	Low	-55 to 125℃	3	SOW8 (300mil)	SOW8	1000
NSI8222W1-DSWVR	5	1	1	100	High	-55 to 125℃	3	SOW8 (300mil)	SOW8	1000
NSI8220C0-DSWVR	5	2	0	100	Low	-55 to 125℃	3	SOW8 (300mil)	SOW8	1000
NSI8220C1-DSWVR	5	2	0	100	High	-55 to 125℃	3	SOW8 (300mil)	SOW8	1000
NSI8221C0-DSWVR	5	1	1	100	Low	-55 to 125℃	3	SOW8 (300mil)	SOW8	1000
NSI8221C1-DSWVR	5	1	1	100	High	-55 to 125℃	3	SOW8 (300mil)	SOW8	1000
NSI8222C0-DSWVR	5	1	1	100	Low	-55 to 125℃	3	SOW8 (300mil)	SOW8	1000

Part Number	Isolation Rating (kV)	Number of side 1 inputs	Number of side 2 inputs	Max Data Rate (Mbps)	Default Output State	Temperature	MSL	Package Type	Package Drawing	SPQ
NSI8222C1-DSWVR	5	1	1	100	High	-55 to 125℃	3	SOW8 (300mil)	SOW8	1000
NOTE: All packages are RoHS-compliant with peak reflow temperatures of 260 ℃ according to the JEDEC industry standard classifications and peak solder temperatures.										

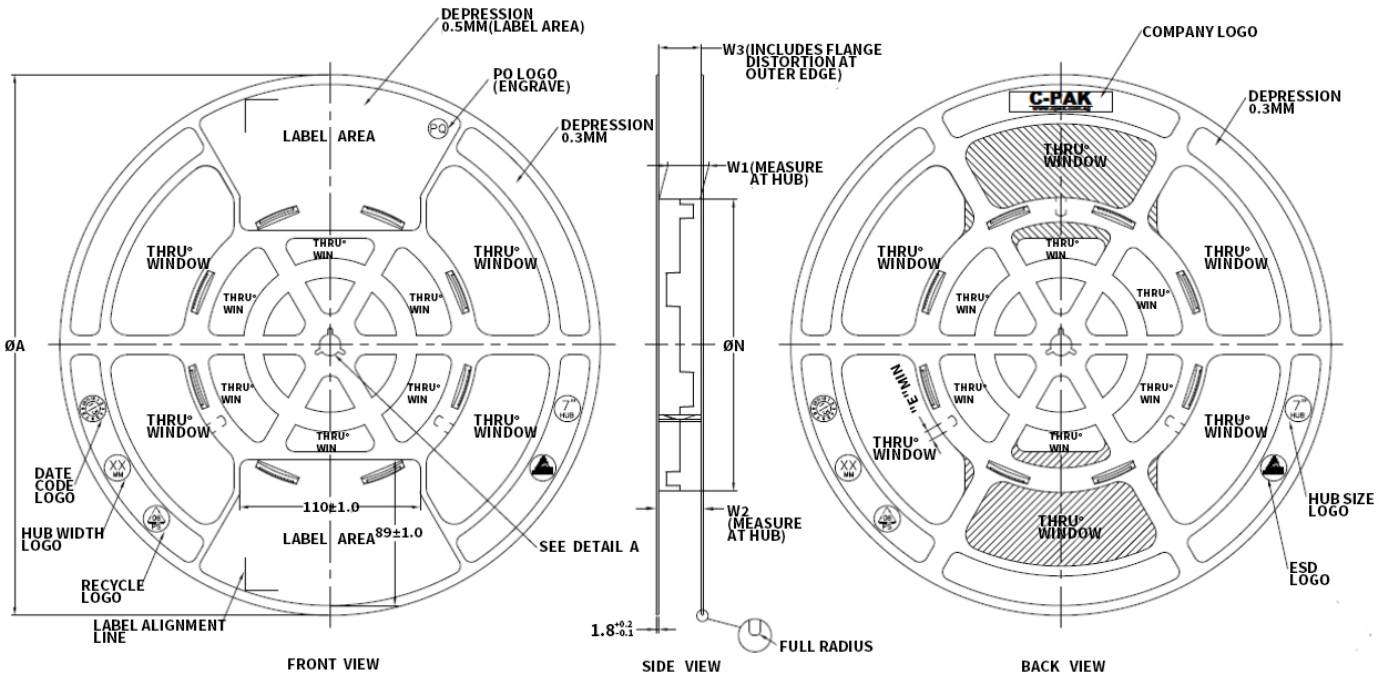
Part Number Rule:

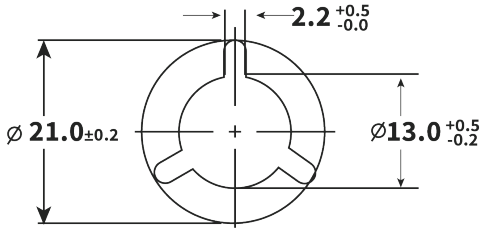


12. Documentation Support

Part Number	Product Folder	Datasheet	Technical Documents	Isolator selection guide
NSI822x	tbd	tbd	tbd	tbd

13. Tape and Reel Information



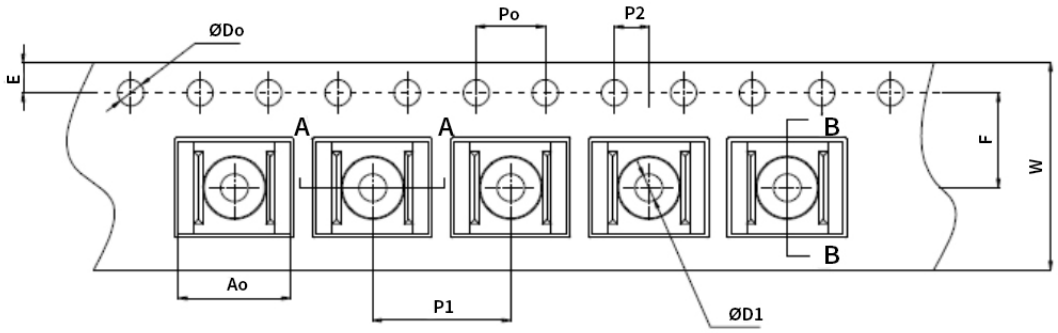


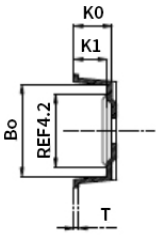
ARBOR HOLE
DETAIL A
SCALE: 3:1

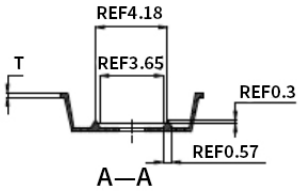
PRODUCT SPECIFICATION						
TAPE WIDTH	ØA ±2.0	ØN ±2.0	W1	W2 (Max)	W3	E (MIN)
08MM	330	178	8.4 +1.5 -0.0	14.4	SHALL ACCOMMODATE TAPE WIDTH WITHOUT NTERFERENCE	5.5
12MM	330	178	12.4 +2.0 -0.0	18.4		5.5
16MM	330	178	16.4 +2.0 -0.0	22.4		5.5
24MM	330	178	24.4 +2.0 -0.0	30.4		5.5
32MM	330	178	32.4 +2.0 -0.0	38.4		5.5

SURFACE RESISTIVITY			
LEGEND	SR RANGE	TYPE	COLOUR
A	BELOW 10^{12}	ANTISTATIC	ALL TYPES
B	10^{6} TO 10^{11}	STATIC DISSIPATIVE	BLACK ONLY
C	10^{5} & BELOW 10^{5}	CONDUCTIVE(GENERIC)	BLACK ONLY
E	10^{9} TO 10^{11}	ANTISTATIC(COATED)	ALL TYPES

Figure 13.1 Reel Information (for all packages)







Common size

Appearance	Size(mm)
E	1.75±0.10
F	5.5±0.10
P2	2.00±0.10
D0	1.55±0.05
D1	1.6±0.10
P0	4.00±0.10
10P0	40.00±0.20

Pocket size

Appearance	Size(mm)
W	12.00±0.30
P_1	8.00±0.10
A_o	6.50±0.10
B_o	5.30±0.10
K_o	2.20±0.10
K_1	1.90±0.10
T	0.30±0.05

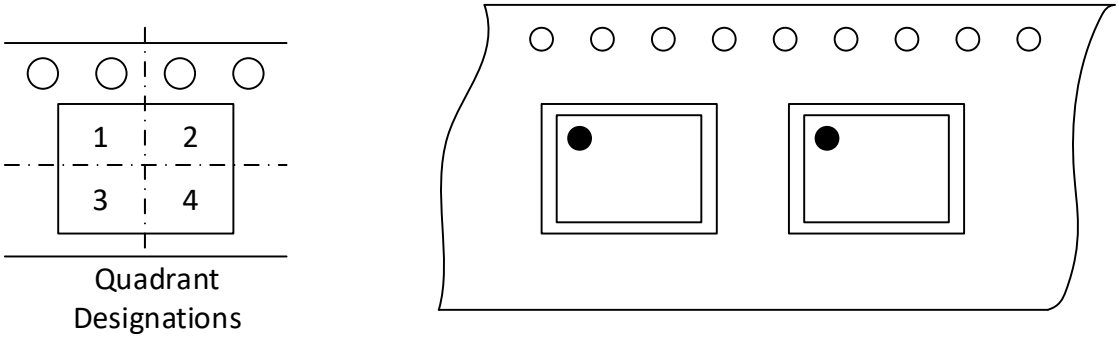
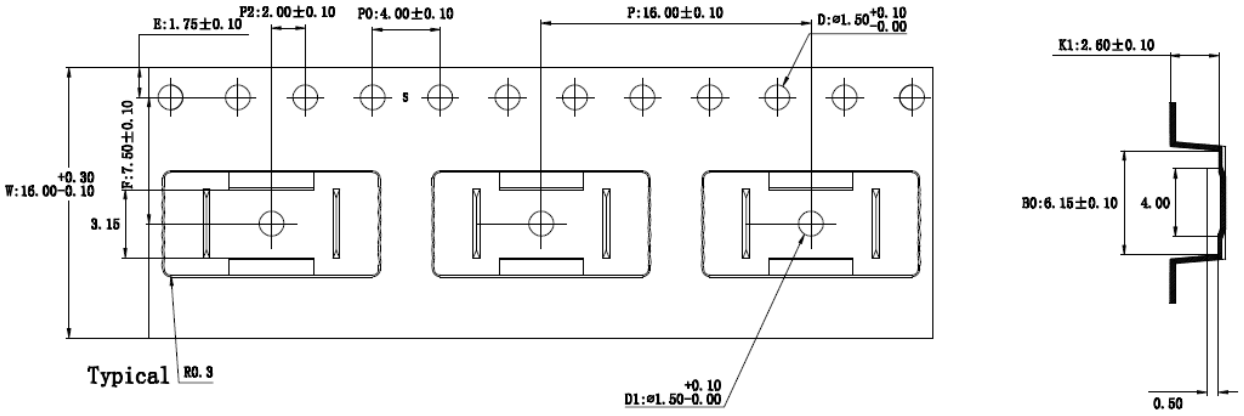


Figure 13.2 Tape Information of SOP8(150mil)



技术要求：
Technical Requirements:

1. 每10个料带链孔径累计公差为±0.20毫米。
   10 sprocket hole pitch cumulative toleran±0.20mm
2. 料带弯曲每250毫米不可超过1毫米。
   Carrier camber is within 1 mm in 250 mm
3. 所有尺寸符合EIA-481-D标准要求。
   All dimensions meet EIA-481-D requirements

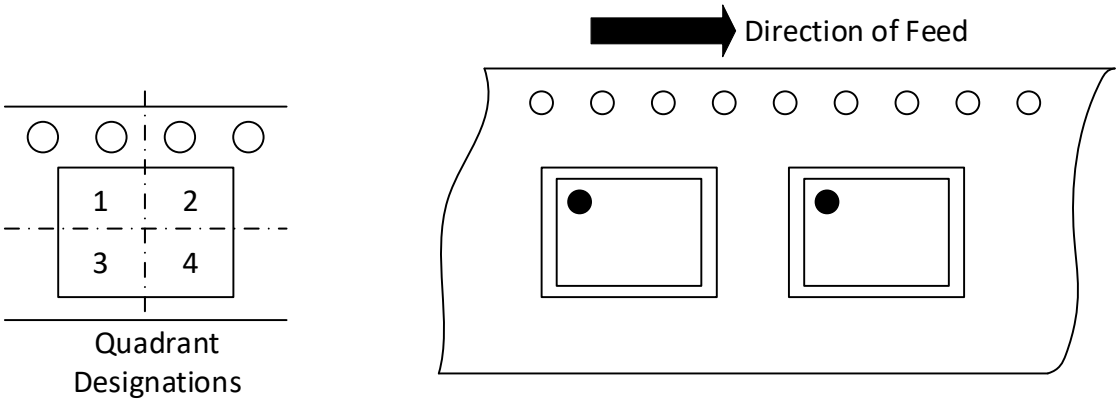


Figure 13.3 Tape Information of SOW8(300mil)

14. Revision History

Revision	Description	Date
1.0	Initial version	2019/12/20
1.1	Update SOW8 package PIN description	2020/6/23
1.2	Changed tape and reel information	2021/2/4
1.3	Operating temperature support -55 to 125 ℃	2021/7/7
1.4	Update SOWW16 package	2021/12/5
1.5	Update Package Board Layout Example. Changed AEC-Q100 description.	2022/4/16
1.6	Update SOWW16 MSL, Pin Configuration and VISO.	2022/9/30
1.7	Correct formatting and images. Update Safety certification info throughout the document. Update Package Information and Tape and Reel Information. Update Function Description.	2024/8/23
1.8	Correct formatting and images. Update Input characteristics. Update eye diagram.	2025/1/13
2.0	Delete SOW16(300mil)/SOWW16(600mil) package products. Delete typical supply current equations. Update electrical characteristics of SOP8(150mil) and SOW8(300mil) products. Update supply current characteristics at 2.5V/3.3V/5V. Update switching characteristics at 2.5V/3.3V/5V. Add NSI822xCx products. Add AMR description. Add ESD ratings description. Add Ψ_{JT} and Ψ_{JB} into thermal information. Update eye diagram. Update package information of SOP8(150mil) and SOW8(300mil) products. Update order information. Change the MSL level to 3. Update part number rule.	2025/11/25

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