JWH7295

IEEE 802.3at Compliant 8 Channel Power Sourcing Equipment Converter

DESCRIPTION

The JWH7295 is a highly integrated, IEEE 802.3at-compliant Power Sourcing Equipment converter. The JWH7295 is designed to power compliant 802.3af and 802.3at PDs. It contains eight low R_{DSON} high-voltage MOSFET, each with an accurate, lossless internal current sense and an onboard MCU. It significantly reduces the complexity of Power over Ethernet designs while easing PCB layout.

The JWH7295 includes an I^2C serial interface operable up to 1MHz. The advanced power management features include current and voltage read-back and programmable over current (I_{CUT}) and current limit (I_{LIM}) thresholds.

JWH7295 guarantees robustness with all possible fault conditions and over loads.

The JWH7295 is available in a space-saving 56-pin QFN (8mm × 8mm) package.

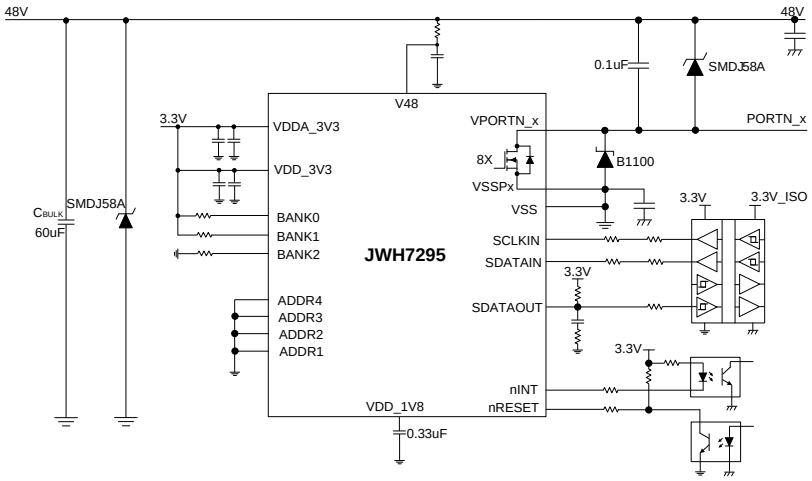
FEATURES

- Fully Compliant IEEE 802.3at Type 1 and 2 PSE
- Can Work Together with JWH7295FW without Requiring a MCU
- Low Power Path Dissipation per Channel 200mΩ MOSFET R_{DSON}
- Very High Reliability Four Point PD Detection
- Continuous, Dedicated Per-Channel Voltage and Current Monitoring
- 1MHz I^2C Compatible Serial Control Interface
- I^2C Programmable PD Power Up to 35W
- Over-Temperature Protection
- Available in QFN8*8-56 Package
- In Conformity with IEC 62368-1:2018

APPLICATIONS

- Routers and Switches for Enterprise and Commercial Markets

TYPICAL APPLICATION



ORDER INFORMATION

DEVICE[1)]	PACKAGE	TOP MARKING[2)]	ENVIRONMENTAL[3)]
JWH7295QFNV#TA	QFN8*8-56	JWH7295 YW□□□□□	Green

Notes:

1) JW□□□□#TA
- Tray
- Package Code
- Part No.

2) Line1: JW □□□□□
- Product code
- JoulWatt LOGO

Line2: YW □□□□□
- Lot number
- Week code
- Year code

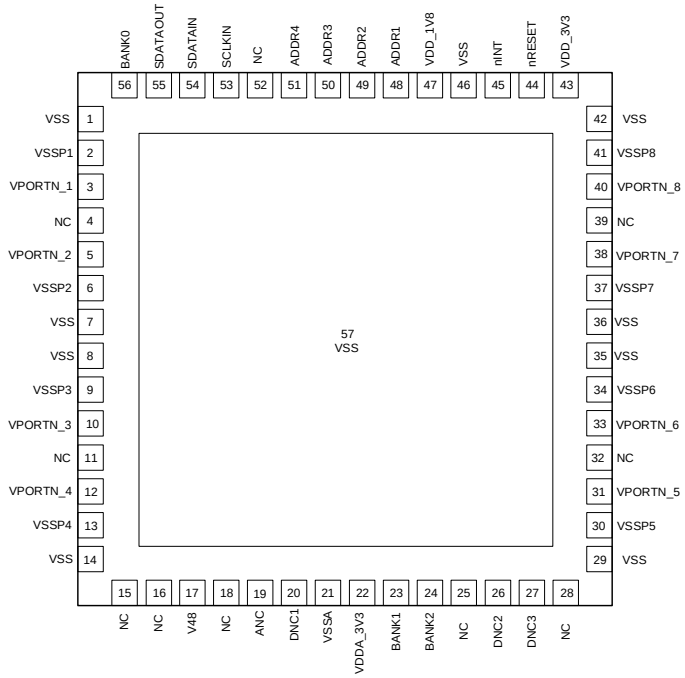
3) All JoulWatt products are packaged with Pb-free and Halogen-free materials and compliant to RoHS standards.

DEVICE INFORMATION

DEVICE	PACKAGE	MSL	STATUS
JWH7295QFNV#TA	QFN8*8-56	MSL3	Available

PIN CONFIGURATION

TOP VIEW



ABSOLUTE MAXIMUM RATING[1)]

V48 Pin……..……..……-0.3V to 80V
VPORTN_1, VPORTN_2, VPORTN_3, VPORTN_4 ……..……..……..…-0.3V to 80V
VPORTN_5, VPORTN_6, VPORTN_7, VPORTN_8……..……..……..…-0.3V to 80V
VDD_3V3, VDDA_3V3 Pin...…….....-0.3V to 6.5V
VDD_1V8 Pin...…….....-0.3V to 2.3V
BANKn, nRESET, nINT, ADDRn..……..... -0.3V to 6.5V
SCLKIN, SDATAIN, SDATAOUT…..…….....……..…-0.3V to 6.5V
ANC, DNC1, DNC2, DNC3…..…….....……..…-0.3V to 6.5V
Junction Temperature[2) 3)] 150ºC
Lead Temperature 260ºC
Storage Temperature ..... -65ºC to +150ºC
ESD Rating (Charged-Device Model, CDM).....±500V

RECOMMENDED OPERATING CONDITIONS[3)]

Supply Voltage Range (V48)……..…….……44V to 60V
Operation Junction Temperature (T_J) …..-40ºC to +125ºC

THERMAL PERFORMANCE[4)]

	θ_{JA}	θ_{JB}	θ_{Jc}
QFN8*8-56	25.3ºC/W	6.2 ºC/W	0.5ºC/W

Notes:

1) Exceeding these ratings may damage the device. These stress ratings do not imply function operation of the device at any other conditions beyond those indicated under RECOMMENDED OPERATING CONDITIONS.

2) The JWH7295 includes thermal protection that is intended to protect the device in overload conditions. Continuous operation over the specified absolute maximum operating junction temperature may damage the device.

3) The device is not guaranteed to function outside of its operating conditions.

4) Measured on JESD51-7, 4-layer PCB.

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range(-40°C to 85°C), otherwise specifications are at T_A=25 ℃. V48=54V, and VDD_3V3=VDDA_3V3=3.3V unless otherwise noted.

Item	Symbol	Condition		Min.	Typ.	Max.	Units
V_{48} Undervoltage Lock-out	V_{48_UVLO}	20h[7:0]=0xAA, Rising	●	44	45	46	V
		20h[7:0]=0xAA, Falling	●	43	44	45	V
V_{DD} Undervoltage Lock-out	V_{DD_UVLO}	Rising	●	2.4	2.55	2.9	V
		Falling	●	1.9	2.2	2.5	V
Internal Regulator Supply Voltage	V_{1V8}	V_{DD_3V3}=2.0V	●	1.7	1.8	1.9	V
V_{48} Supply Current	I_{48}	V_{48} = 54V	●		1.2	3	mA
V_{DD} Supply Current	I_{DD}	V_{DD} = 3.3V	●		3	10	mA
Detection							
Detection Voltage Compliance	V_{OC}	V48-V_{PORTN_x}, Open Port	●	10	11	12	V
Detection Current – Force Current	I_1	First Point	●	215	240	265	μA
	I_2	Second Point	●	135	160	185	μA
Detection Current – Force Voltage	V_1	Third Point	●	7	8	9	V
	V_2	Forth Point	●	3.4	4	5	V
Detection Current Compliance	I_{DETMAX}	V48-V_{PORTN_x} = 0V	●	1	1.2	1.5	mA
Min. Valid Signature Resistance	R_{MIN}		●	16	17	18	KΩ
Max. Valid Signature Resistance	R_{MAX}		●	30.5	32	33.5	KΩ
Valid Signature Capacitance[5)]	C_{Good}			0		650	nF
Invalid Signature Capacitance[5)]	C_{Bad}			10		50	μF
Shorted Port Reject Signature Resistance[5)]	R_{Short}				1		KΩ
Low Reject Signature Resistance[5)]	R_{Low}			1.1		15	KΩ
Open Port Signature Resistance[5)]	R_{Open}			50			KΩ
Detection Voltage Read Back							
Resolution[5)]					16		Bits
Full Scale[5)]					20		V
LSB Weight[5)]					1.22		mV/LSB
ADC Sampling Time[5)]					2.5		ms
Classification							
PSE Classification Voltage	V_{CLASS}	V48-V_{PORTN_x}, 0.1mA ≤ I_{CLASS} ≤ 50mA	●	15.5	18	20.5	V
Classification Event Current Limit	I_{CLASS_LIM}		●	60	75	90	mA
PSE Mark Event Voltage	V_{MARK_PSE}	V48-V_{PORTN_x}, 0.1mA ≤ I_{CLASS} ≤ 5mA	●	7.5	9	10	V
Mark Event Current Limit	I_{MARK_LIM}	V_{PORTN_x} = V48	●	30	40	50	mA
Classification Threshold Current	$I_{CLASS0-1}$	Class 0 - 1	●	5.1	6.5	7.9	mA
	$I_{CLASS1-2}$	Class 1 - 2	●	13.1	14.5	15.9	mA

	$I_{CLASS2-3}$	Class 2 - 3	●	21.1	23	24.9	mA
	$I_{CLASS3-4}$	Class 3 - 4	●	31.1	33	34.9	mA
Classification Current Read Back							
Resolution[5]					16		bits
Full Scale[5]					85		mA
LSB Weight[5]					5.19		μA/LSB
ADC Sampling Time[5]					2.5		ms
ADC Measurement Accuracy[5]				-3		3	mA
Power MOSFET R_{DSON}							
MOS R_{DSON}	R_{ON}				200		mΩ
Output Voltage Sense							
Power Good Threshold Voltage	V_{PG}	V_{PORTN_x}	●	2	2.4	2.8	V
VPORTN_x PIN Pull Up Resistance	R_{PU}				115		kΩ
Current Sense							
2-Pair Overcurrent Threshold, Single-Signature PD	I_{CUT_2P}	Class 1, CUTn[7:0] = C7h	●		109.4		mA
		Class 2, CUTn[7:0] = CAh	●		156.3		
		Class 3, CUTn[7:0] = D8h	●		375		
		Class 4, CUTn[7:0] = EAh	●		656.3		
2-Pair Overcurrent Threshold, Dual-Signature PD	I_{CUT_2P}	Class 1, CUTn[7:0] = C7h	●		109.4		mA
		Class 2, CUTn[7:0] = CAh	●		156.3		
		Class 3, CUTn[7:0] = D8h	●		375		
		Class 4, CUTn[7:0] = EAh	●		656.3		
4-Pair Overcurrent Threshold, Single-Signature PD	I_{CUT}	Class 1, 76h[7:0] = 0x07	●		109.4		mA
		Class 2, 76h[7:0] = 0x0A	●		156.3		
		Class 3, 76h[7:0] = 0x18	●		375		
		Class 4, 76h[7:0] = 0x2A	●		656.3		
2-Pair Current Limit	I_{LIM_2P}	Class1-Class3, LIMn[7:0]=0x20		400	425	450	mA
2-Pair Inrush Current Limit	I_{INRUSH_2P}	Iinrush[1:0]=1		404	425	446	mA
		Iinrush[1:0]=2		808	850	892	
		Iinrush[1:0]=3		1212	1275	1338	
MPS hold current threshold	I_{HOLD_2P}	mps[1:0]=1	●	2	3.5	5	mA
		mps[1:0]=2	●	3	4.5	6	
		mps[1:0]=3	●	4	6.5	8	
Short-Circuit Threshold[5]	V_{SC}	V_{PORTN_x}			0.8		V
Short-Circuit Foldback Current[5]	I_{SC}	I_{PORTN_x}				200	mA
UL2367 Protective Current Rating[5]					1.6		A
Port Current Read Back							
Resolution[5]					16		bits
Full Scale[5]					2		A

LSB Weight[5]					30.5		μA/ LSB
ADC Sampling Time[5]					1		ms
Port Voltage Read Back							
Resolution[5]					16		bits
Full Scale[5]					64		V
LSB Weight[5]		V48-V_{PORTN_x}			0.9766		mV/LSB
ADC Sampling Time[5]					1		ms
ADC Measurement Accuracy[5]				-1.5		1.5	V
Digital Interface							
Digital Input Low Voltage	V_{ILD}	V_{DD} =3.0V ADDRn, BANKn, nRESET SCLIN, SDAIN	•			1	V
Digital Input High Voltage	V_{IHD}	V_{DD} =3.0V ADDRn, BANKn, nRESET SCLIN, SDAIN	•	2.2			V
Digital Output Low Voltage	V_{OLD}	I_{SDAOUT} =3mA, I_{INT}=3mA	•			0.4	V
		I_{SDAOUT} =5mA, I_{INT}=5mA	•			0.7	
Internal Pull Up to VDD		SDAIN, SDAOUT, SCLIN, nINT		90	140		kΩ
Internal Pull Up to VDD		ADDRn		25	45		kΩ
Internal Pull Up to VDD		nRESET		130	180		
Internal Pull Down to GND		BANKn		100	150		kΩ
Capacitive Load for Each Bus Line[5]	C_b					400	pF
Timing							
Detection Backoff Time[5]	$t_{BACKOFF}$			220	250	280	ms
First Long Class Event Duration[5]	t_{LCE}			88	96	105	ms
Class Event Duration[5]	t_{CLE}			6	12	20	ms
Mark Event Duration[5]	t_{ME}			6	9	12	ms
Turn On Rise Time[5]	t_{RISE}	V48-V_{PORTN_x}: 10% to 90% of V48, C_{PORT}=0.1μF		15	24		μs
Turn On Ramp Rate[5]	S_{RR}	C_{PORT}=0.1μF				10	V/μs
Fault Delay[5]	t_{ED}	From tcut/ tlim/ tstart/ tdis Fault to Next Detection		1	1.3	2	s
Midspan Mode Detection Backoff[5]	t_{dbo}			2.3	2.5	2.7	s
Maximum Current Limit Duration During Port Start-Up[5]	t_{START}	tconf[5:4] = 0x0		52	60	66	ms
Maximum Current Limit Duration After Port Start-Up[5]	t_{LIM}	tlim12 = tlim34 = 0x00		52	60	66	ms
Maximum Overcurrent Duration After Port Start-Up[5]	t_{CUT}	tconf[3:2] = 0x0		52	60	66	ms
Maintain Power Signature (MPS) Pulse Width Sensitivity[5]	t_{MPS}	80h[1:0]=0x0		4	5	6	ms
Maintain Power Signature (MPS) Dropout Time[5]	t_{DIS}	tconf[1:0] = 0x0		320	360	400	ms

Port Shut Down Delay[5]	t_{BANK}					50	μs
I²C Watchdog Timer Duration[5]	t_{WD}			2	2.5	3	s
Minimum Pulse Width for nRESET[5]	t_{RST}			1			μs
I²C Timing							
Clock Frequency[5]	t_{CLK}					1	MHz
Bus Free Time[5]	t_1			480			ns
Start Hold Time[5]	t_2			240			ns
SCL Low Time[5]	t_3			480			ns
SCL High Time[5]	t_4			240			ns
Data Hold Time[5]	t_5	Data Into Chip		60			ns
		Data Out of Chip				120	ns
Data Set-Up Time[5]	t_6			80			ns
Start Set-Up Time[5]	t_7			240			ns
Stop Set-Up Time[5]	t_8			240			ns
SCL, SDAIN Rise Time[5]	t_r					120	ns
SCL, SDAIN Fall Time[5]	t_f					60	ns
Fault Present to $\overline{INT}$ Pin Low[5]						150	ns
Stop Condition to $\overline{INT}$ Pin Low[5]						1.5	μs
SCL Fall to ACK Low[5]						120	μs
Protection							
Over Temperature Warning[5]	T_{OTW}				140		℃
Over Temperature Warning Hysteresis[5]					8		℃
Global Over Temperature Protection Threshold[5]	T_{OTP}			150		175	℃
Global Over Temperature Protection Hysteresis[5]					20		℃
Port Temperature Protection Threshold[5]	T_{port_OTP}				215		℃

Note:

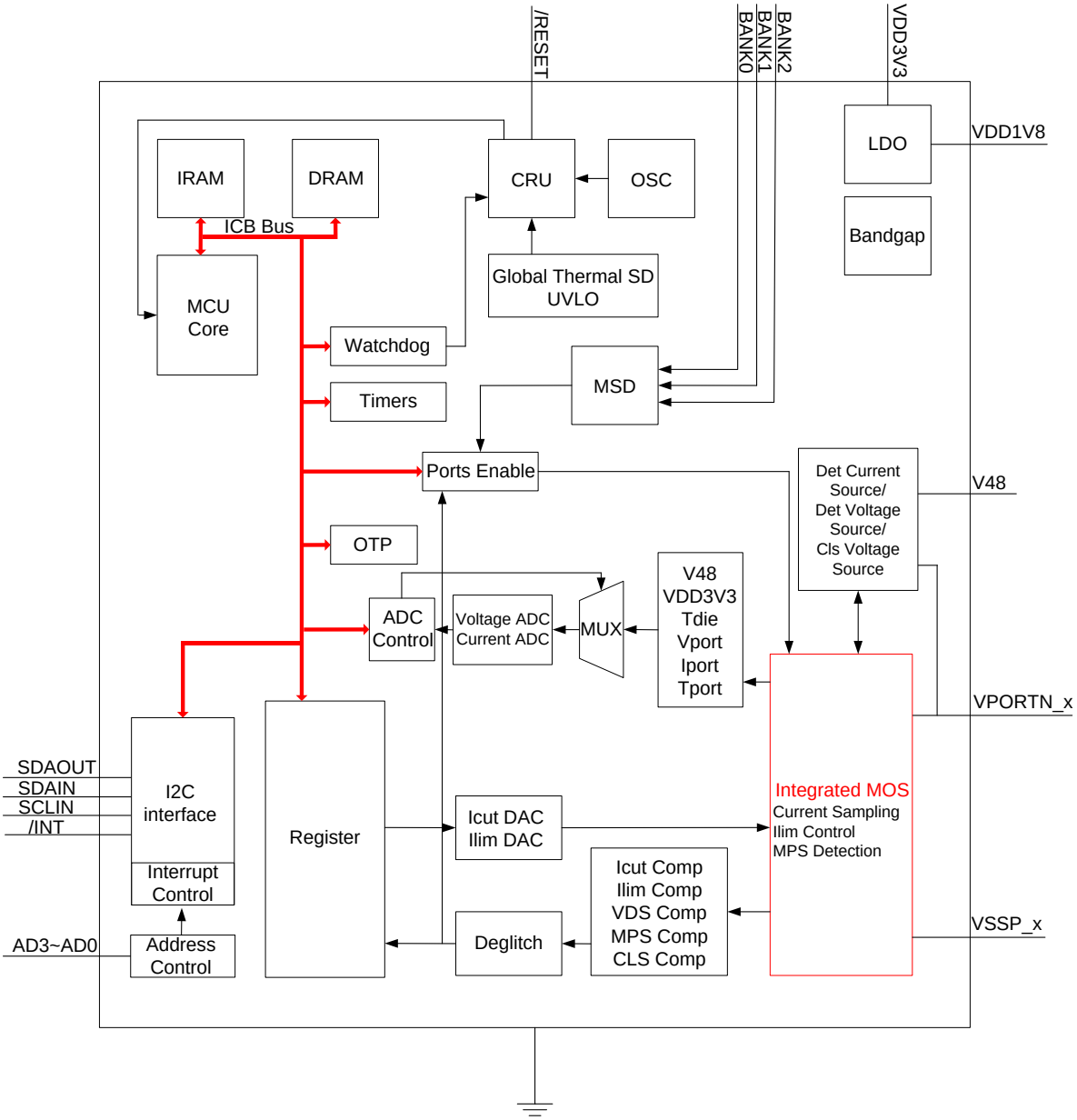
5) Guaranteed by design.

PIN DESCRIPTION

Pin QFN8*8-56	Name	Description
1, 7, 8, 14, 29, 35, 36, 42, 46	VSS	Ground Pins.
2, 6, 9, 13, 30, 34, 37, 41	VSSP1, VSSP2, VSSP3, VSSP4, VSSP5, VSSP6, VSSP7, VSSP8	Ground Pins.
3, 5, 10, 12, 31, 33, 38, 40	VPORTN_1, VPORTN_2, VPORTN_3, VPORTN_4, VPORTN_5, VPORTN_6, VPORTN_7, VPORTN_8	Internal MOS drain, return pin of power interface.
4,11,15, 16,18, 25, 28, 32, 39, 52	NC	No Connection.
17	V48	48V analog power supply. A 0.1uF capacitor is connected between V48 and GND as close to this pin as possible.
19	ANC	Analog Test Pin.
20	DNC1	Digital Test Pin 1.
21	VSSA	Analog Ground Pin.
22	VDDA_3V3	3.3V analog power supply. Connect to an external 3.3V power supply to this pin. VDDA_3V3 must be bypassed to GND near the JWH7295 with at least a 1uF capacitor.
23, 24, 56	BANK1, BANK2, BANK0	Power Bank Pins. Internal pulled down to GND.
26	DNC2	Digital Test Pin 2.
27	DNC3	Digital Test Pin 3.
43	VDD_3V3	3.3 digital power supply. Connect to a 3.3V external power supply to this pin. VDD_3V3 must be bypassed to GND near the JWH7295 with at least a 1uF

		capacitor.
44	nRESET	Chip reset pin, active low. When the nRESET pin is low, the JWH7295 is held inactive with all ports off and all internal registers reset to their power-up states. When nRESET is pulled high, the JWH7295 begins normal operation. /RESET can be connected to an external cap or RC network to provide a power turn on delay. Internal filtering of the nRESET pin prevents glitches less than 1uS wide from resetting the JWH7295. Internal pulled up to VDD_3V3.
45	nINT	nINT will generate a low pulse when any of several events occur in the JWH7295. Internal pulled up to VDD_3V3.
47	VDD_1V8	1.8V digital power supply. Less than 0.5μF but at least 0.1μF ceramic capacitor is needed between this pin and DGND.
48	ADDR1	Address bit 1. Internally pulled up to VDD_3V3.
49	ADDR2	Address bit 2. Internally pulled up to VDD_3V3.
50	ADDR3	Address bit 3. Internally pulled up to VDD_3V3.
51	ADDR4	Address bit 4. Internally pulled up to VDD_3V3.
53	SCLKIN	Serial clock input. Clock input for the I2C serial interface bus. SCL must be tied to high if not used. Internal pull up to VDD_3V3.
54	SDATAIN	Serial data input. Data input for the I2C serial interface bus. The JWH7295 uses two pins to implement the bidirectional SDA function to simplify opto-isolation of the I2C bus. To implement a standard bidirectional SDA pin, tie the SDAOUT and SDAIN together. SDAIN must be tied high if not used. Internal pull up to VDD_3V3.
55	SDATAOUT	Serial data output, data output for I2C interface bus. The JWH7295 uses two pins to implement the bidirectional SDA function to simplify opto-isolation of the I2C bus. To implement a standard bidirectional SDA pin, tie the SDAOUT and SDAIN together. SDAOUT should be grounded or left floating if not used. Internal pull up to VDD_3V3.
Thermal Pad		Electrically referenced to VSS. Connect to a large thermal mass trace or GND plane to dramatically improve thermal performance.

BLOCK DIAGRAM

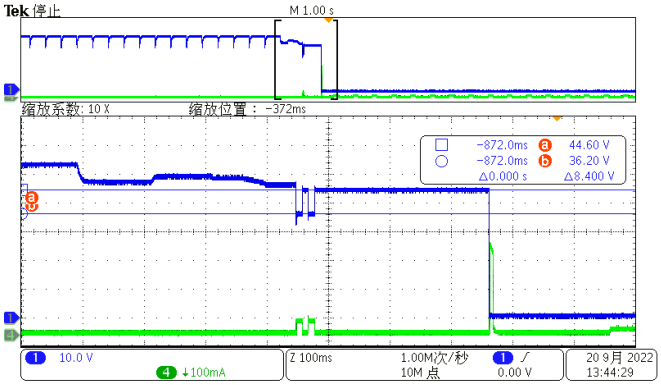


TYPICAL PERFORMANCE CHARACTERISTICS

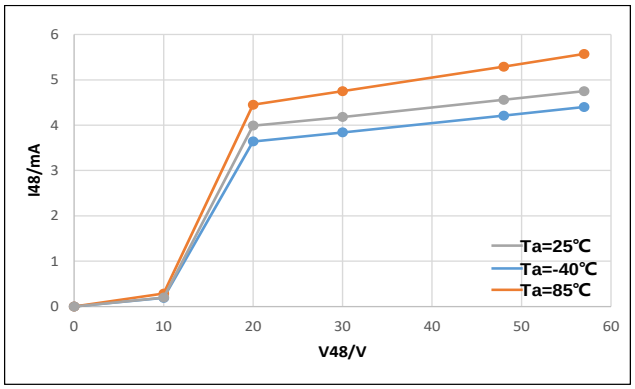
V48 = 54V, VDD_3V3 = VDDA_3V3 = 3.3V, TA = +25°C, unless otherwise noted

Power-On Sequence in AUTO Mode

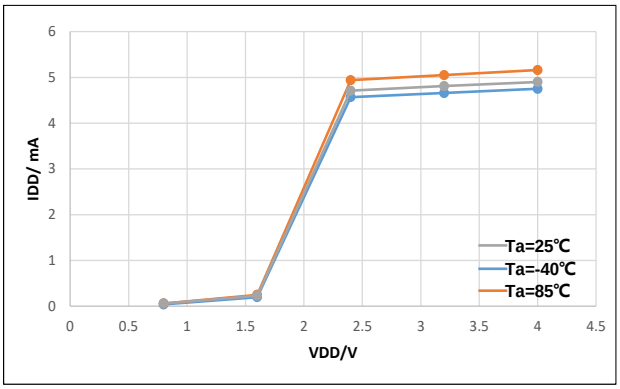
Class-4 Event in AT



V48 Quiescent Current



VDD Quiescent Current



FUNCTIONAL DESCRIPTION

The JWH7295 is a eight-port PSE for power over Ethernet applications. Each of the eight ports can be used as an eight-port PSE in compliance with the IEEE 802.3at standard.

Operation Mode

The JWH7295 includes four independent ports, each of which can operate in one of four modes: manual, semi-auto, auto, or shutdown. When the four ports operate in auto mode, it will automatically detect, class, and power on. Host can configure MDSEL register (12h) after power-up to select between four modes of operation for each of the four ports.

Table 1. Operation Modes

MODE	MDSEL	DETECT/ CLASS	POWER-UP	AUTOMATIC I_{CUT}/I_{LIM} ASSIGNMENT
Auto	11b	Enabled at Reset	Automatically	Yes
Semi-auto	10b	Host Enabled	Upon Request	No
Manual	01b	Once Upon Request	Upon Request	No
Shutdown	00b	Disabled	Disabled	No

- In manual mode, the port waits for instructions from the host system before taking any action. It runs a single detection or classification cycle when commanded by the host, and reports the result in its Port Status register. The host system can command the port to turn on or turn off the power at any time. This mode should only be used for diagnostic and test purposes.
- In semi-auto mode, the port repeatedly attempts to detect and classify any PD attached to it. It reports the status back to the host, and waits for a command from the host before applying power to the port. The host must enable detection (and optionally enable classification) for the port before starting detection.
- Auto mode operates as the same as semi-auto mode except that it will automatically apply the power to the port if detection is successful. In auto mode, I_{CUT} and I_{LIM} values are set automatically by the JWH7295.
- In shutdown mode, the port is disabled and will not detect or power a PD.

Regardless of which mode it is in, the JWH7295 will remove power automatically from any port that generates a current limit fault. It will also automatically remove power from any port that generates a disconnect event if disconnect detection is enabled. The host controller may also command the port to remove power at any time.

Reset Pins

Reset occurs at power-up, or whenever the nRESET pin is pulled low.

The JWH7295 needs be used with a host controller. After reset, the host will download the firmware to the device.

Each port will detect and classify repeatedly until a PD is discovered, set I_{CUT} and I_{LIM} according to the classification results, apply power after successful detection, and remove power when a PD is disconnected.

Table 2 shows the I_{CUT} and I_{LIM} values that will be automatically set in Auto mode, based on the discovered class when connected to single-signature PD.

Table 2. I_{CUT} and I_{LIM} Values in Auto Mode for SSPD

CLASS	I_{CUT_2P}	I_{CUT}	I_{LIM_2P}
Class 0, 13W	375mA	375mA	425mA
Class 1, 4W	109mA	109mA	425mA
Class 2, 7W	156mA	156mA	425mA

Class 3, 13W	375mA	375mA	425mA
Class 4, 30W	656mA	656mA	850mA

Table 3 shows the I_{CUT} and I_{LIM} values that will be automatically set in Auto mode, based on the discovered class when connected to dual-signature PD.

Table 3. I_{CUT} and I_{LIM} Values in Auto Mode for DSPD

CLASS	I_{CUT_2P}	I_{LIM_2P}
Class 0, 13W	375mA	425mA
Class 1, 4W	109mA	425mA
Class 2, 7W	156mA	425mA
Class 3, 13W	375mA	425mA
Class 4, 30W	656mA	850mA

The automatic setting of the I_{CUT} and I_{LIM} values only occurs if the JWH7295 is in auto mode.

Detection

To avoid damaging network devices that were not designed to tolerate DC voltage, a PSE must determine whether the connected device is a real PD before applying power. The IEEE specification requires that a valid PD have a common-mode resistance of 25k ±5% at any port voltage below 10V. The PSE must accept resistances that fall between 19k and 26.5k, and it must reject resistances above 33k or below 15k. The PSE may choose to accept or reject resistances in the undefined areas between the must-accept and must-reject ranges. In particular, the PSE must reject standard computer network ports, many of which have 150Ω common-mode termination resistors that will be damaged if power is applied to them.

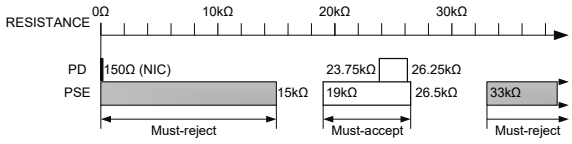


Figure 1. IEEE 802.3af Signature Resistance Ranges

PD signature resistances between 17k and 29.7k (typically) are detected as valid and reported as Detect Good in the corresponding Port Status register. Values outside this range, including open and short-circuit, are also reported. If the port measures less than 1V at the first test, the detection cycle will abort and Short Circuit will be reported. Table 4 shows the possible detection results.

Table 4. Detection Status

MEASURED PD SIGNATURE	DETECTION RESULT
Incomplete	0 = Unknown
R_{PD} < 1.5k	1 = Short
R_{PD} > 1.5k and C_{PD} > 2uF	2 = C_{PD} Too High
1.5k < R_{PD} < 17k	3 = R_{SIG} Low
17k < R_{PD} < 29.7k	4 = Good
29.7k < R_{PD} < 50k	5 = R_{SIG} High
R_{PD} > 50k	6 = Open
FETBAD	7 = FETBAD
Reserved	8~F = Reserved

More on Operating Modes

The port's operating mode determines when the JWH7295 runs a detection cycle. In manual mode, the port is idle until the host starts a detect cycle. It then runs detection, reports the results, and returns to idle to wait for another command.

In semi-auto mode, the JWH7295 autonomously polls a port for PDs, but it will not apply power until commanded to power on by the host. The Port Status register is updated at the end of each detection cycle. If a valid signature resistance is detected and classification is enabled, the port will classify the PD and report that result as well. The port will then wait for 250ms (or 2.5 seconds if midspan mode is enabled), and will repeat the detection cycle to ensure that the data in the port status register is up-to-date.

In Auto mode, after Detect Good is reported and the port is classified (if classification is enabled), it is automatically powered on without further intervention. In Auto mode, the I_{CUT} and I_{LIM} thresholds are automatically set; see the Reset and the Reset Pin section for more information.

The signature detection circuit is disabled when the port is initially powered up in shutdown mode, or when the corresponding Detect Enable bit is cleared.

Classification

802.3af Classification

A PD can optionally present a classification signature to the PSE to indicate the maximum power it will draw while operating. The IEEE specification defines this signature as a constant current draw when the PSE port voltage is in the V_{CLASS} range (between 15.5V and 20.5V), with the current level indicating one of 5 possible PD classes. Figure 2 shows a typical PD load line, starting with the slope of the 25kΩ signature resistor below 10V, then transitioning to the classification signature current (in this case, Class 3) in the V_{CLASS} range.

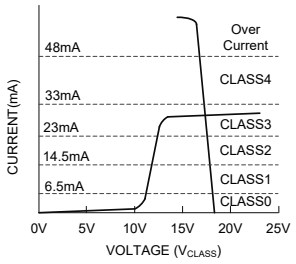


Figure 2. PD Classification

If classification is enabled, the port will classify the PD immediately after a successful detection cycle in semi-auto or auto modes, or when commanded in manual mode. It measures the PD classification signature by applying 18V for 12ms (both values typical) to the port via the V_{PORTN_X} pin and measuring the resulting current; it then reports the discovered class in the Port Status registers. If the JWH7295 in auto mode, it will additionally use the classification result to set the I_{CUT} and I_{LIM} thresholds. See the Reset and the Reset Pin section for more information.

The classification circuit is disabled when the port is initially powered up in shutdown mode, or when the corresponding class enable bit is cleared.

802.3at Classification

A Type 2 PD that is requesting more than 13W will indicate Class 4 during normal 802.3af classification. If the JWH7295 sees Class 4, it forces the port to a specified lower voltage (called the mark voltage, typically 9V), pauses briefly, and then re-runs classification to verify the Class 4 reading. The second cycle alerts the PD that it is connected to a Type 2 PSE which can supply Type 2 power levels.

Note that the port only runs the second classification cycle when it detects a Class 4 during first classification; if the first classification returns Class 0 to 3, the port assumes it is connected to a Type 1 PD and does not run the second classification cycle.

Power Control

Power Supplies and Bypassing

The JWH7295 requires two supply voltages to operate. V_{DD} requires 3.3V (nominally) and V_{48} requires a voltage of between 44V and 60V. V_{DD} provides power for the internal digital circuit, and draws a maximum of 4mA. A ceramic decoupling cap of at least 1μF should be placed from V_{DD} to GND as close to the chip pin as possible. Meanwhile, a ceramic decoupling cap (0.1~0.5μF) should be placed from VDD_1V8 to GND as close to the chip pin as possible.

Once the power supply is completed, it is necessary to activate the chip core to ensure that JWH7295 can function properly. We only need to input the following command words to a specific register address through the IIC interface: 0xC0=0x6C; 0xC1=0xC0; 0xC3=0x1F; 0xC5=0x10. And then wait for 5ms until PSE is fully activated before starting normal operation.

Internal MOSFET

The primary function of the JWH7295 is to control the delivery of power to the PSE port. It does this by controlling the gate drive voltage of an internal power MOSFET while monitoring the current via an internal sense resistor and the output voltage at the V_{PORTN_x} pin. This circuit delivers V48 input supply to the port in a controlled manner that satisfies the PD's power needs while minimizing power dissipation in the MOSFET.

Inrush Control

Once the command has been given to turn on a port, the JWH7295 ramps up the gate of that port's internal MOSFET in a controlled manner. Under normal power-up circumstances, the MOSFET gate will rise until the port current reaches the inrush current limit level, at which point the gate will be controlled to maintain the specified I_{INRUSH} current. During this inrush period, a timer (t_{START}) runs. When output charging is complete, the port current will fall and the gate will be allowed to continue rising to fully enhance the MOSFET and minimize its on-resistance. The inrush period is maintained until the t_{START} timer expires. At this time if the inrush current limit level is still exceeded the port will be turned back off and a t_{START} fault reported.

Current Limit

Each JWH7295 channel includes two current limiting thresholds (I_{CUT} and I_{LIM}), each with a corresponding timer (t_{CUT} and t_{LIM}). Setting the I_{CUT} and I_{LIM} thresholds depends on several factors: the class of the PD, the voltage of the main supply (V_{48}), the type of PSE (Type 1 or Type 2) and whether or not the system is required to implement class enforcement.

Per the IEEE specification, the JWH7295 will allow the port current to exceed I_{CUT} for a limited period of time before removing power from the port, whereas it will actively control the MOSFET gate drive to keep the port current below I_{LIM}. The port does not take any action to limit the current when only the I_{CUT} threshold is exceeded, but does start the t_{CUT} timer. If the current drops below the I_{CUT} current threshold before its timer expire, the t_{CUT} timer counts back down, but at 1/16 the rate that it counts up. If the t_{CUT} timer reaches 60ms (typ.) the port is turned off and the port t_{CUT} fault is set. This allows the current limit circuit to tolerate intermittent overload signals with duty cycles below about 6.3%; longer duty cycle overloads will turn the port off.

The I_{LIM} current limiting circuit is always enabled and actively limiting port current. JWH7295 allows t_{LIM} to be set to a shorter value than t_{CUT} to provide more aggressive MOSFET protection and turn off a port before MOSFET damage can occur. The t_{LIM} timer starts when the ILIM threshold is exceeded. When the t_{LIM} timer reaches 60ms(typ.), the port is turned off and the port t_{LIM} fault is set.

I_{CUT} is typically set to a lower value than I_{LIM} to allow the port to tolerate minor faults without current limiting.

I_{LIM} Foldback

The JWH7295 features a foldback circuit that reduces the port current if the port voltage falls below the normal operating voltage. This keeps MOSFET power dissipation at safe levels. Current limit and foldback behavior are programmable on a per-port basis. Table 5 gives examples of recommended I_{LIM} register settings.

The JWH7295 will support current levels well beyond the maximum values in the 802.3bt specification.

Table 5. Example Current Limit Settings

I_{LIM}(mA)	Internal Register Setting (hex)
53	04
106	08
159	0C
213	10
266	14
319	18
372	1C
425	**20**

VDD and V48 UVLO

When both V_{DD_3V3} and V48 exceeds the UVLO rising threshold, the JWH7295 begins to work normally. If either voltage drops below UVLO falling threshold, the JWH7295 stops working. The powering up sequence of the two external power source is not strict restriction.

Voltage and Current Readback

The JWH7295 measures the output voltage and current at each port with internal 14-bit A/D converters. Port data is only valid when the port power is on.

Disconnect

The JWH7295 monitors the port to make sure that the PD continues to draw the minimum specified current. A disconnect timer counts up whenever the current is below I_{HOLD_2P}, indicating that the PD has been disconnected. If the t_{DIS} timer expires, the port will be turned off and the disconnect bit in the fault event register will be set. If the current returns before the t_{DIS} timer runs out, the timer resets and will start counting from the beginning if the undercurrent condition returns. As long as the PD exceeds the minimum current level more often than t_{DIS}, it will stay powered.

Although not recommended, the DC disconnect feature can be disabled by clearing the corresponding DC Disconnect Enable bits. Note that this defeats the protection mechanisms built into the IEEE spec, since a powered port will stay powered after the PD is removed. If the still powered port is subsequently connected to a non-PoE data device, the device may be damaged.

BANKn Pins

The JWH7295 includes a hardware shutdown function for each port. When the code of BANKn pin is equal to the bit of fast pull down register and this bit is set to 0, the corresponding channel will be shut down immediately.

Serial Digital Interface

The JWH7295 communicates with the host using a standard I^2C 2-wire interface. The JWH7295 is a slave-only device, and communicates with the host master using the standard I^2C protocols. Interrupts are signaled to the host via the nINT pin. When an interrupt happens, a 256uS low level pulse will be generate. The Timing Diagrams (Figures 3 through 5) show typical communication waveforms and their timing relationships.

The JWH7295 requires both the V_{DD_3V3} and V_{48} supply rails to be present for the serial interface to function.

Bus Addressing

The JWH7295 has 2 serial bus address per device, which is 01xxxx0 and 01xxxx1 with four bits set by the ADDR4-ADDR1 pins; this allows up to 16 JWH7295s on a single bus. All JWH7295s also respond to the address 1100100b, allowing the host to write the same command (typically configuration commands) to multiple JWH7295s in a single transaction.

Interrupt and Alert

Most JWH7295 port events can be configured to trigger an interrupt, asserting the nINT pin and alerting the host to the event. To minimize serial bus traffic and conserve host CPU cycles, multiple JWH7295s can share a common nINT line.

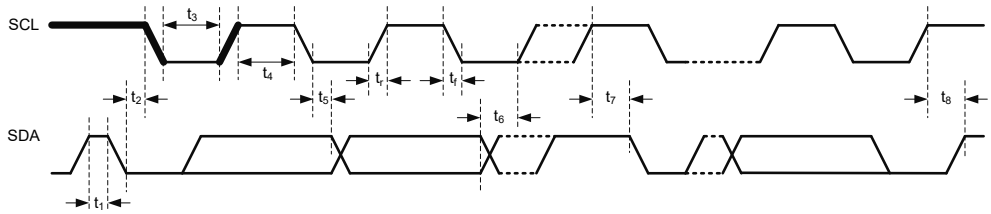


Figure 3. I²C Interface Timing

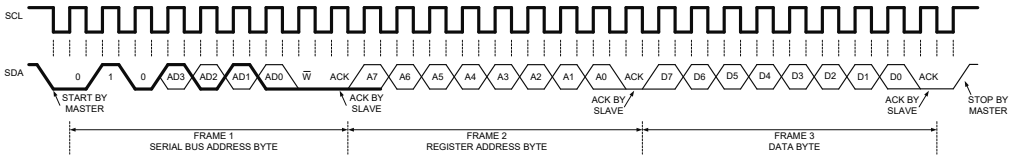


Figure 4. Writing to a Register

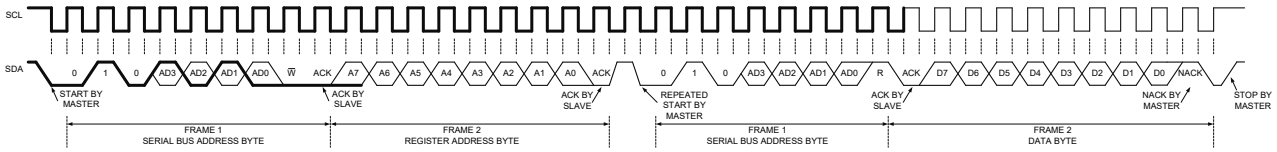


Figure 5. Reading from a Register

Isolating the Serial Bus

The JWH7295 includes a split SDA pin (SDAIN and SDAOUT) to ease opto-isolation of the bidirectional SDA line.

IEEE 802.3 Ethernet specifications require that network segments (including PoE circuit) be electrically isolated from the chassis ground of each network interface device. However, network segments are not required to be isolated from each other, provided that the segments are connected to devices residing within a single building on a single power distribution system.

For simple devices such as small PoE switches, the isolation requirement can be met by using an isolated main power supply for the entire device. This strategy can be used if the device has no electrically conducting ports other than twisted-pair Ethernet. In this case, the SDAIN and SDAOUT pins can be tied together and will act as a standard I²C SDA pin.

If the device is part of a larger system, contains additional external non-Ethernet ports, or must be referenced to protective ground for some other reason, the Power over Ethernet subsystem (including all JWH7295s) must be electrically isolated from the rest of the system. Figure 6 shows a typical isolated serial interface. The SDAOUT pin of the JWH7295 is designed to drive the inputs of an opto-coupler directly. Standard I²C devices typically cannot drive opto-couplers, so U1 is used to buffer the signals from the host controller side.

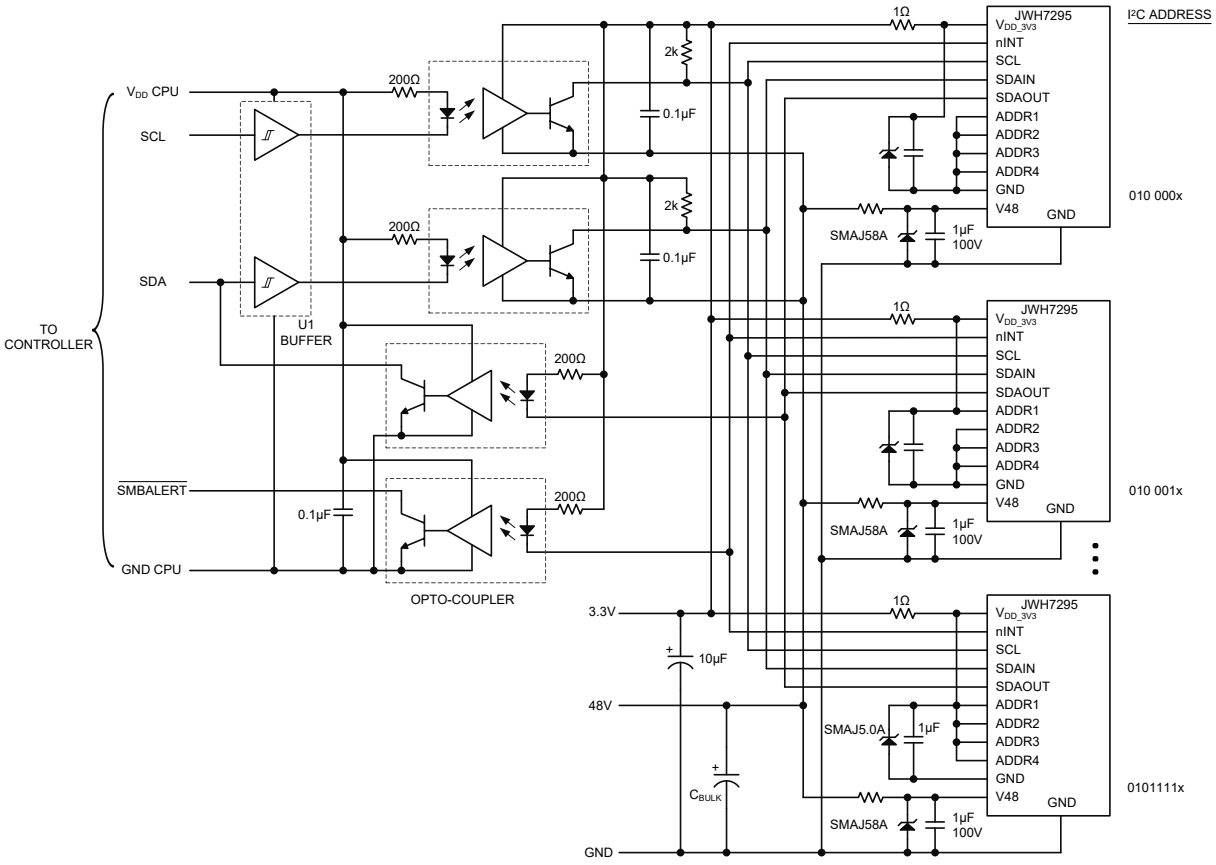
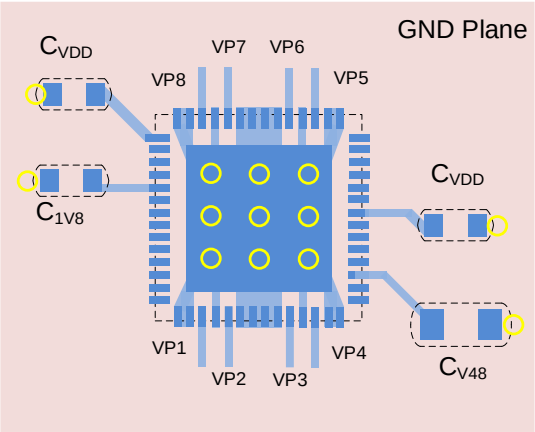


Figure 6. Opto-Isolating the I²C Bus

PCB Layout Guidelines

For minimum noise problem and best operating performance, the PCB layout of JWH7295 must be carefully designed:

1. Locate the V48 capacitor as close as possible to the ICs.
2. The V_{DD} and V_{1V8} capacitors should be placed as close to the chip as possible.
3. Use the GND Plane for power loss dissipation.

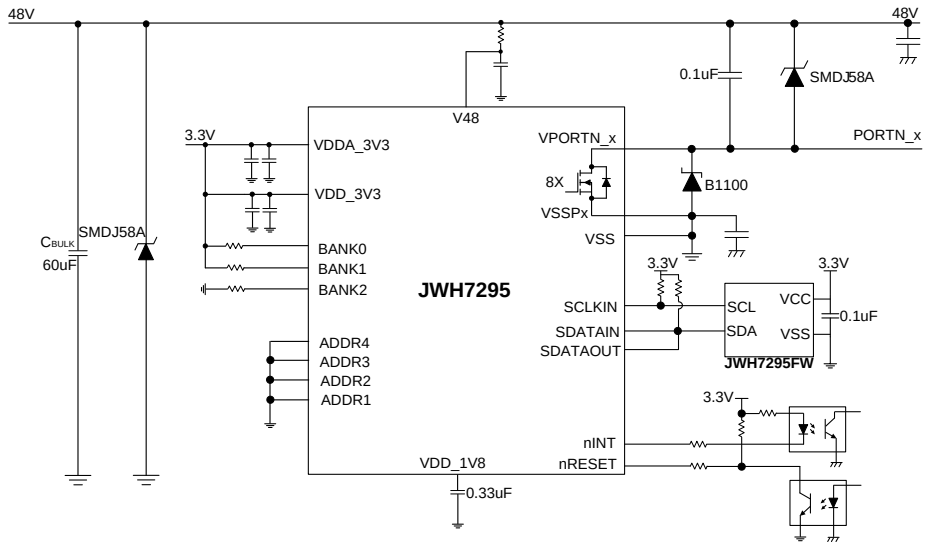


REFERENCE DESIGN

Note: Information in the following reference design sections is not part of JoulWatt component specification. Customers are responsible for determining suitability of components chosen for their purposes and should validate their design implementation to make sure the proper system functionality.

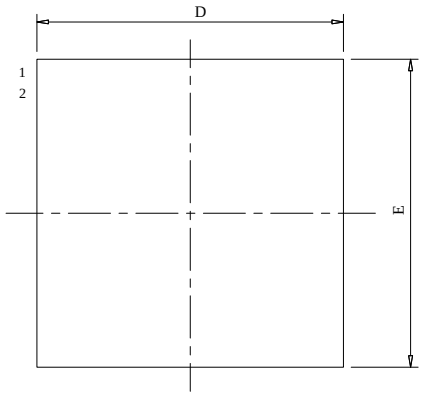
It is convenient for engineers to apply JWH7295 with JWH7295FW.The JWH7295FW is a system on chip (SoC) integrated with 16k byte flash，which is sufficient to support loading firmware of JWH7295. The firmware supports JWH7295 to enter automatic mode and no longer need to configure any register. The firmware is compatible with IEEE 802.3af/at.

The JWH7295FW also has IIC interface to implement communication with JWH7295. Just as shown in the figure below, engineer only prepares the 3.3V power and IIC interface. Its communication rate reaches 100kb/s， which supports the normal operation of JWH7295 within 4 seconds of power on. The JWH7295FW is available in a space-saving SOP16 package, which helps customer save PCB size.

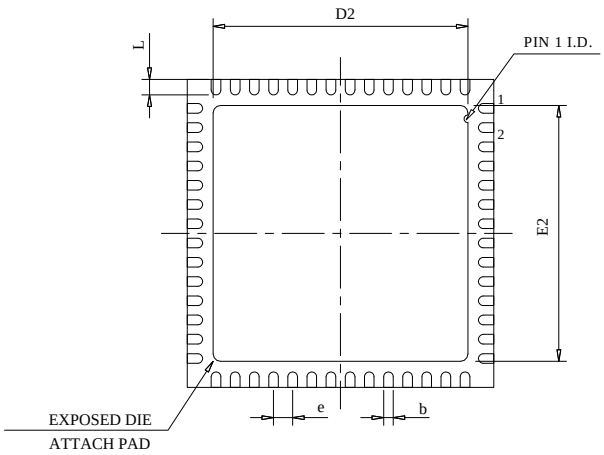


PACKAGE OUTLINE

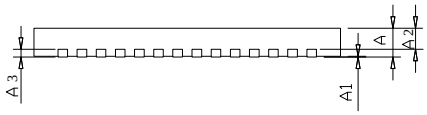
QFN8*8-56 Unit: mm



TOP VIEW



BOTTOM VIEW



SIDE VIEW

SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	0.80	0.85	0.90
A1	0	0.02	0.05
A2	---	0.65	---
A3	0.203REF		
b	0.20	0.25	0.30
D	7.90	8.00	8.10
E	7.90	8.00	8.10
e	0.50 BSC		
D2	5.6	5.7	5.8
E2	5.6	5.7	5.8
L	0.3	0.4	0.5

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