# LPDDR5/5X Datasheet

## RS4G32LO5D8FDB-31BT

### 315-ball

**Revision 1.0**

**Dec. 18. 2023**

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# Revision History

| Version | Date | Changes |
|---|---|---|
| V1.0 | 2023-12-18 | Basic spec and architecture |

***Notes：*** *This data sheet contains minimum and maximum limits specified over the power supply and temperature range set forth herein. Although considered final, these specifications are subject to change at any time without notice, as further product development and data characterization sometimes occur.*

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# 1. Product Overview

## 1.1. Feature Overview

- Architecture
  - 12.8 GB/s maximum bandwidth per channel
  - Frequency range: 800–5 MHz (data rate range per pin: 6400–40 Mbp/s with WCK:CK = 4:1)
  - Selectable CKR (WCK:CK = 2:1 or 4:1)
- LPDDR5/5X data interface
  - Single x16 channel/die
  - Double-data-rate command/address entry
  - Differential command clocks (CK_t/CK_c) for high-speed operation
  - Differential data clocks (WCK_t/WCK_c)
  - Optional differential read strobe (RDQS_t/ RDQS_c)
  - 16n-bit or 32n-bit prefetch architecture
  - 4KB page size with 8-bank (8B mode), 2KB page size with bank group (BG mode), or 16-bank (16B mode) operation
  - Command-selectable burst lengths (BL = 16 or 32) in bank group or 16-bank modes
  - Background ZQ calibration/command-based ZQ calibration- Optional link protection (link ECC)
  - Optional link protection (link ECC)
  - Partial-array self refresh (PASR) and partial-array auto refresh (PAAR) with segment mask
- Ultra-low-voltage core and I/O power supplies
  - $V_{DD1}$ = 1.70–1.95V; 1.8V NOM
  - $V_{DD2H}$ = 1.01–1.12V; 1.05V NOM
  - $V_{DD2L}$ = $V_{DD2H}$ or 0.87–0.97V; 0.9V NOM
  - $V_{DDQ}$ = 0.5V NOM or 0.3V NOM (ODT off)
- I/O characteristics
  - Interface-LVSTL 0.5/0.3
  - I/O type: Low-swing single-ended, $V_{SS}$ terminated
  - $V_{OH}$-compensated output drive

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- Programmable $V_{SS}$ on-die termination (ODT)
- Non target ODT support
- DVFSQ support

- Low power features
  - DVFSC: Dynamic voltage frequency scaling core
  - Single-ended CK, single-ended WCK, and single- ended RDQS

  $V_{DD1}/V_{DD2H}/V_{DD2L}/V_{DDQ}$ （ODT on） / (ODT off): 1.8V/1.05V/0.9V/0.5V/0.3V
- Array configuration
  - 4 Gig x 32 (2 channels x 16 I/O)
- Device configuration
  - 1G16 x 8 die in package
- FBGA “green” package
  - 315-ball FBGA (12.4mm x15mm Seated height: 1.1mm MAX)
- Speed grade, cycle time ($^{t}$WCK)
  - 6400 Mb/s
- Operating temperature range
  - -25°C to + 85°C

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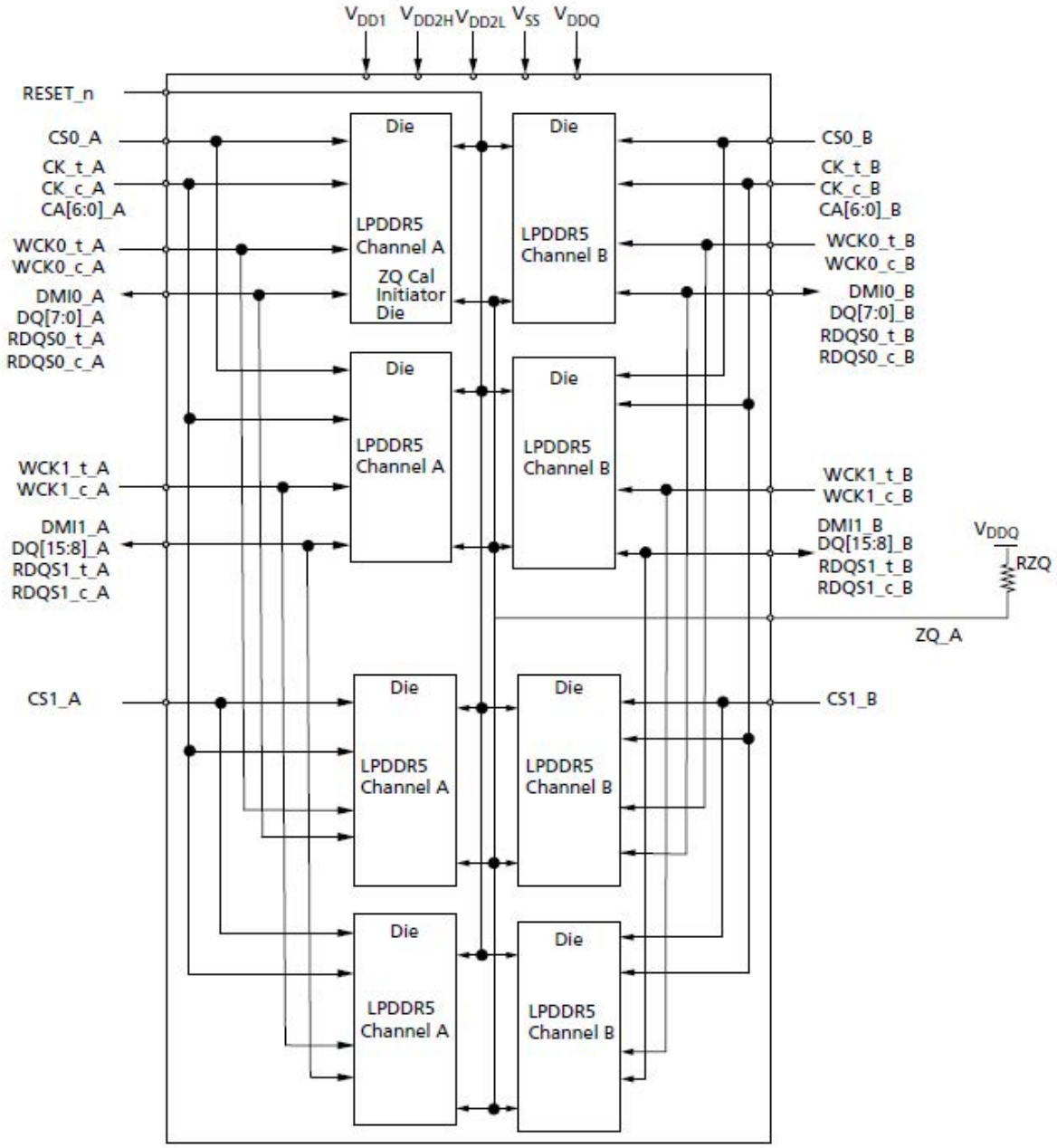
# 2. Physical Specifications

## 2.1. Function Block Diagram




**Eight-Die, Dual-Channel Package,Dual-Rank Block Diagram**

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## 2.2. Package ballout & Addressing

### 315-Ball Dual-Channel Discrete VFBGA

| | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 | 13 | 14 | 15 | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| A | NC | NC | VDDQ | DMI0_A | VSS | VDD2L | VDD2H | VDD2H | VDD2H | VDD2L | VSS | DMI1_A | VDDQ | NC | NC | A |
| B | NC | VDDQ | RDQS0_t_A | VSS | DQ4_A | VDD2L | VDD2H | VSS | VDD2H | VDD2L | DQ12_A | VSS | RDQS1_t_A | VDDQ | NC | B |
| C | VDD1 | DQ1_A | VDDQ | RDQS0_c_A | VSS | DQ5_A | VDD2H | VSS | VDD2H | DQ13_A | VSS | RDQS1_c_A | VDDQ | DQ9_A | VDD1 | C |
| D | DQ0_A | VSS | DQ3_A | VDDQ | WCK0_c_A | VSS | VSS | VDD2H | VSS | VSS | WCK1_c_A | VDDQ | DQ11_A | VSS | DQ8_A | D |
| E | VSS | DQ2_A | VSS | WCK0_t_A | VDDQ | DQ6_A | VDD2H | VSS | VDD2H | DQ14_A | VDDQ | WCK1_t_A | VSS | DQ10_A | VSS | E |
| F | VDDQ | VSS | VDDQ | VDDQ | DQ7_A | VDD2H | VDD2H | VSS | VDD2H | VDD2H | DQ15_A | VDDQ | VDDQ | VSS | VDDQ | F |
| G | VDDQ | VDDQ | VSS | CA0_A | VSS | CS1_A | VSS | CA2_A | VSS | CA4_A | VSS | CA6_A | VSS | VDDQ | VDDQ | G |
| H | RESET_N | VDD2L | VSS | VSS | CA1_A | VSS | CS0_A | VSS | CK_t_A | VSS | CA3_A | VSS | CA5_A | VDD2L | ZQ_A | H |
| J | VSS | VDD2L | VSS | RFU | VDD2H | RFU | VSS | VSS | CK_c_A | VSS | VDD2H | VSS | VSS | VDD2L | VSS | J |
| K | VDD2H | VDD2H | VDD2H | VDD2H | VDD2H | VDD2H | VSS | VSS | VSS | VDD2H | VDD2H | VDD2H | VDD2H | VDD2H | VDD2H | K |
| L | VSS | VSS | VSS | VSS | VSS | VDD2H | VDD2H | VDD2H | VDD2H | VDD2H | VSS | VSS | VSS | VSS | VSS | L |
| M | VDD2H | VDD2H | VDD2H | VDD2H | VDD2H | VDD2H | VSS | VSS | VSS | VDD2H | VDD2H | VDD2H | VDD2H | VDD2H | VDD2H | M |
| N | VSS | VDD2L | VSS | VSS | VDD2H | VSS | CK_C_B | VSS | VSS | VSS | VDD2H | VSS | VSS | VDD2L | VSS | N |
| P | RFU | VDD2L | CA5_B | VSS | CA3_B | VSS | CK_t_B | VSS | CS0_B | VSS | CA1_B | VSS | VSS | VDD2L | RFU | P |
| R | VDDQ | VDDQ | VSS | CA6_B | VSS | CA4_B | VSS | CA2_B | VSS | CS1_B | VSS | CA0_B | VSS | VDDQ | VDDQ | R |
| T | VDDQ | VSS | VDDQ | VDDQ | DQ15_B | VDD2H | VDD2H | VSS | VDD2H | VDD2H | DQ7_B | VDDQ | VDDQ | VSS | VDDQ | T |
| U | VSS | DQ10_B | VSS | WCK1_t_B | VDDQ | DQ14_B | VDD2H | VSS | VDD2H | DQ6_B | VDDQ | WCK0_t_B | VSS | DQ2_B | VSS | U |
| V | DQ8_B | VSS | DQ11_B | VDDQ | WCK1_c_B | VSS | VSS | VDD2H | VSS | VSS | WCK0_c_B | VDDQ | DQ3_B | VSS | DQ0_B | V |
| W | VDD1 | DQ9_B | VDDQ | RDQS1_c_B | VSS | DQ13_B | VDD2H | VSS | VDD2H | DQ5_B | VSS | RDQS0_c_B | VDDQ | DQ1_B | VDD1 | W |
| Y | NC | VDDQ | RDQS1_t_B | VSS | DQ12_B | VDD2L | VDD2H | VSS | VDD2H | VDD2L | DQ4_B | VSS | RDQS0_t_B | VDDQ | NC | Y |
| AA | NC | NC | VDDQ | DMI1_B | VSS | VDD2L | VDD2H | VDD2H | VDD2H | VDD2L | VSS | DMI0_B | VDDQ | NC | NC | AA |
| | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 | 13 | 14 | 15 | |

VSS | VDD1 | VDD2H | VDD2L | VDDQ | CK | RDQS | WCK | DQ,DMI | CA,CS,ZQ,RESET | NC,RFU

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## 2.3. Pad Definition

| Symbol | Type | Description |
|---|---|---|
| CK_t_[A:B]<br>CK_c_[A:B] | Input | **Clock:** CK_t and CK_c are differential clock inputs. All double data rate (DDR) com- mand/address inputs are sampled on both crossing points of CK_t and CK_c. The first crossing point is the rising (falling) edge of CK_t (CK_c) and second crossing point is falling (rising) edge of CK_t (CK_c). Single data rate (SDR) inputs, CS is sampled on the crossing point that is the rising (falling) edge of CK_t (CK_c). |
| CS0_[A:B], CS1_[A:B] | Input | **Chip select:** CS is part of the command code, and is sampled on the rising (falling) edge of CK_t (CK_c) unless the device is in power-down or deep sleep mode where it becomes an asynchronous signal. Each rank (0, 1) has its own CS signals. CS1_[A:B] be- come NC pins in a single-rank package. |
| CA[6:0]_[A:B] | Input | **Command/address inputs:** Provide the command and address inputs according to the command truth table. |
| WCK[1:0]_t_[A:B]<br>WCK[1:0]_c_[A:B] | Input | **Data clock:** WCK_t and WCK_c are differential clock inputs used for write data cap- ture and read data output. |
| DQ[15:0]_[A:B] | I/O | **Data input/output:** Bidirectional data bus. |
| RDQS[1:0]_t_[A:B]<br>RDQS[1:0]_c_[A:B] | I/O Output | **Read data strobe:** RDQS_t and RDQS_c are differential output clock signals used to strobe data during a READ operation. RDQS_t is also used as a parity pin during write link protection enabled. Each byte of data has RDQS_t and RDQS_c signals. |
| DMI[1:0]_[A:B] | I/O | **Data mask inversion:** DMI serves multiple functions such as data mask (DM), data bus inversion (DBI), and parity at READ with ECC operation by setting the mode regis- ter. DMI is a bidirectional signal and each byte of data has a DMI signal. |
| ZQ_A | Reference | **ZQ calibration reference:** Used to calibrate the output drive strength and the termi- nation resistance. The ZQ pin should be connected to VDDQ through a 240Ω ±1% resistor. |
| $V_{DDQ}$, $V_{DD1}$, $V_{DD2H}$, $V_{DD2L}$ | Supply | **Power supplies:** Isolated on the die for improved noise immunity. |
| $V_{SS}$ | Supply | **Ground reference:** Power supply ground reference. |
| RESET_n | Input | **RESET:** When asserted LOW, the RESET pin resets all channels of the die. Reset is an asynchronous sig-nal. |
| NC | – | **No connect:** Not internally connected. |

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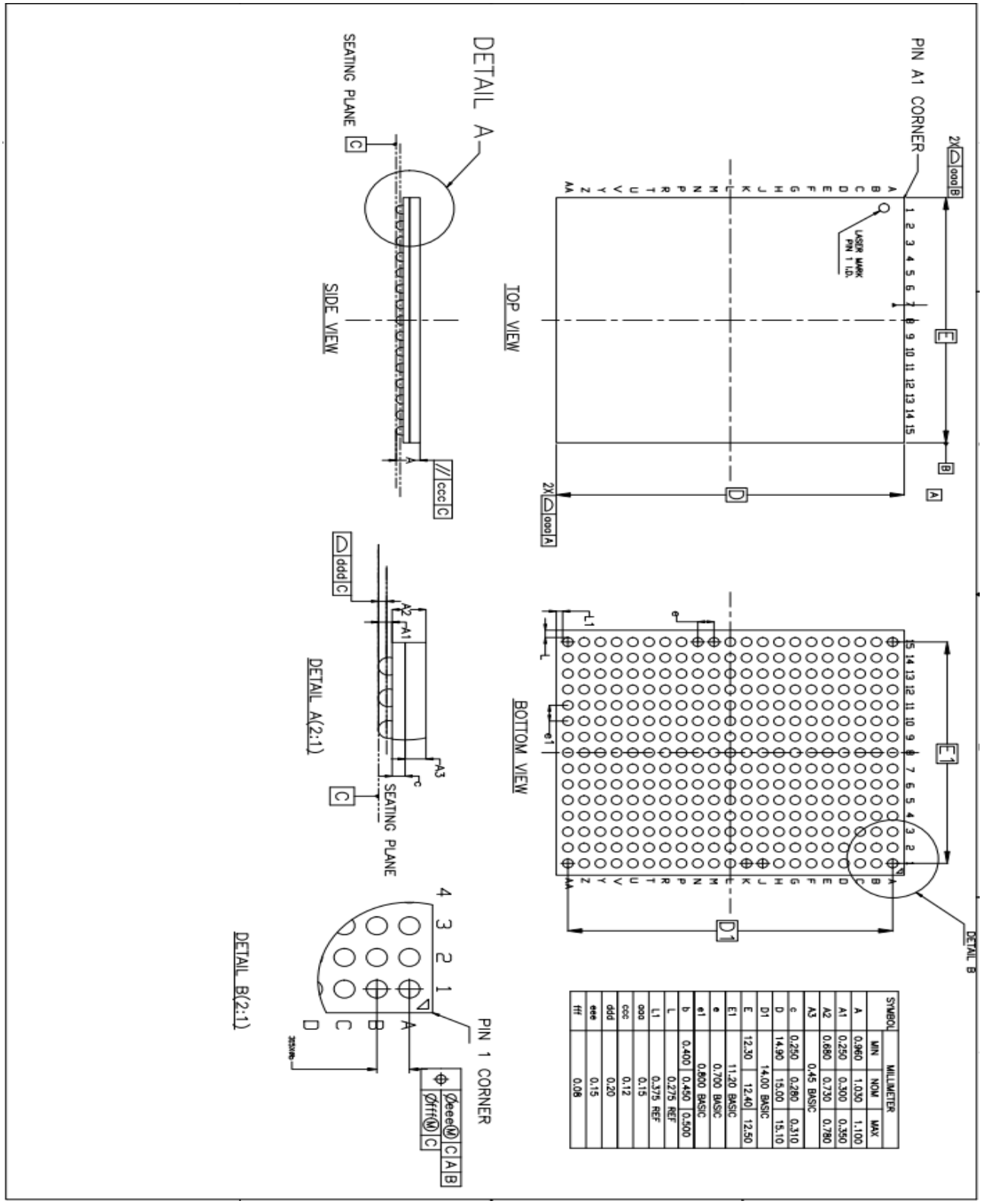
## 2.4. Discrete Package Dimension

### 12.4mm X15mm (Package Code: DB)

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# 3. Core Specifications

## 3.1. Part Number Decoding

**RS 4G32 LO5 D8 F DB - 31 BT**

**Rayson**
**Mobile DRAM Memory**

**Configuration**
**4G32** = 4 Gig x 32

**Product Family**
**LO5** = LPDDR5/5X Resource

**Die Count**
**D8** = 8 die

**Operating Voltage**
**F** = $V_{DD1}$ 1.80V
$V_{DD2H}$ 1.05V
$V_{DD2L}$ 0.9V
$V_{DDQ}$ 0.5V/0.3V

**Package code**
**DB** = 315ball FBGA-12.4*15

**Speed**
**31** = 6400Mb/s/pin

**Operating temperature**
**BT** = -25°C to +85°C

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## 3.2. Ordering Options

**Table 1: Part Number List**

| Part Number | Total Density | Data Rate | Operating temperature |
|---|---|---|---|
| RS4G32LO5D8FDB-31BT | 16GB(128Gb) | 6400 Mb/s/pin | -25°C to + 85°C |

**Table 2: Refresh Requirement Parameters**

| Parameter | Symbol | 16Gb | | unit |
|---|---|---|---|---|
| | | BG and 16 B Mode | 8B Mode | |
| REFRESH cycle time (all banks) | $^{t}$RFCab | 280 | 280 | ns |
| REFRESH cycle time (per bank) | $^{t}$RFCpb | 140 | 140 | ns |
| Per bank refresh to per bank refresh time (different bank) | $^{t}$PBR2PBR | 90 | 90 | ns |
| Per bank refresh to ACTIVATE command time (different bank) | $^{t}$PBR2ACT | 7.5 | 10 | ns |

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## 3.3. Die Addressing Table

| Configuration | | 4G32(128Gb/package) | | |
|---|---|---|---|---|
| Die Configuration | Channel A, rank 0<br>Channel A, rank 1 | x 8 mode × 1 die<br>x 8 mode × 1 die | | |
| | Channel B, rank 0<br>Channel B, rank 1 | x 8 mode × 1 die<br>x 8 mode × 1 die | | |
| | Channel A, rank 0<br>Channel A, rank 1 | x 8 mode × 1 die<br>x 8 mode × 1 die | | |
| | Channel B, rank 0<br>Channel B, rank 1 | x 8 mode × 1 die<br>x 8 mode × 1 die | | |
| Die Addressing | Bits | 17,179,869,184 | | |
| | Bank mode | BG mode | 16B mode | 8B mode |
| | Configuration | 128Mb × 8 DQ<br>× 4 Banks × 4 BG | 128Mb × 8 DQ<br>× 16 Banks | 256Mb × 8 DQ<br>× 8 Banks |
| | Number of banks | 4 | 16 | 8 |
| | Number of banks groups | 4 | 1 | 1 |
| | Array prefetch bits | 128 | 128 | 256 |
| | Rows per bank | 131,072 | | |
| | Columns | 64 | | |
| | Page size (bytes) | 1024 | 1024 | 2048 |
| | Native burst length | 16 | 16 | 32 |
| | Number of I/Os | 8 | | |
| | Bank address | BA[1:0] | BA[3:0] | BA[2:0] |
| | Bank group address | BG[1:0] | - | - |
| | Row address | R[15:0] (R14 = 0 when R15 = 1) | | |
| | Column address | C[5:0] | | |
| | Burst address | B[3:0] | B[3:0] | B[4:0] |
| | Burst starting address boundar | 128-bit | | |

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## 3.4. Mode Register Contens

| MR0 | | |
|---|---|---|
| OP7 | Per-pin DFE | **OP[0] = 1b:** Device supports different NT ODT latency for DQ and RDQS<br>**OP[1] = 0b:** Device supports x16 mode<br>**OP[2] = 1b:** Device supports enhanced WCK always-on mode.<br>**OP[3]** =**1b:** Device supports optimized refresh mode<br>**OP[4]** = **1b:** Device supports both DMI behavior mode 1 and 2 and mode selection<br>**OP[5] = 1b:** The NT ODT behavior follows the unified NT ODT behavior<br>**OP[6] = 1b:** Device supports Pre Emphasis mode<br>**OP[7] = 0b:** Device does not support Per Pin DFE |
| OP6 | Pre Emphasis | |
| OP5 | Unified NT ODT bebavior mode | |
| OP4 | DMI output behavior mode | |
| OP3 | Optimized refresh mode | |
| OP2 | Enhanced WCK always-on mode | |
| OP1 | Latency Mode | |
| OP0 | NT ODT timing mode | |

| MR1 | | |
|---|---|---|
| OP7 | | **OP[0] = 0b:** Device does not support CS ODT behavior OP<br>**OP[1] = 1b:** Device supports ARFM |
| OP6 | | |
| OP5 | | |
| OP4 | | |
| OP3 | | |
| OP2 | | |
| OP1 | ARFM support | |
| OP0 | CS ODT OP support | |

| MR3 | | |
|---|---|---|
| OP7 | | **OP[4:3] = 00b:** BG;<br>**01b:**8B;<br>**10b:**16B Mode Supported |
| OP6 | | |
| OP5 | | |
| OP4 | BK/BG Org | |
| OP3 | | |
| OP2 | | |
| OP1 | | |
| OP0 | | |

| MR5 | | |
|---|---|---|
| OP7 | Manufacturer ID | **1111 1111b : Micron** |
| OP6 | | |
| OP5 | | |
| OP4 | | |
| OP3 | | |
| OP2 | | |
| OP1 | | |
| OP0 | | |

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| MR6 | | |
|---|---|---|
| OP7 | Revision ID1 | 00000 0111b |
| OP6 | | |
| OP5 | | |
| OP4 | | |
| OP3 | | |
| OP2 | | |
| OP1 | | |
| OP0 | | |

| MR8 | | |
|---|---|---|
| OP7 | I/O width | **OP[7:6]** = **00b:** x16/channel |
| OP6 | | |
| OP5 | Density | **OP[5:2]** = **0110b:** 16Gb |
| OP4 | | |
| OP3 | | |
| OP2 | | |
| OP1 | Type | **OP[1:0] =01b:**LPDDR5X SDRAM |
| OP0 | | |

| MR13 | | |
|---|---|---|
| OP7 | | **OP[2]=0b:**Normal operation (default)<br>**1b:** Output the $V_{REF(CA)}$ value on DQ7 and $V_{REF(DQ)}$ value on DQ6 |
| OP6 | | |
| OP5 | | |
| OP4 | | |
| OP3 | | |
| OP2 | VR0 | |
| OP1 | | |
| OP0 | | |

| MR19 | | |
|---|---|---|
| OP7 | | **OP[5] = 1b:**WCK2DQ Osc FM supported |
| OP6 | | |
| OP5 | WCK2DQ Osc FM support | |
| OP4 | | |
| OP3 | | |
| OP2 | | |
| OP1 | | |
| OP0 | | |

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| MR21 | | |
|---|---|---|
| OP7 | WXS | **OP[0] = 1b:** WRITE DATA COPY function supported<br>**OP[1] = 1b:** READ DATA COPY function supported<br>**OP[2] = 1b:** WRITE X function supported<br>**OP[3]** = 1**b:** Device ODTD-CS is supported<br>**OP[7]** = 1**b:** Data to be written can be selected with 0 and 1 |
| OP6 | | |
| OP5 | | |
| OP4 | | |
| OP3 | ODTD-CSFS | |
| OP2 | WXFS | |
| OP1 | RDCFS | |
| OP0 | WDCFS | |

| MR22 | | |
|---|---|---|
| OP7 | RECC | **OP[5:4] = 00b:** Write link ECC disabled (default)<br>**01b:** Write link ECC enabled<br>**OP[7:6] = 00b:** Read link ECC disabled (default)<br>**01b:** Read link ECC enabled |
| OP6 | | |
| OP5 | WECC | |
| OP4 | | |
| OP3 | | |
| OP2 | | |
| OP1 | | |
| OP0 | | |

| MR24 | | |
|---|---|---|
| OP7 | DFES | **OP[3] = 1b:** Device supports Read DCA<br>**OP[7] = 1b:** Devices supports DFE |
| OP6 | | |
| OP5 | | |
| OP4 | | |
| OP3 | Read DCA | |
| OP2 | | |
| OP1 | | |
| OP0 | | |

| MR26 | | |
|---|---|---|
| OP7 | | **OP[6] = 1b**: Read/write-based RDQS_t TRAINING function supported |
| OP6 | RDQSTFS | |
| OP5 | | |
| OP4 | | |
| OP3 | | |
| OP2 | | |
| OP1 | | |
| OP0 | | |

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| MR27 | | |
|---|---|---|
| OP7 | RAAMULT | **OP[0]** = **1b**: RFM is required<br>**OP[5:1]** = **01110b:** 112<br>**OP[7:6]**=**01b:** 4X |
| OP6 | | |
| OP5 | RAAIMT | |
| OP4 | | |
| OP3 | | |
| OP2 | | |
| OP1 | | |
| OP0 | RFM | |

| MR43 | | |
|---|---|---|
| OP7 | | **OP[6] = 1b:** Simultaneous SBE on each DQ byte and DMI are independently counted |
| OP6 | SBEC Rule | |
| OP5 | | |
| OP4 | | |
| OP3 | | |
| OP2 | | |
| OP1 | | |
| OP0 | | |

| MR57 | | |
|---|---|---|
| OP7 | ARFM[3] | **OP[1:0]** = **10b**: 2 x RAAIMT<br>**OP[3:2]** = **00b**: 1=Does not support single-bank mode<br>**OP[7:6]** = **00b**: default (01110b:112), 01b:Level A=01101b: 104,Level B=01100b:96,Level C =01011:88 |
| OP6 | | |
| OP5 | | |
| OP4 | | |
| OP3 | RFMSB | |
| OP2 | | |
| OP1 | RAADEC | |
| OP0 | | |

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**Notes**: *1、 The contents of Product Specific Mode Register definition will reflect information specific to each die in these packages.*

*2、 Refer to General LPDDR5/5X Specifications 1 for mode registers not described here. 3、 Write link ECC and read link ECC are supported.*

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