MP4248

36V, 140W, Buck-Boost with Integrated Low-Side MOSFETs, Supports High-Side Current Sense and I²C Interface

DESCRIPTION

The MP4248 is a buck-boost converter with two integrated low-side MOSFETs (LS-FETs). The device can deliver up to 140W of peak output power at a certain input voltage (V_{IN}) range with excellent efficiency.

The MP4248 is suitable for USB power delivery (PD) applications. It can work with external USB PD controllers via the I²C interface.

The I²C interface and one-time programmable (OTP) memory provide flexibility for configurable features.

Fault condition protections include constant current (CC) current limiting with a high-side (HS) current sense, output over-voltage protection (OVP), and thermal shutdown (TSD).

The MP4248 requires a minimal number of readily available, standard external components, and it is available in a QFN-20 (3mmx5mm) package.

FEATURES

- IEC62368-1 Certified
- 140W Buck-Boost Converter with Integrated Low-Side MOSFETs (LS-FETs)
- Integrated Gate Driver for High-Side MOSFETs (HS-FETs)
- Configurable Input UVLO
- 3.6V to 36V Start-Up Input Voltage Range
- 1V to 36V Output Voltage (V_{OUT}) Range with 1% Accuracy
- Supports 2.8V Falling V_{IN} When V_{OUT} > 3.5V
- Up to 98% Peak Efficiency
- I²C-Configurable V_{REF} Range: 0.1V to 2.147V with 1mV Resolution
- Accurate Output CC Current Limit: ±5%, Supports High-Side (HS) Current Sense
- Accurate Output Current Monitor (IMON)
- Meets USB PD 3.1 EPR AVS and PPS Specification
- Selectable 280kHz, 420kHz, and 580kHz Switching Frequency (f_{SW})
- Selectable Forced PWM Mode or Automatic PFM/PWM Mode
- Output Bias VCC LDO for Higher Efficiency
- Line Drop Compensation via R_{SENS}
- I²C, Alert, and OTP Memory
- EN Shutdown Passive Discharge
- Output OCP, OVP, and Thermal Shutdown Protection
- Available in a QFN-20 (3mmx5mm) Package

MPL Optimized Performance with MPS Inductor MPL-AY1265 Series

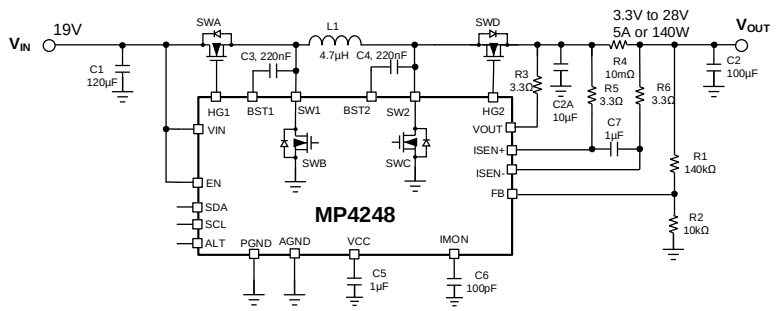
APPLICATIONS

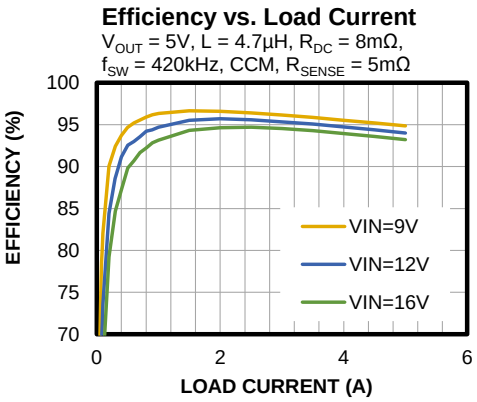
- USB Type-C and USB Power Delivery (PD)
- USB Type-C PD Monitors and Docking Stations
- USB Type-C, USB Type-A Communication Interface, Car Charger
- Wireless Charging

All MPS parts are lead-free, halogen-free, and adhere to the RoHS directive. For MPS green status, please visit the MPS website under Quality Assurance. “MPS”, the MPS logo, and “Simple, Easy Solutions” are trademarks of Monolithic Power Systems, Inc. or its subsidiaries.

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2024 MPS. All Rights Reserved.

TYPICAL APPLICATION





MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2024 MPS. All Rights Reserved.

ORDERING INFORMATION

Part Number*	Package	Top Marking	MSL Rating
MP4248GQV-0000	QFN-20 (3mmx5mm)	*See Below*	1
MP4248GQV-0011			
MP4248GQV-0012			
MP4248GQV-xxxx**			
EVKT-MP4248	Evaluation kit	-	-

* For Tape & Reel, add suffix -Z (e.g. MP4248GQV-xxxx-Z).

** "xxxx" is the configuration code identifier for the register setting stored in the OTP. Each "x" can be a hexadecimal value between 0 and F. The default code is "0000". The MP4248-0011 (address is 67h) and MP4248-0012 (address is 68h) can be used for 140W EPR applications. The MP4248-0011's I²C slave address is 67h; the MP4248-0012's I²C slave address is 68h.

TOP MARKING

MPYW

4248

LLL

MP: MPS prefix
Y: Year code
W: Week code
4248: Part number
LLL: Lot number

EVALUATION KIT (EVKT-MP4248)

EVKT-MP4248 kit contents (items below can be ordered separately):

#	Part Number	Item	Quantity
1	EVL4248-QV-00A	MP4248 evaluation board	1
2	EVKT-USBI2C-02 Bag	Includes USB to I²C communication interface, one USB cable, and one ribbon cable.	1
3	MP4248GQV-0000	IC with default configuration	2
4	Online resources	Include GUI and supplemental files	-

Order directly from MonolithicPower.com or our distributors.

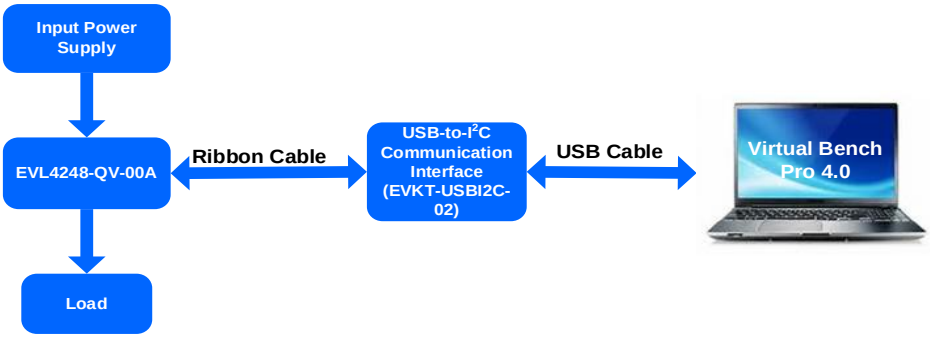
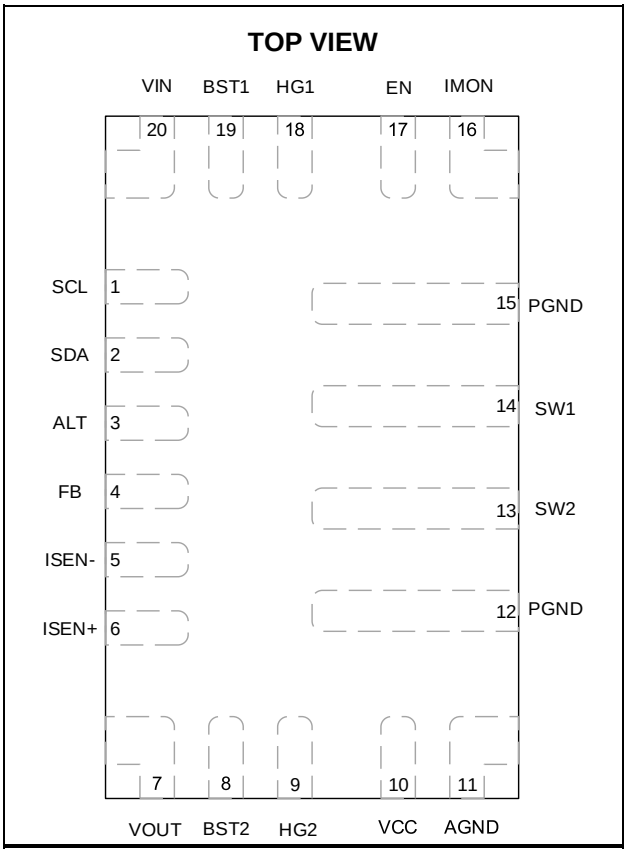


Figure 1: EVKT-MP4248 Evaluation Kit Set-Up

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2024 MPS. All Rights Reserved.

PACKAGE REFERENCE



QFN-20 (3mmx5mm)

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2024 MPS. All Rights Reserved.

PIN FUNCTIONS

Pin #	Name	Description
1	SCL	**I²C clock signal input.**
2	SDA	**I²C data line.**
3	ALT	**I²C alert pin.** Open-drain output, active low.
4	FB	**Feedback pin.** Connect the FB pin to the tap of an external resistor divider, connected from the output to AGND, to set the output voltage.
5	ISEN-	**Negative node of the current-sense signal input.** Place a current-sense resistor between ISEN+ and ISEN-.
6	ISEN+	**Positive node of the current sense-signal input.** Place a current-sense resistor between ISEN+ and ISEN-.
7	VOUT	**Output voltage sense input.** The VOUT pin can also be used to provide the VCC supply under certain output voltage (V_{OUT}) conditions.
8	BST2	**Bootstrap.** A 0.22µF capacitor is connected between SW2 and BST2 to form a floating supply across the high-side switch driver.
9	HG2	**High-side 2 gate drive output for the boost high-side switch (SWD).**
10	VCC	**Internal 5V LDO regulator output.** Decouple the VCC pin with a 0.47µF to 1µF capacitor.
11	AGND	**Analog ground.** Connect AGND to PGND, and connect AGND to the VCC capacitor's ground node.
12, 15	PGND	**Power ground.** PGND requires extra care during PCB layout. Connect PGND to GND with copper traces and vias.
13	SW2	**Switch 2 node of the buck-boost.** Connect SW1 to SW2 with a power inductor. Use a wide PCB trace to make the connection.
14	SW1	**Switch1 node of the buck-boost.** Connect SW1 to SW2 with a power inductor. Use a wide PCB trace to make the connection.
16	IMON	**Current monitor output.** Represent the signal between the ISEN+ and ISEN- pins.
17	EN	**EN input.** Apply a high logic to EN to enable the chip.
18	HG1	**High-side 1 gate drive output for the buck high-side switch (SWA).**
19	BST1	**Bootstrap.** A 0.22µF capacitor is connected between SW1 and BST1 to form a floating supply across the high-side switch driver.
20	VIN	**Supply Voltage for internal logic circuitry but not for power MOSFETs.** Kelvin connect the VIN pin to the SWA MOSFET's drain with a wide PCB trace, and it cannot be affected by another DC/DC converter.

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2024 MPS. All Rights Reserved.

ABSOLUTE MAXIMUM RATINGS (1)

Supply voltage (V_{IN}) ..... -0.4V to +40V
V_{SW1} .....-0.3V (-8V for <10ns) to V_{IN} + 0.3V (+43V for <10ns)
V_{SW2} .....-0.3V (-8V for <10ns) to V_{OUT} + 0.3V (+43V for <10ns)
$V_{BST1/BST2}$, $V_{HG1/HG2}$ .....$V_{SW1/SW2}$ + 6V
V_{OUT}, $V_{ISEN+/ISEN-}$..... -0.3V to +40V
VEN ..... -0.3V to +40V
All other pins..... -0.3V to +6V
Continuous power dissipation (T_A = 25°C) (2) (5)
QFN-20 (3mmx5mm).....6W
Junction temperature (T_J) ..... 150°C
Lead temperature ..... 260°C
Storage temperature..... -65°C to +150°C

ESD Ratings (3)

Human body model (HBM)……..
SW1, HG1, and BST1 .....-2kV to +1.8kV
All other pins……..±2kV
Charged-device model (CDM).....±750V

Recommended Operating Conditions (4)

Operating V_{IN} range ..... 3.6V to 36V
Operating V_{OUT} range..... 1V to 36V
Output current..... 7A
Output power……..140W
Operating junction temp (T_J) .... -40°C to +125°C

Thermal Resistance θ_{JA} θ_{JC}

EVL4248-QV-00A (5)……20.7…2.4…°C/W
QFN-20 (3mmx5mm) (6)……39.1....2.5…°C/W

Notes:

1) Exceeding these ratings may damage the device.
2) The maximum allowable power dissipation is a function of the maximum junction temperature, T_J (MAX), the junction-to-ambient thermal resistance, θ_{JA}, and the ambient temperature, T_A. The maximum allowable continuous power dissipation at any ambient temperature is calculated by P_D (MAX) = (TJ (MAX) - T_A) / θ_{JA}. Exceeding the maximum allowable power dissipation can cause excessive die temperature, and the regulator may go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
3) HBM, per JEDEC specification JESD22-A114; CDM, per JEDEC specification JESD22-C101. JEDEC document JEP155 states that 500V HBM allows safe manufacturing with a standard ESD control process. JEDEC document JEP157 states that 250V CDM allows safe manufacturing with a standard ESD control process.
4) The device is not guaranteed to function outside of its operating conditions. The output power can reach 140W for V_{IN} ≥19V applications. Thermal derating must be considered for different SWA/SWB selections and PCB size.
5) Measured on the EVL4248-QV-00A, 4-layer PCB, 64mmx64mm.
6) Measured on a JESD51-7, 4-layer PCB. The value of θ_{JA} given in this table is only valid for comparison with other packages and cannot be used for design purposes. These values were calculated in accordance with JESD51-7, and simulated on a specified JEDEC board. They do not represent the performance obtained in an actual application.

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2024 MPS. All Rights Reserved.

ELECTRICAL CHARACTERISTICS

V_{IN} = 12V, V_{EN} = 5V, T_J = -40°C to +125°C (7), typical value is tested at T_J = 25°C, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
Supply current (shutdown)	I_{Q_STD}	V_{EN} = 0V		1	10	μA
Supply current (quiescent)	I_{Q1}	No switching, I²C set OPERATION on, EN on, PFM mode, T_J = 25°C		775	1500	μA
	I_{Q2}	I²C set operation = off, EN on, T_J = 25°C		135	300	μA
EN rising threshold	V_{EN_RISING}	EN to enable switching	-5%	1.22	+5%	V
EN hysteresis	V_{EN_HYS}			200		mV
EN pull-down resistor	R_{EN}	EN = 2V		1.9	3	MΩ
Thermal shutdown (8)	T_{STD}			160		°C
Thermal hysteresis (8)	T_{STD_HYS}			20		°C
VCC regulator	V_{CC}		4.85	5.15	5.45	V
VCC load regulation	V_{CC_LOG}	I_{CC} = 50mA		2	5	%
VCC power source change threshold	V_{CC_VTH}	V_{IN} = 12V, ramp V_{OUT} from 5V to 10V	6.4	6.8	7.2	V
V_{CC} under-voltage lockout (UVLO) threshold rising	$V_{CC_UVLO_R}$		3.15	3.35	3.55	V
V_{CC} UVLO threshold hysteresis	$V_{CC_UVLO_HYS}$			150		mV
V_{IN} UVLO falling threshold	V_{UVLO_VIN}		2.35	2.56	2.75	V
Buck-Boost Converter						
Switch B on resistance	$R_{DS_ON_B}$			20	45	mΩ
Switch C on resistance	$R_{DS_ON_C}$			14	35	mΩ
Feedback voltage	V_{FB1}		-3%	330	+3%	mV
	V_{FB2}		-2%	500	+2%	mV
	V_{FB3}		-1.5%	2	+1.5%	V
Output absolute over-voltage protection (OVP) rising threshold	$V_{OUT_OVP_ABS}$	Trim option 1, T_J = 25°C	24.5	26.5	28.5	V
		Trim option 2, T_J = 25°C	37	39	41	V
Output absolute OVP hysteresis	$V_{OUT_OVP_ABS_HYS}$	Trim option 1, T_J = 25°C		670		mV
		Trim option 2, T_J = 25°C		920		mV
Output OVP rising threshold	V_{OUTOVP_R}		114%	120%	126%	V_{FB}
Output OVP hysteresis	$V_{OUT_OVP_HYS}$			10%		V_{FB}

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2024 MPS. All Rights Reserved.

ELECTRICAL CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{EN} = 5V, T_J = -40°C to +125°C (7), typical value is tested at T_J = 25°C, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
Switch leakage	SW_{LKG}	V_{EN} = 0V, V_{SW1} = 36V, V_{SW2} = 36V, T_J = 25°C			1	μA
		V_{EN} = 0V, V_{SW1} = 36V, V_{SW2} = 36V, T_J = -40°C to+125°C (7)			15	
Oscillator frequency	f_{SW1}	T_J = 25°C	220	280	340	kHz
	f_{SW2}	T_J = 25°C	340	420	500	
	f_{SW3}	T_J = 25°C	480	580	680	
Frequency dithering span	f_{SRANGE}	2kHz triangle modulation, T_J = 25°C		±8		%
Hiccup off timer (8)	t_{HICCUP}	V_{REF} = 0.5V		50		ms
Soft-start time	t_{SS}	Output from 10% to 90%, V_{OUT} = 5V, constant slew rate for other V_{REF}		1		ms
Minimum on time (8)	$t_{ON_MIN_BT}$	Boost SWC		180		ns
Minimum off time (8)	t_{OFF_MIN}	Buck SWB		180		ns
ISENS over-current (OC) threshold	I_{OC1}	OC threshold = 1A, R_{SENS} = 5mΩ, T_J = -40°C to +125°C	4.25	5	5.75	mV
	I_{OC2}	OC threshold=3A, R_{SENS} = 5mΩ, T_J = -40°C to +125°C	-5%	15	+5%	mV
	I_{OC3}	OC threshold = 5A, R_{SENS} = 5mΩ, T_J = -40°C to +125°C	-5%	25	+5%	mV
Low-side B valley limit (8)	I_{LIMIT2}	Switch B, VALLEY_CL = 01b, T_J = -40°C to +125°C		9		A
Low-side C current limit (8)	I_{LIMIT3}	Switch C, PEAK_CL = 01b, T_J = -40°C to +125°C		12		A
V_{OUT} under-voltage (UV) threshold to enter hiccup mode	$V_{OUT_UV_HICCUP}$		-5%	2.93	+5%	V
Line drop compensation	V_{DROP}	I_{OUT} = 1A		100		mV
Output discharge resistor	R_{DISCHG}			65		Ω
Mode Transition Threshold						
Buck-boost to buck transition threshold (8)	V_{MODE_TH2}	V_{IN} / V_{OUT}		120		%
Buck-boost to boost transition hysteresis (8)	V_{MODE_HYS2}	V_{IN} / V_{OUT}		82		%
High-Side Gate Driver						
Gate source current capability (8)	I_{DR1H_SRC}	V_{BST-SW} = 5.2V, 4.7nF load		0.8		A
	I_{DR2H_SRC}	V_{BST-SW} = 5.2V, 4.7nF load		1.2		A
Gate source resistance	R_{DR1H_SRC}	V_{BST-SW} = 5.2V		3	5	Ω
	R_{DR2H_SRC}	V_{BST-SW} = 5.2V		2	3	Ω

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2024 MPS. All Rights Reserved.

ELECTRICAL CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{EN} = 5V, T_J = -40°C to +125°C (7), typical value is tested at T_J = 25°C, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
Gate sink current capability (8)	I_{DR1H_SIN}	V_{BST-SW} = 5.2V, 4.7nF load		1.8		A
	I_{DR2H_SIN}	V_{BST-SW} = 5.2V, 4.7nF load		3.3		A
Gate sink resistance	R_{DR1H_SIN}			1	2	Ω
	R_{DR2H_SIN}			1	2	Ω
Dead time of two edges (8)	$t_{DHS1_HS3_RISE}$	Body-diode conduct current duration		12		ns
	$t_{DHS2_HS4_FALLING}$	Body-diode conduct current duration		20		ns
ALT pin leakage	I_{ALT_LKG}	V_{ALT} = 5V		0.1		μA
ALT pin pull low resistance	R_{ALT}				20	Ω
I²C Interface Specification (8)						
Input logic high	V_{IH}		1.35			V
Input logic low	V_{IL}				0.9	V
Output voltage logic low	V_{OUT_L}				0.4	V
SCL clock frequency	f_{SCL}			400	1000	kHz
SCL high time	t_{HIGH}		60			ns
SCL low time	t_{LOW}		160			ns
Data set-up time	t_{SU_DAT}		10			ns
Data hold time	t_{HD_DAT}		0	60		ns
Setup time for (repeated) start command	t_{SU_STA}		160			ns
Hold time for (repeated) start command	t_{HD_STA}		160			ns
Bus free time between a start and a stop command	t_{BUF}		160			ns
Setup time for stop command	t_{SU_STO}		160			ns
Rise time of SCL and SDA	t_R		10		300	ns
Fall time of SCL and SDA	t_F		10		300	ns
Pulse width of suppressed spike	t_{SP}		0		50	ns
Capacitance for each bus line	C_B				400	pF
Power Good (PG) Indication						
PG lower rising threshold	$V_{PG_R_L}$	PG switches high	88.5%	93%	98.5%	V_{FB}
PG lower falling threshold	$V_{PG_F_L}$	PG switches low	77%	82.5%	88%	V_{FB}
PG upper rising threshold	$V_{PG_R_H}$	PG switches low	115%	120%	126%	V_{FB}
PG upper falling threshold	$V_{PG_F_H}$	PG switches high	105%	110%	115%	V_{FB}

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2024 MPS. All Rights Reserved.

ELECTRICAL CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{EN} = 5V, T_J = -40°C to +125°C (7), typical value is tested at T_J = 25°C, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
Current Monitor Function						
IMON output voltage gain	G_{IMON1}	I²C set R_{SENS} = 5mΩ, 25mV sense voltage, T_A = 25°C	-3%	68	+3%	V/V
IMON output voltage gain	G_{IMON2}	I²C set R_{SENS} = 10mΩ, 50mV sense voltage, T_A = 25°C	-3%	34	+3%	V/V

Notes:

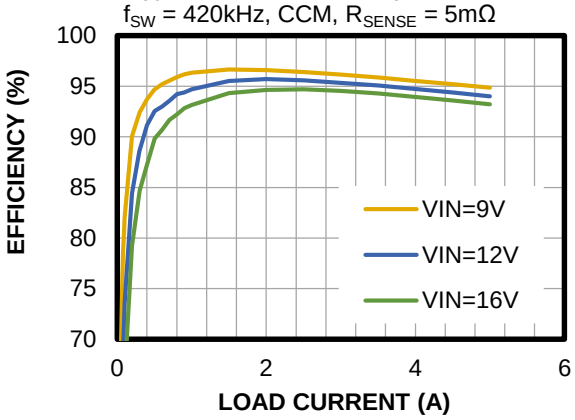
7) All minimum and maximum parameters are tested at T_J = 25°C. Over-temperature limits are guaranteed by characterization and correlation.
8) Guaranteed by characterization.

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2024 MPS. All Rights Reserved.

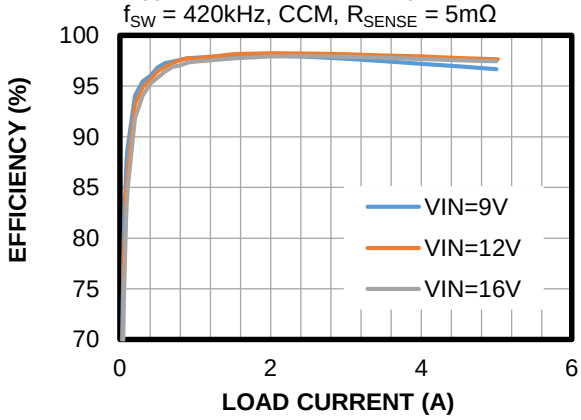
TYPICAL CHARACTERISTICS

V_{IN} = 12V, V_{OUT} = 5V, L = 4.7µH, f_{SW} = 420kHz, forced PWM mode, T_A = 25°C, unless otherwise noted.

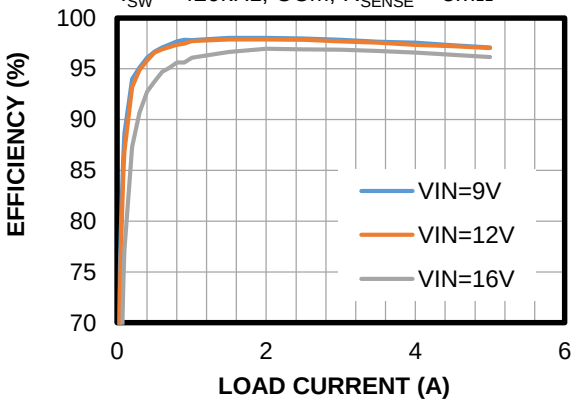
Efficiency vs. Load Current
V_{OUT} = 5V, L = 4.7µH, R_{DC} = 8mΩ, f_{SW} = 420kHz, CCM, R_{SENSE} = 5mΩ



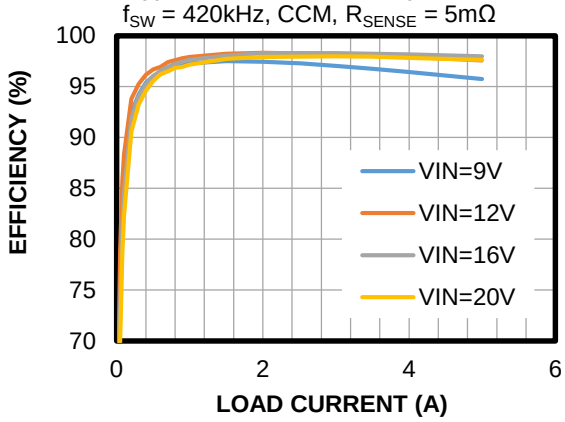
Efficiency vs. Load Current
V_{OUT} = 12V, L = 4.7µH, R_{DC} = 8mΩ, f_{SW} = 420kHz, CCM, R_{SENSE} = 5mΩ



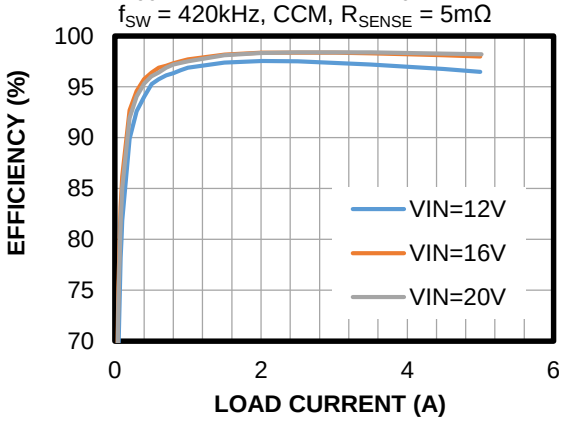
Efficiency vs. Load Current
V_{OUT} = 9V, L = 4.7µH, R_{DC} = 8mΩ, f_{SW} = 420kHz, CCM, R_{SENSE} = 5mΩ



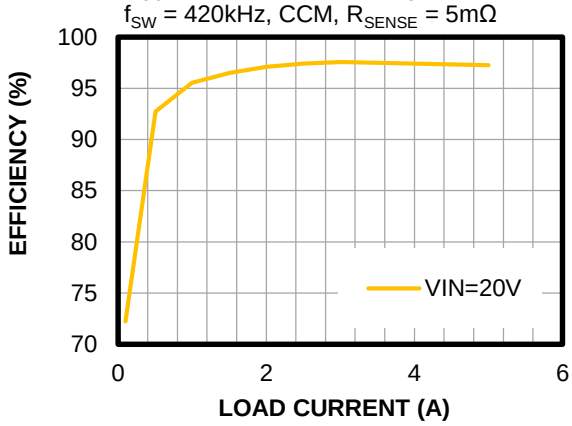
Efficiency vs. Load Current
V_{OUT} = 15V, L = 4.7µH, R_{DC} = 8mΩ, f_{SW} = 420kHz, CCM, R_{SENSE} = 5mΩ



Efficiency vs. Load Current
V_{OUT} = 20V, L = 4.7µH, R_{DC} = 8mΩ, f_{SW} = 420kHz, CCM, R_{SENSE} = 5mΩ



Efficiency vs. Load Current
V_{OUT} = 28V, L = 4.7µH, R_{DC} = 8mΩ, f_{SW} = 420kHz, CCM, R_{SENSE} = 5mΩ



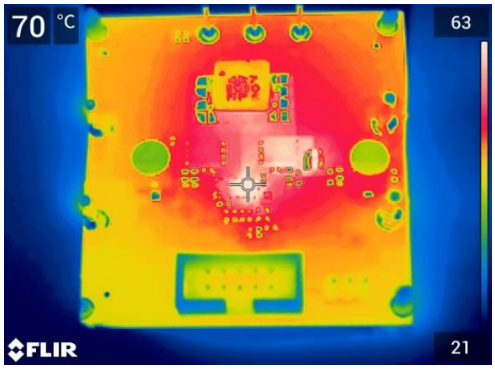
MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2024 MPS. All Rights Reserved.

TYPICAL CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{OUT} = 5V, L = 4.7µH, f_{SW} = 420kHz, forced PWM mode, T_A = 25°C, unless otherwise noted.

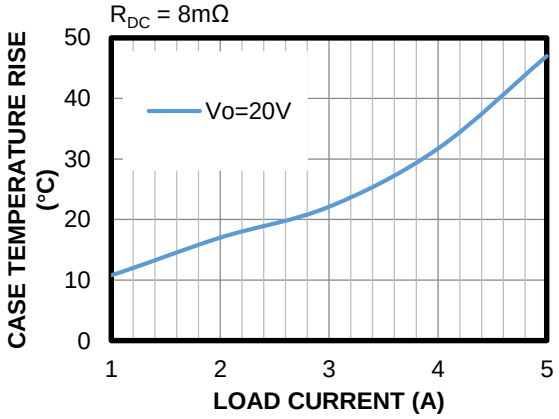
Case Temperature

V_{IN} = 20V, V_{OUT} = 28V, I_{OUT} = 5A, f_{SW} = 420KHZ, L = 4.7µH



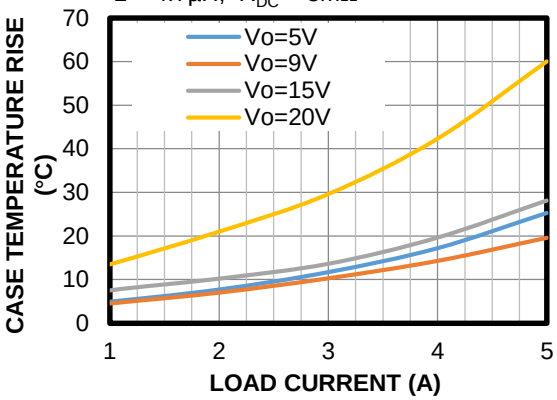
Case Temperature Rise

V_{IN} = 12V, V_{OUT} = 20V, f_{SW} = 280kHz, based on 6cmx6cm board, L = 6.8µH, R_{DC} = 8mΩ



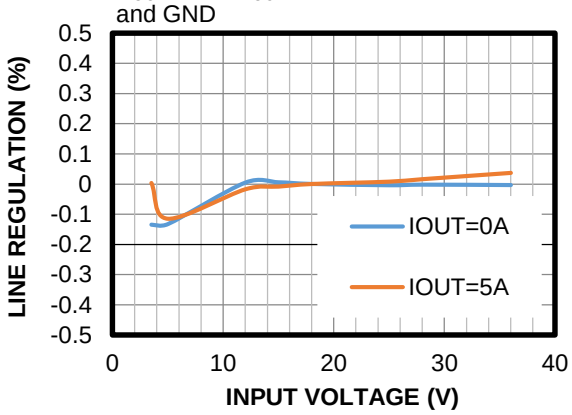
Case Temperature Rise

V_{IN} = 12V, V_{OUT} = 5V/9V/15V/20V, f_{SW} = 420kHz, based on 6cmx6cm board, L = 4.7µH, R_{DC} = 8mΩ



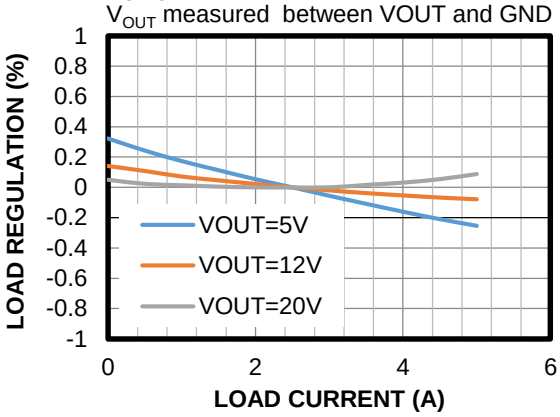
Line Regulation

V_{OUT} = 5V, V_{OUT} measured between VOUT and GND

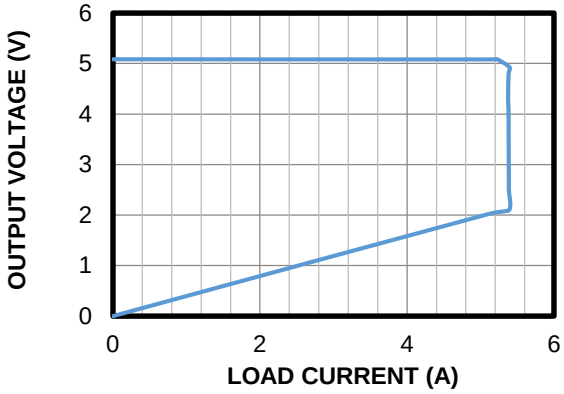


Load Regulation

R_{SENSE} = 5mΩ, no line drop compensation, V_{OUT} measured between VOUT and GND



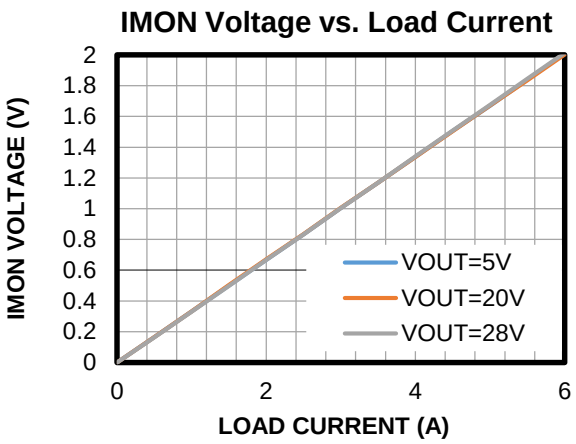
CC/CV Curve

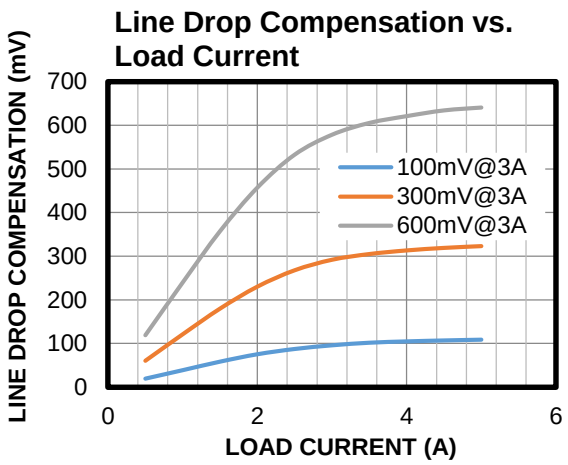


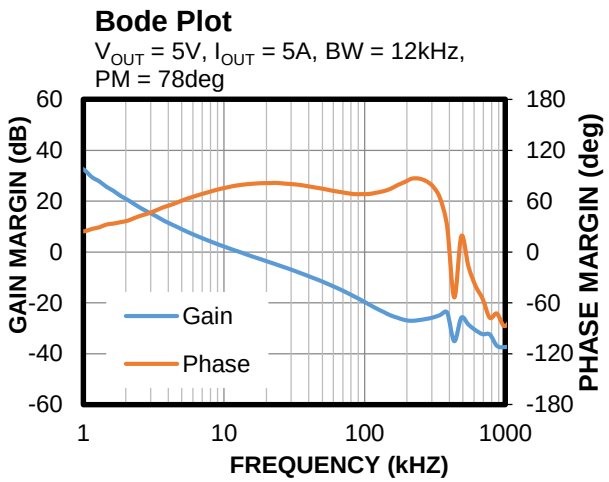
MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2024 MPS. All Rights Reserved.

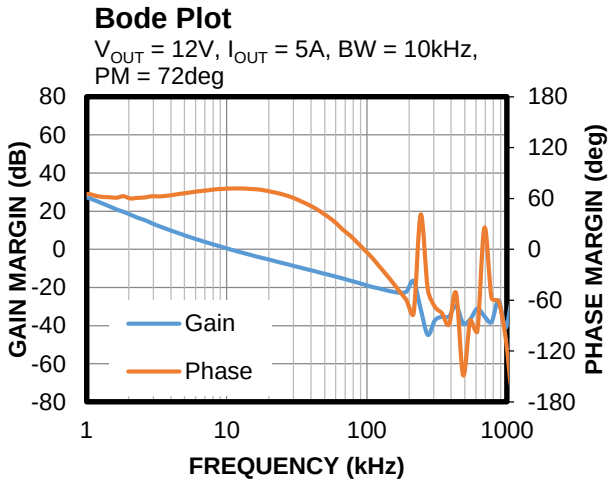
TYPICAL CHARACTERISTICS *(continued)*

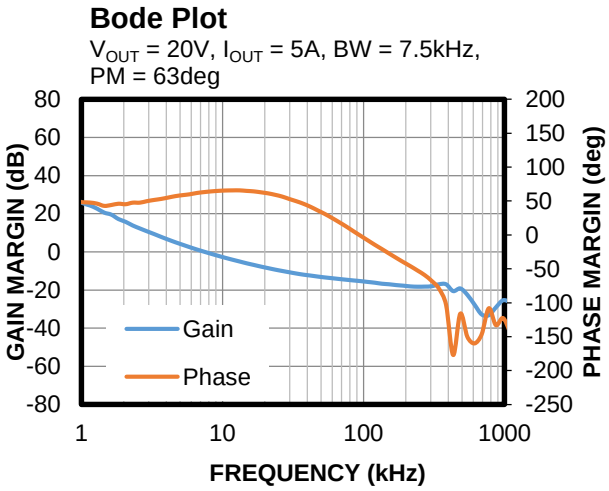
V_{IN} = 12V, V_{OUT} = 5V, L = 4.7μH, f_{SW} = 420kHz, forced PWM mode, T_A = 25°C, unless otherwise noted.











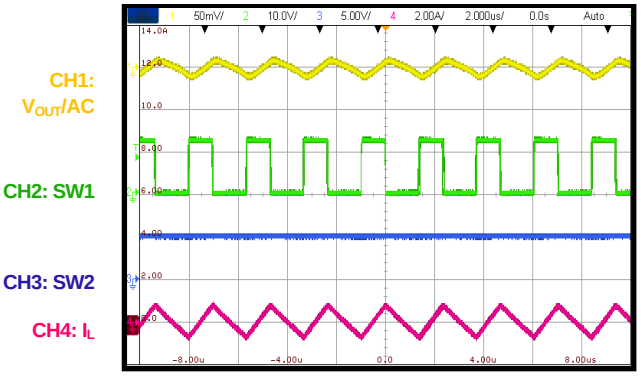
MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2024 MPS. All Rights Reserved.

TYPICAL PERFORMANCE CHARACTERISTICS

V_{IN} = 12V, V_{OUT} = 5V, L = 4.7μH, f_{SW} = 420kHz, forced PWM mode, T_A = 25°C, unless otherwise noted.

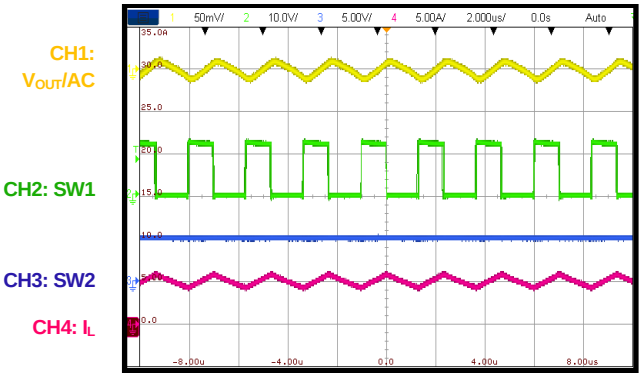
Output Voltage Ripple

V_{OUT} = 5V, load = 0A



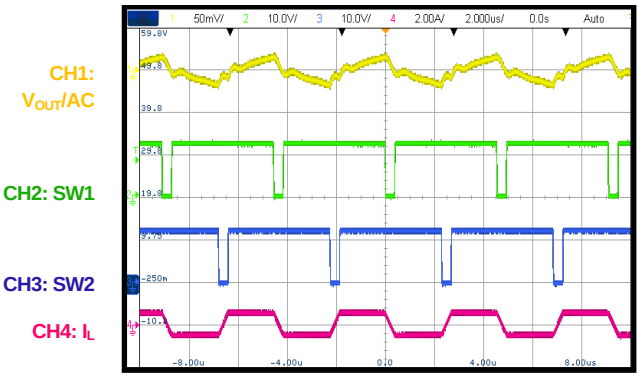
Output Voltage Ripple

V_{OUT} = 5V, load = 5A



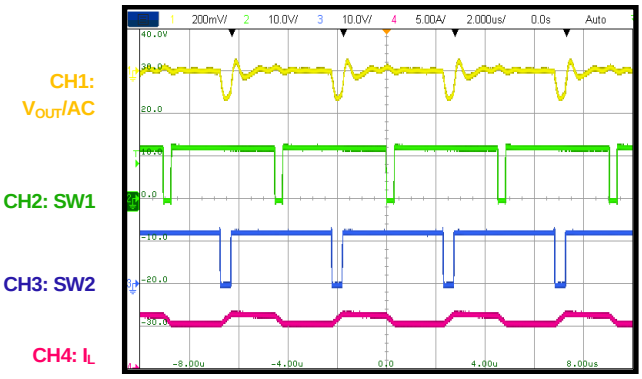
Output Voltage Ripple

V_{OUT} = 12V, load = 0A, f_{SW} decreased to half its value in buck-boost mode



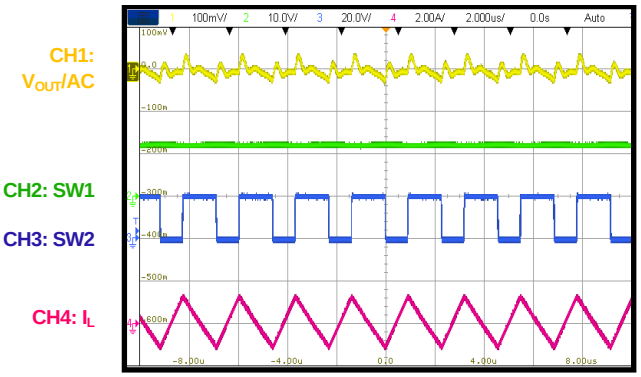
Output Voltage Ripple

V_{OUT} = 12V, load = 5A, f_{SW} decreased to half its value in buck-boost mode



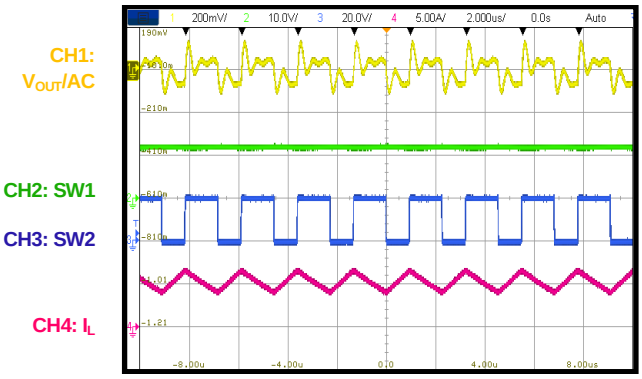
Output Voltage Ripple

V_{OUT} = 20V, load = 0A



Output Voltage Ripple

V_{OUT} = 20V, load = 3A

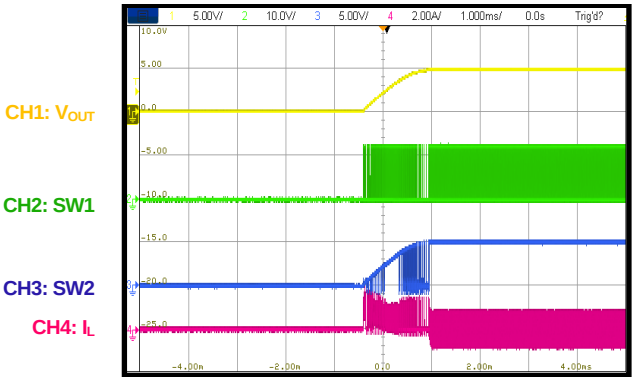


MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2024 MPS. All Rights Reserved.

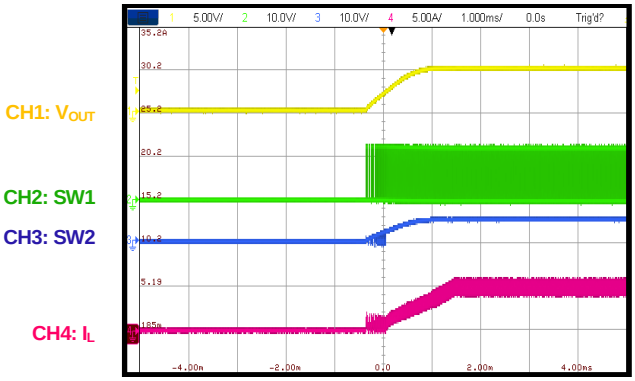
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{OUT} = 5V, L = 4.7μH, f_{SW} = 420kHz, forced PWM mode, T_A = 25°C, unless otherwise noted.

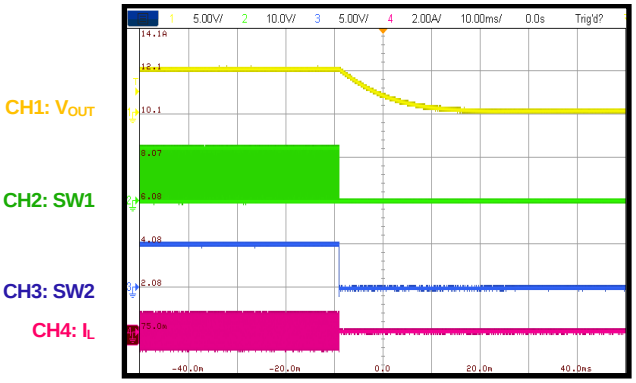
I²C Operation On
Load = 0A



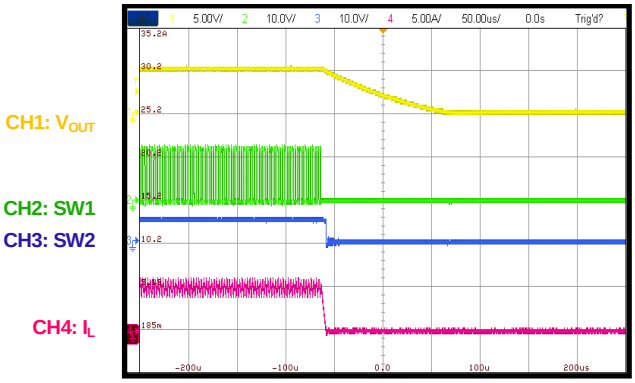
I²C Operation On
Load = 5A



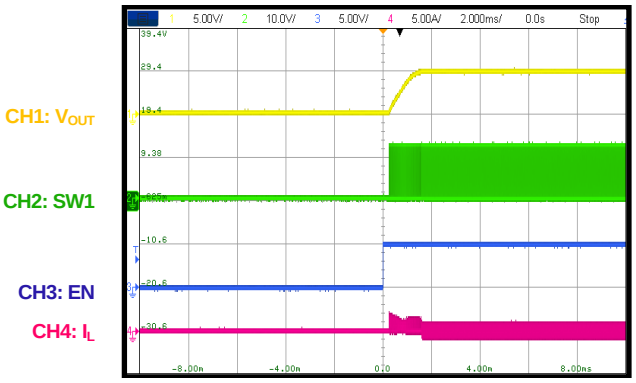
I²C Operation Off
Load = 0A



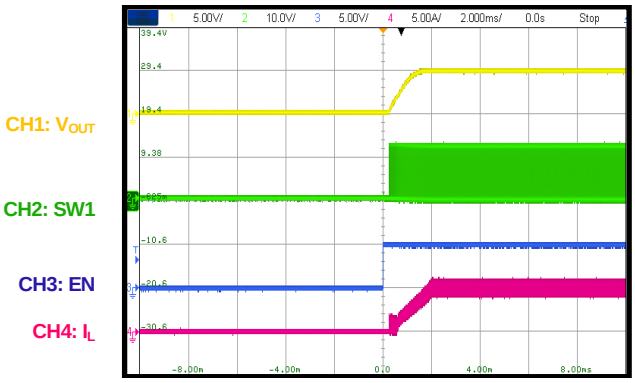
I²C Operation Off
Load = 5A



EN Pin Enabled
Load = 0A



EN Pin Enabled
Load = 5A

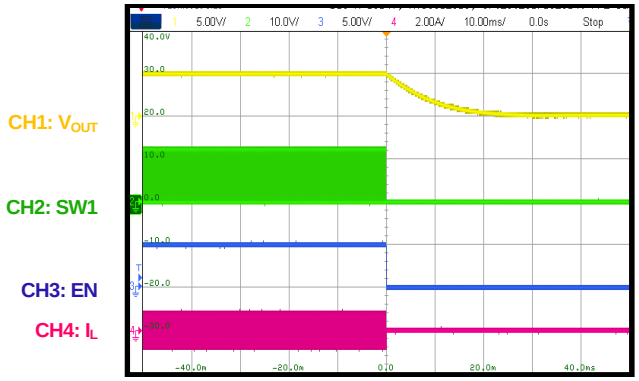


MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2024 MPS. All Rights Reserved.

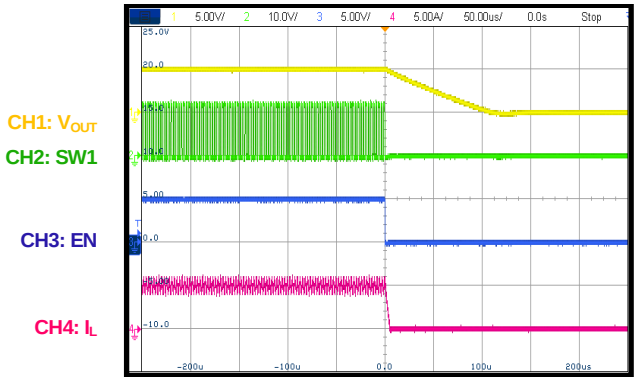
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{OUT} = 5V, L = 4.7μH, f_{SW} = 420kHz, forced PWM mode, T_A = 25°C, unless otherwise noted.

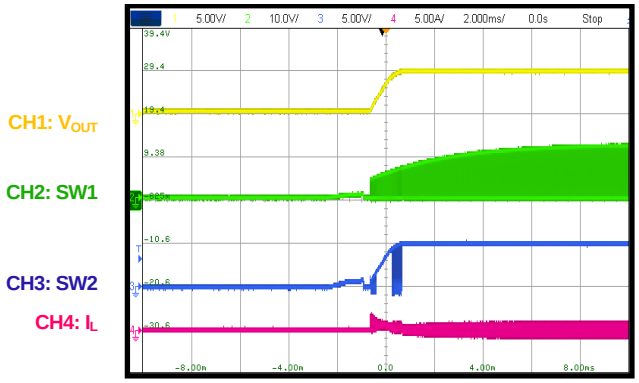
EN Pin Disabled
Load = 0A



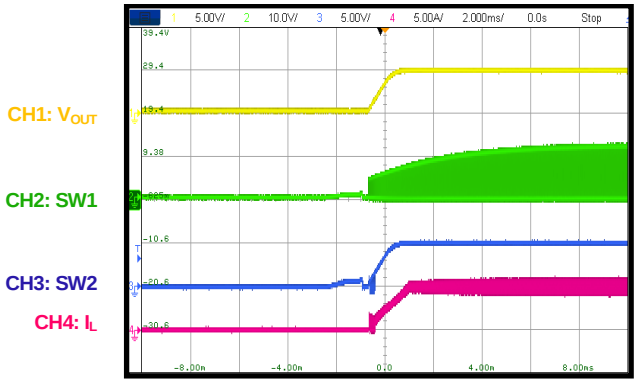
EN Pin Disabled
Load = 5A



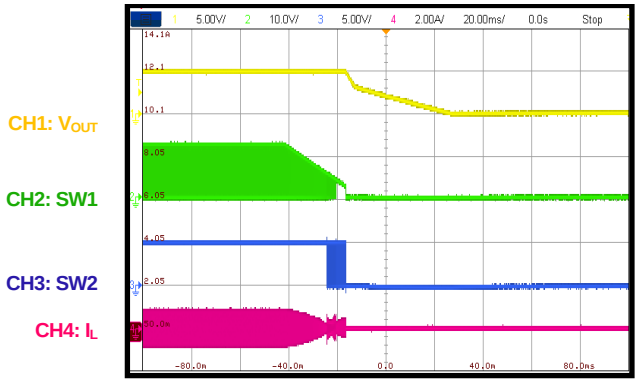
Input Start-Up
Load = 0A



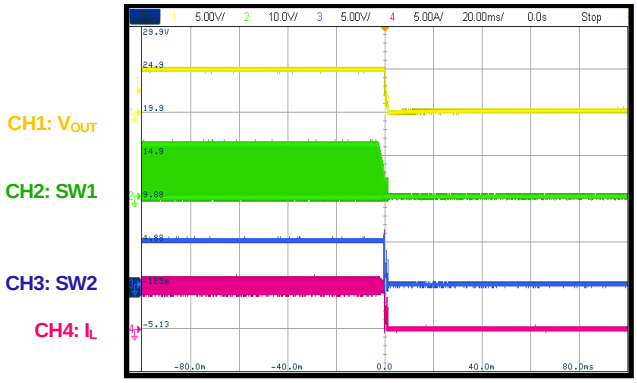
Input Start-Up
Load = 5A



Input Shutdown
Load = 10mA



Input Shutdown
Load = 5A



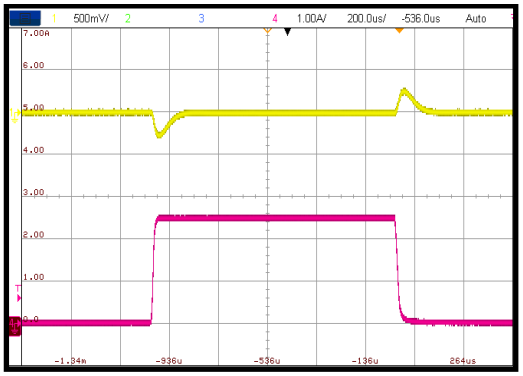
MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2024 MPS. All Rights Reserved.

TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{OUT} = 5V, L = 4.7μH, f_{SW} = 420kHz, forced PWM mode, T_A = 25°C, unless otherwise noted.

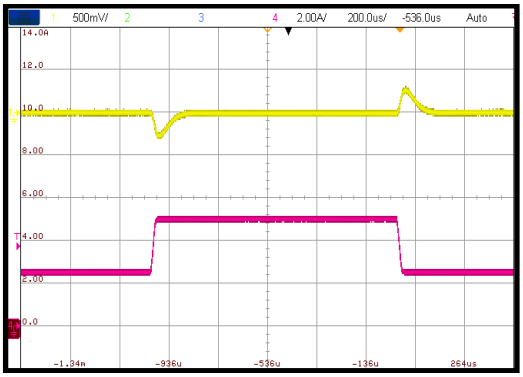
Load Transient Response

V_{IN} = 12V, V_{OUT} = 5V, I_{OUT} = 0A to 2.5A, 150mA/μs



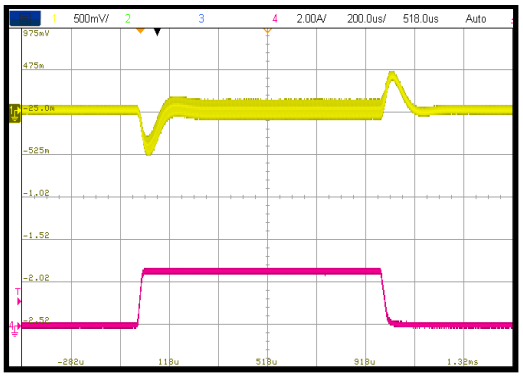
Load Transient Response

V_{IN} = 12V, V_{OUT} = 5V, I_{OUT} = 2.5A to 5A, 150mA/μs



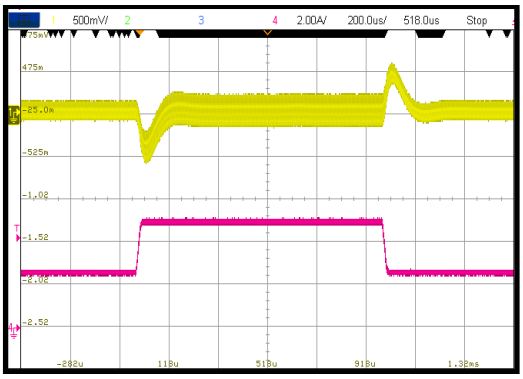
Load Transient Response

V_{IN} = 12V, V_{OUT} = 20V, I_{OUT} = 0A to 2.5A, 150mA/μs



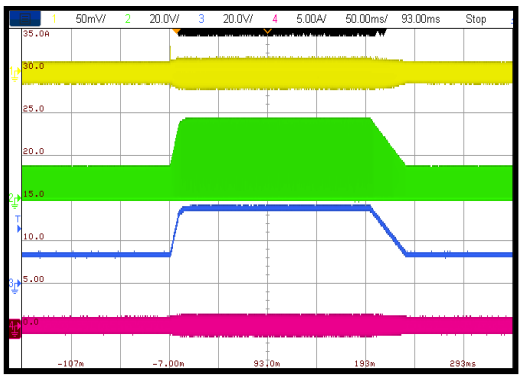
Load Transient Response

V_{IN} = 12V, V_{OUT} = 20V, I_{OUT} = 2.5A to 5A, 150mA/μs



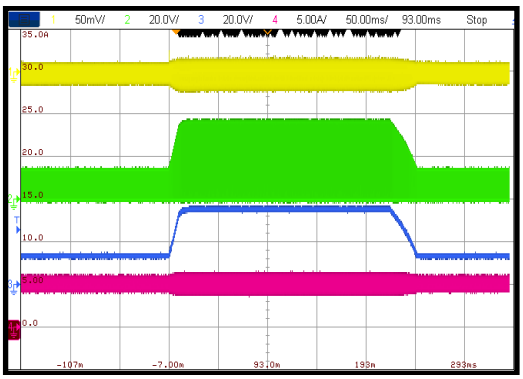
Input Voltage Transient Response

V_{IN} = 14V to 35V, V_{OUT} = 5V, load = 0A



Input Voltage Transient Response

V_{IN} = 14V to 35V, V_{OUT} = 5V, load = 5A



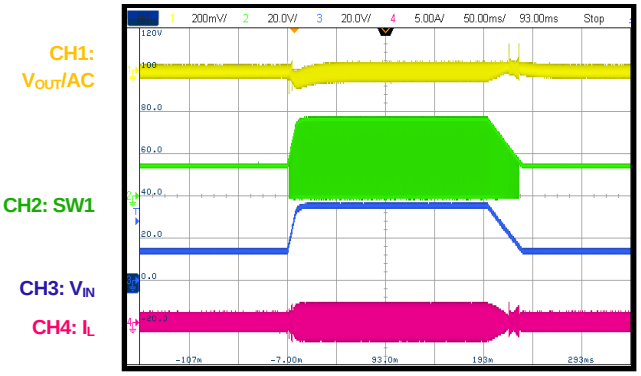
MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2024 MPS. All Rights Reserved.

TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{OUT} = 5V, L = 4.7μH, f_{SW} = 420kHz, forced PWM mode, T_A = 25°C, unless otherwise noted.

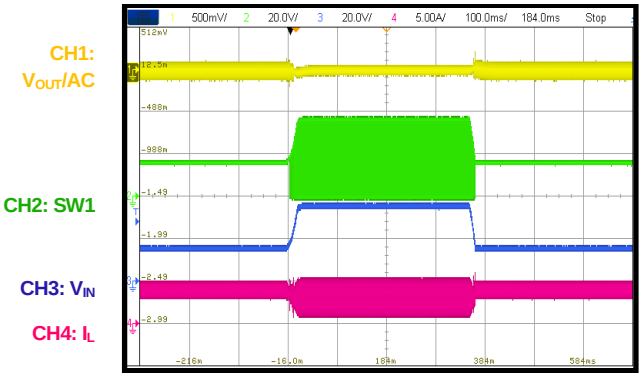
Input Voltage Transient

V_{IN} = 14V to 35V, V_{OUT} = 20V, load = 0A



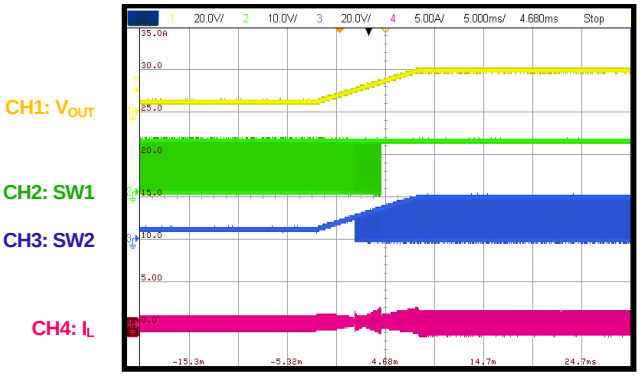
Input Voltage Transient

V_{IN} = 14V to 35V, V_{OUT} = 20V, load = 3A



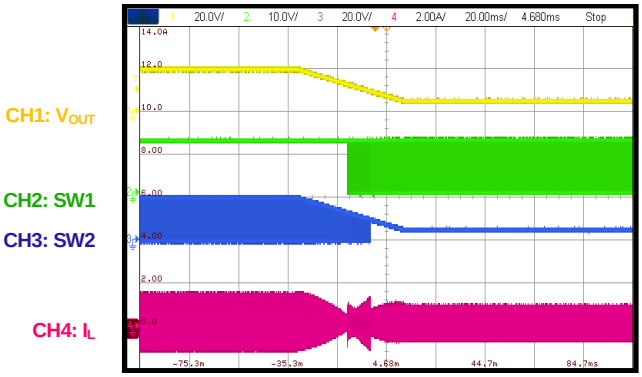
Output Voltage Transition

V_{OUT} = 5V to 20V, I_{OUT} = 0A



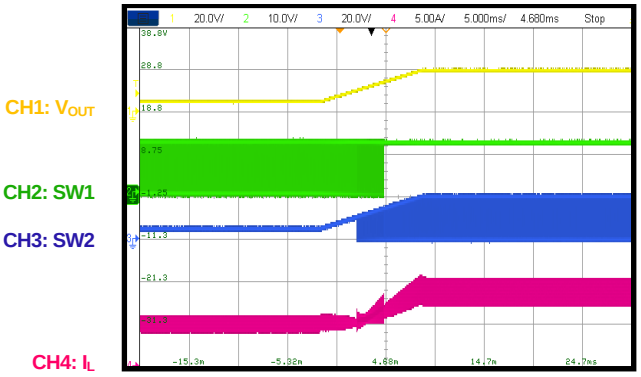
Output Voltage Transition

V_{OUT} = 20V to 5V, I_{OUT} = 0A



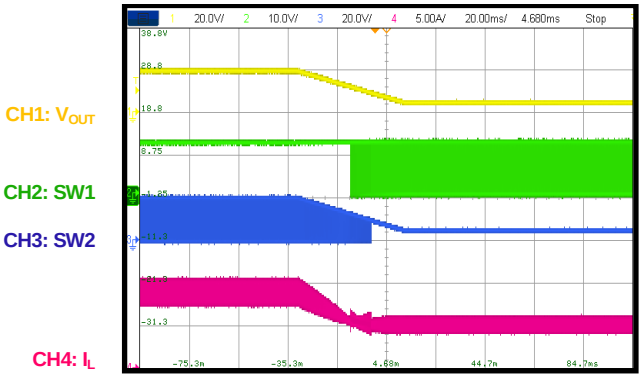
Output Voltage Transition

V_{OUT} = 5V to 20V, I_{OUT} = 3A



Output Voltage Transition

V_{OUT} = 20V to 5V, I_{OUT} = 3A



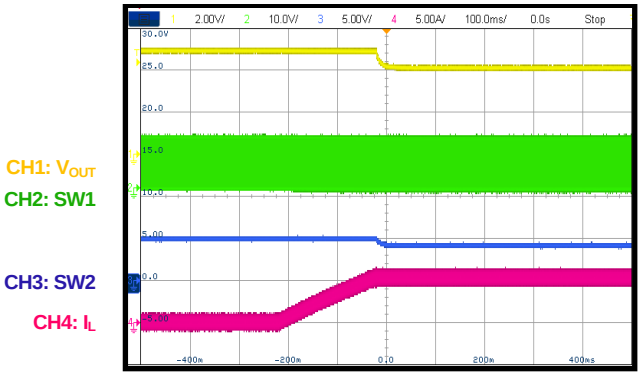
MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2024 MPS. All Rights Reserved.

TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{OUT} = 5V, L = 4.7μH, f_{SW} = 420kHz, forced PWM mode, T_A = 25°C, unless otherwise noted.

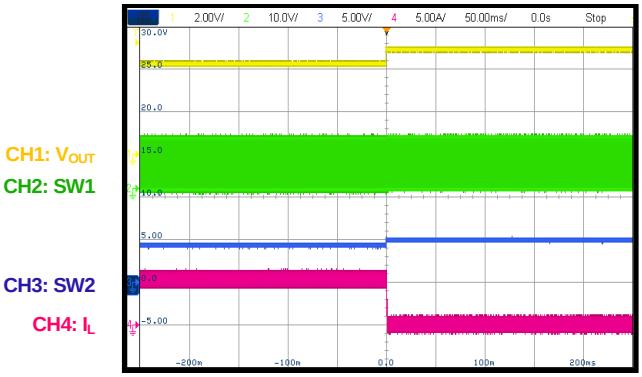
CC Entry

CV load = 4V, CC limit = 5.4A

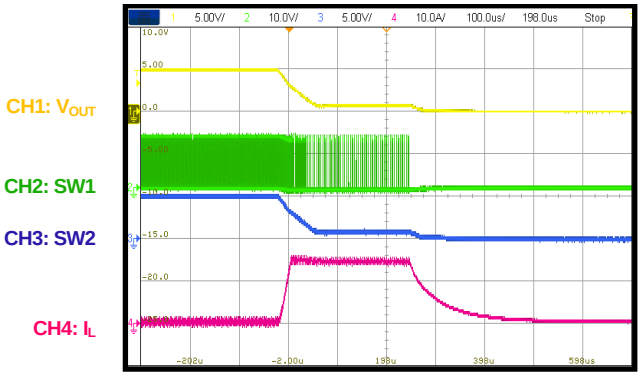


CC Recovery

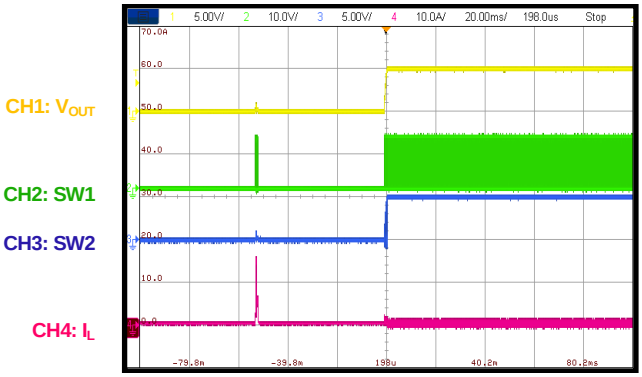
CV load = 4V, CC limit = 5.4A



Short-Circuit Protection Entry



Short-Circuit Protection Recovery



MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2024 MPS. All Rights Reserved.

FUNCTIONAL BLOCK DIAGRAM

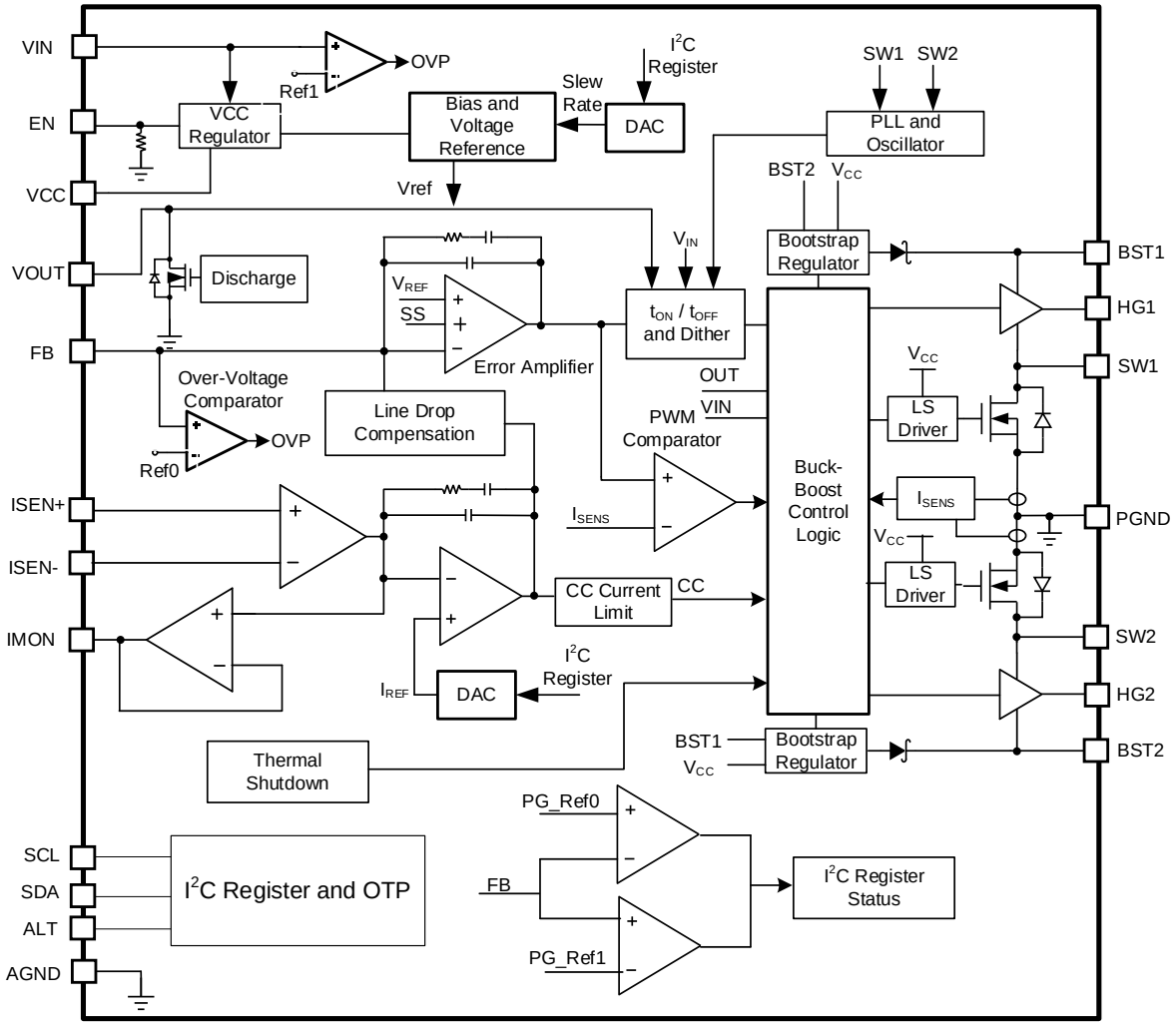


Figure 2: Functional Block Diagram

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2024 MPS. All Rights Reserved.

OPERATION

The MP4248 is a buck-boost converter with integrated low-side MOSFETs (LS-FETs). The device operates with a fixed frequency for all modes (buck, boost, and buck-boost). A special buck-boost control strategy provides high efficiency across the full input range, with a smooth transient between different modes. Figure 2 on page 20 shows the internal block diagram.

Buck-Boost Operation

The MP4248 can regulate the output voltage (V_{OUT}) above, equal to, or below the input voltage (V_{IN}). The device has a one inductor, four-switch (SWA, SWB, SWC, and SWD) power structure (see Figure 3).

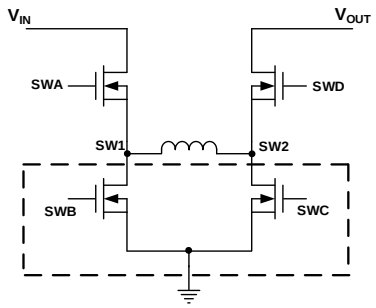


Figure 3: Buck-Boost Topology

Based on this architecture, the MP4248 can operate in buck mode, boost mode, or buck-boost mode with different V_{IN} inputs (see Figure 4).

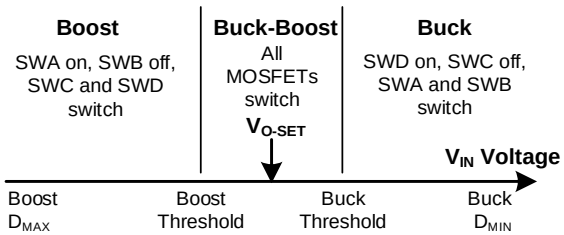


Figure 4: Buck-Boost Operation Range

Buck Mode (V_{IN} > V_{OUT})

When V_{IN} is significantly greater than V_{OUT}, the MP4248 works in buck mode. SWA and SWB switch for buck regulation. Meanwhile, SWC is off, and SWD remains on to conduct the inductor current (I_L).

In each buck mode cycle, SWA first turns on when the FB voltage (V_{FB}) drops below the reference voltage (V_{REF}). After SWA turns off, SWB turns on to conduct I_L until it triggers the COMP control signal. By repeating this operation, the converter regulates V_{OUT}.

Boost Mode (V_{IN} < V_{OUT})

When V_{IN} is significantly lower than V_{OUT}, the MP4248 operates in boost mode. In boost mode, SWC and SWD switch for boost regulation. Meanwhile, SWB is off, and SWA remains on to conduct I_L.

In each boost mode cycle, SWC turns on to conduct I_L. When I_L rises and triggers the control signal on the COMP pin, SWC turns off and SWD turns on for the freewheel current. Then SWC turns on and off repeatedly to regulate V_{OUT}.

Buck-Boost Mode (V_{IN} ≈ V_{OUT})

When V_{IN} is almost equal to V_{OUT}, the converter cannot provide enough energy to the load in buck mode due to SWA's minimum off time (see Figure 5). In boost mode, the converter supplies too much power to the load due to SWC's minimum on time. Under these conditions, the MP4248 utilizes buck-boost control to regulate the output.

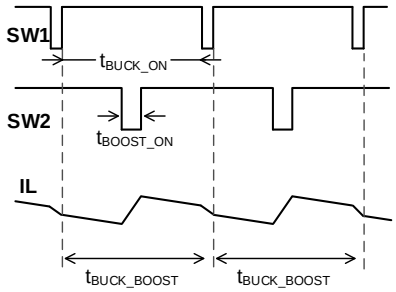


Figure 5: Buck-Boost Waveform

If V_{IN} is almost equal to V_{OUT}, the device operates in buck-boost mode, and one boost switching cycle is inserted into each buck switching period. The MOSFETs turn on in the following sequence:

1. SWA and SWD
2. SWA and SWC
3. SWA and SWD
4. SWB and SWD

This process allows I_L to meet the COMP voltage (V_{COMP}) requirement while also supplying sufficient current to the output.

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2024 MPS. All Rights Reserved.

Working Mode Selection

The MP4248 works with a fixed frequency under heavy-load conditions. When the load current decreases, the MP4248 can operate in forced continuous conduction mode (FCCM) or pulse-skip mode (PSM) based on the MODE register setting.

Forced Continuous Conduction Mode (FCCM) (Or Forced PWM)

When the MP4248 works in FCCM, the buck on time and boost off time are determined by the internal circuit to achieve a fixed frequency based on the V_{IN} / V_{OUT} ratio. When the load decreases, the average input current (I_{IN}) drops, and I_L may go negative from VOUT to VIN during the off time (while SWD is on). This forces I_L to work in FCCM with a fixed frequency, which produces a lower output voltage ripple than in PSM.

Pulse-Skip Mode (PSM) (Auto-PFM/PWM)

Once I_L drops to 0A in PSM, SWD turns off to prevent the current from flowing from VOUT to GND. This forces I_L to work in discontinuous conduction mode (DCM). Simultaneously, the internal off-time clock becomes longer once the MP4248 enters DCM. When the I_L conduction period decreases, the frequency drops, which saves power loss and reduces the output voltage ripple.

If V_{COMP} drops to the PSM threshold, the MP4248 stops switching to reduce switching power loss. The MP4248 resumes switching once V_{COMP} exceeds the PSM threshold. The switching pulse skip is based on V_{COMP} under very light-load conditions. PSM has a higher efficiency than FCCM under light loads, but the output voltage ripple may be higher due to the group switching pulse.

Power Supply

The MP4248 internal circuit (including the gate drivers) is powered by VCC. When V_{IN} is sufficient and EN is high, the MP4248 tries to regulate the VCC voltage (V_{CC}) at 5V. V_{CC} and BST have separate under-voltage lockout (UVLO) thresholds that can keep the gate signal off.

If V_{IN} and V_{OUT} both exceed 6.8V, then the MP4248 powers VCC from the lower voltage source between the two values to reduce power loss. If V_{IN} and V_{OUT} both exceed 6.8V, the MP4248 powers VCC from the higher voltage power source between V_{IN} and V_{OUT} to ensure that the VCC voltage is sufficiently high.

Enable (EN) Control

The MP4248 has an enable (EN) control pin. Pull EN high to enable the IC. Pull EN low or float EN to disable the IC (see Figure 6).

EN is a high-voltage pin that can be connected to VIN directly or through a resistor. A resistor divider can be connected to EN to set the V_{IN} on/off threshold.

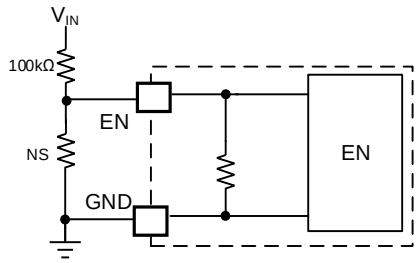


Figure 6: EN Connection

Under-Voltage Lockout (UVLO)

Under-voltage lockout (UVLO) protects the chip from operating at an insufficient supply voltage. The UVLO comparator monitors V_{IN} and V_{CC}. The MP4248 is enabled when V_{CC} exceeds its rising UVLO threshold. The MP4248 stops working if either V_{IN} or V_{CC} falls below its respective UVLO falling threshold.

The default V_{IN} UVLO rising threshold is 3.3V, and the falling threshold is 2.56V. This rising and falling thresholds can be trimmed via the one-time programmable (OTP) memory to 5.5V and 3.3V.

Internal Soft Start (SS)

Internal soft start (SS) prevents the converter's V_{OUT} from overshooting during start-up. When the chip starts up, the internal circuitry generates a soft-start voltage (V_{SS}) that ramps up from 0V to 5V. When V_{SS} is below V_{REF}, the error amplifier (EA) uses V_{SS} as the reference. When V_{SS} exceeds V_{REF}, the error amplifier uses V_{REF} as the reference.

If the output of the MP4248 is pre-biased to a certain voltage during start-up, the IC disables the switching of both the high-side and low-side

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2024 MPS. All Rights Reserved.

MOSFETs (HS-FETs and LS-FETs, respectively) until the voltage on the internal SS capacitor (C_{SS}) exceeds the internal V_{FB}.

CC Mode Over-Current-Protection (OCP)

The MP4248 senses the output current (I_{OUT}) via the ISEN+ and ISEN- pins. If I_{OUT} exceeds the set current-limit threshold, the MP4248 enters constant current (CC) limit mode. In this mode, the current amplitude is limited. As the load resistance is reduced, V_{OUT} drops until V_{FB} falls below the under-voltage (UV) threshold, which is about 40% below V_{REF}. Once the UV threshold is triggered and V_{OUT} falls below 2.93V, the MP4248 enters hiccup mode to periodically restart the part.

This protection mode is especially useful when the output is dead-shorted to ground. This greatly reduces the average short-circuit current, alleviates thermal issues, and protects the regulator. The MP4248 exits hiccup mode once the over-current (OC) condition is removed. The average I_{OUT} limit can be disabled by setting CC_DISABLE to 1.

The MP4248 supports high-side current-sensing for CC limit mode.

Switching Current Limit

The MP4248 senses the LS-FET current in the loop control. This allows the device to provide valley current limiting in buck mode, and peak current limiting in boost mode, during each cycle-by-cycle switching period. In buck mode, the next period does not start until I_L drops to the valley current limit, so the device may fold back the frequency when the valley current limit is triggered.

Based on the cycle-by-cycle switching current limit, the MP4248's maximum input current (I_{IN_MAX}) in buck mode can be calculated with Equation (1):

$$I_{IN_MAX}(A) = \frac{V_{OUT}}{V_{IN}} \times \eta \times (Valley_Current_Limit(A) + \frac{V_{IN} - V_{OUT}}{2 \times L(\mu H) \times f(kHz)} \times \frac{V_{OUT}}{V_{IN}} \times 10^3) \quad (1)$$

Where η is the efficiency.

The MP4248's I_{IN_MAX} in boost mode can be calculated with Equation (2):

$$I_{IN_MAX}(A) = Peak_Current_Limit(A) - \frac{V_{IN}}{2 \times L(\mu H) \times f(kHz)} \times \frac{V_{OUT} - V_{IN}}{V_{OUT}} \times 10^3 \quad (2)$$

The buck valley current limit is typically 13A. The boost peak current limit is typically 15A. The switching current limit can be configured via the I²C register (0xD3, bits D[7:6]).

Output Over-Voltage Protection (OVP)

The MP4248 has output over-voltage protection (OVP). If V_{OUT} exceeds 120% of V_{REF}, then SWA, SWB, SWC, and SWD turn off. The resistor discharge path from the VOUT pin to ground turns on. When V_{FB} drops to 110% of V_{REF}, the chip resumes normal operation.

The default absolute output OVP threshold is about 39V. The discharge resistor turns on when absolute OVP is triggered.

Set OUTPUT_OVP_EN = 0 to disable OVP and absolute OVP simultaneously.

The absolute output OVP threshold can be trimmed to 25.5V via the OTP.

Gate Driver and BST Power

The MP4248 provides two N-channel MOSFET gate drivers for the H-bridge MOSFETs. Each driver is capable of sourcing and sinking current. In buck mode, HG1 switches while HG2 stays on continuously. In boost mode, HG2 switches while HG1 stays on continuously. HG1 and HG2 are both powered by BST1 and BST2.

Capacitors between BST1-to-SW1 and BST2-to-SW2 are necessary to supply the power, which is powered by the internal diode from VCC. The capacitors can also charge each other.

The BST power has its own UVLO control. Its UVLO rising threshold is about 2.7V with a 200mV hysteresis voltage.

Switching Frequency (f_{SW}) and Frequency Spread Spectrum Function

The MP4248 configures the switching frequency (f_{SW}) via the MFR_CTRL1 (D0h) register. f_{SW} can be set to 280kHz, 420kHz, and 580kHz. Typically, a 420kHz f_{SW} is recommended.

The MP4248 has a frequency spread spectrum function. Set DITHER_ENABLE = 1 (0xD0, bit D[7]) to enable this function. Set DITHER_ENABLE = 0 to disable the function. The purpose of the spread spectrum is to minimize the peak emissions at certain frequencies.

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2024 MPS. All Rights Reserved.

The MP4248 uses a 2kHz triangle wave to modulate the internal oscillator. The frequency span for spread spectrum operation is ±8%.

Figure 7 shows frequency spread spectrum.

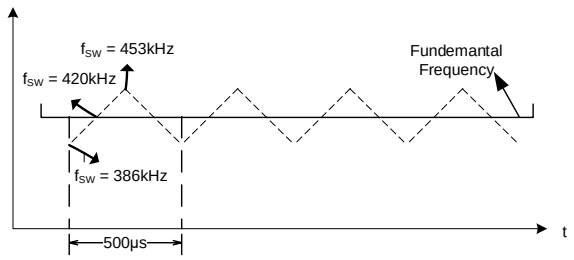


Figure 7: Frequency Spread Spectrum

The MP4248's spread frequency function can be enabled for all configurable f_{SW} values.

Start-Up and Shutdown

If both VIN and EN exceed their respective thresholds, the chip is enabled. The reference block starts first, generating a stable reference voltage and currents, and then the internal regulator is enabled. The regulator provides a stable supply for the remaining circuitries.

Several events can shut down the chip: EN going low, V_{IN} going low, and thermal shutdown. During shutdown, the signaling path is blocked to avoid any fault triggering. Then V_{COMP} and the internal supply rail are pulled down. The floating driver is not subject to this shutdown command.

Slew Rate Control and Output Discharge

The MP4248 can adjust the output voltage slew rate. The rising slew rate can be changed via the internal SR bits (0xD3, bits D[4:3]), and the falling slew rate can be changed via the SR bits (0xD3, bits D[2:1]). There are four potential V_{REF} changes (rising and falling), or slew rates, that can be selected for different application requirements.

If the output capacitance is too high, V_{OUT} may not discharge to the target voltage by the time that V_{REF} charging is complete. If this occurs, the OVP discharge function can continue discharging C_{OUT}.

The output discharge function is enabled if the following conditions are met:

1. The output OVP threshold (about 120% of V_{FB}) has been reached, or absolute OVP is triggered.
2. The I²C OPERATION command sends an off command, or the EN pin is off. Discharge works until a 200ms delay passes.
3. If V_{IN} UVLO is triggered but VCC has a residual voltage, the MP4248's V_{OUT} discharges for a limited time. This discharge function is disabled after the VCC voltage drops below 1.8V.

Output Line Drop Compensation

The MP4248 is capable of compensating for an output voltage drop, such as a high impedance caused by a long trace, to keep a fairly constant load-side voltage.

See the MFR_CTRL2 (D2h) section on page 32 for more details.

Current Monitor Output

The MP4248 senses the average load current through one sensing resistor, and the device outputs a voltage signal on the IMON pin. This signal is amplified by the voltage difference between ISEN+ and ISEN-. It is recommended to place a small capacitor from IMON to AGND.

In PFM mode, IMON can only work normally when the MP4248 operates in CCM.

SYSTEM

Thermal Shutdown (TSD)

Thermal shutdown prevents the chip from operating at exceedingly high temperatures. When the silicon die temperature exceeds 160°C, the entire chip shuts down. Once the temperature falls below the lower threshold (typically 140°C), the chip is enabled.

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2024 MPS. All Rights Reserved.

PMBUS INTERFACE

PMBus Serial Interface Description

The power management bus (PMBus) is an open-standard power management protocol that defines a means of communication with power conversion and other devices.

The PMBus is a two-wire, bidirectional serial interface, consisting of a data line (SDA) and a clock line (SCL). The lines are pulled to a bus voltage externally when they are idle. When connecting to the lines, a master device generates an SCL signal and device address, and arranges the communication sequence. This is based on I^2C operation principles.

Start and Stop Commands

The start and stop commands are signaled by the master device, which signifies the beginning and end of the PMBus transfer. A start (S) command is defined as the SDA signal transitioning from high to low while SCL is high. A stop (P) command is defined as the SDA signal transitioning from low to high while SCL is high (see Figure 8).

The master then generates the SCL clocks and transmits the device address and the read/write (R/W) direction bit on the SDA line. Data is transferred in 8-bit bytes by the SDA line. Each byte of data is followed by an acknowledge (ACK) bit.

PMBus Update Sequence

The MP4248 requires a start command, a valid PMBus address, a register address byte, and a data byte for a single data update. The device acknowledges that it has received each byte by pulling the SDA line low during the high period of a single clock pulse. A valid PMBus address selects the MP4248. The device performs an update on the falling edge of the least significant bit (LSB) byte.

PMBus Bus Message Format

Figure 9 on page 26 shows the PMBus message format. Unshaded cells indicate that the bus host is actively driving the bus, while shaded cells indicate that the MP4248 is driving the bus.

- S = Start command
- Sr = Repeated start command
- P = Stop command
- R = Read bit
- $\overline{W}$ = Write bit
- A = Acknowledge bit (0)
- $\overline{A}$ = Acknowledge bit (1)

“A” represents the acknowledge (ACK) bit. The ACK bit is typically active low (logic 0) if the transmitted byte is successfully received by a device.

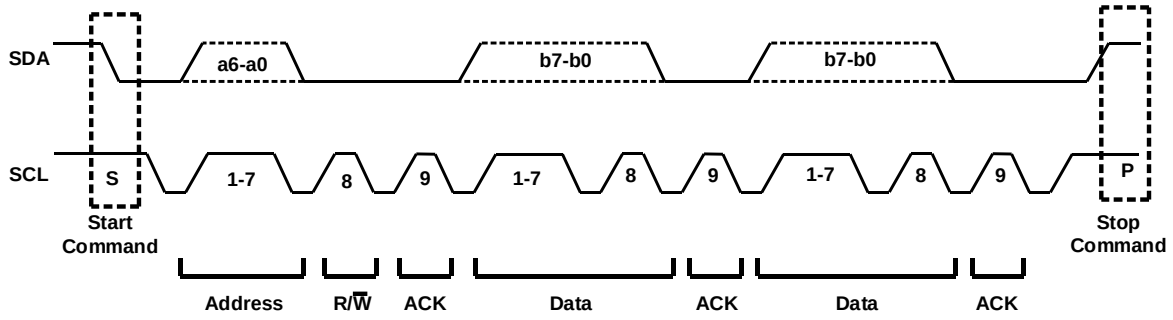


Figure 8: Data Transfer over the PMBus

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2024 MPS. All Rights Reserved.

a) Send Byte

1	7	1	1	8	1	1
S	Slave Address	Wr	A	Command Code	A	P

b) Write Byte

1	7	1	1	8	1	8	1	1
S	Slave Address	Wr	A	Command Code	A	Data Byte	A	P

c) Write Word

1	7	1	1	8	1	8	1	8	1	1
S	Slave Address	Wr	A	Command Code	A	Data Byte Low	A	Data Byte High	A	P

d) Read Byte

1	7	1	1	8	1	1	7	1	1	8	1	1
S	Slave Address	Wr	A	Command Code	A	S	Slave Address	Rd	A	Data Byte	$\overline{A}$	P

e) Read Word

1	7	1	1	8	1	1	7	1	1	8	1
S	Slave Address	Wr	A	Command Code	A	S	Slave Address	Rd	A	Data Byte Low	A

8	1	1
Data Byte High	$\overline{A}$	P

Figure 9: PMBus Message Format

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2024 MPS. All Rights Reserved.

REGISTER DESCRIPTION

I²C/PMBus Register

The I²C is active once V_{IN} and EN both exceeds their UVLO threshold [9].

Command Code	Command Name	Type	Bytes	Data Format	Unit	OTP?	Default Value
0x01	OPERATION	R/W	1	Reg	-	Yes	On
0x03	CLEAR_FAULTS	Send Byte	1	Reg	-	No	-
0x21	VOUT_COMMAND	R/W	2	Linear L16	V	Yes	V_{REF} = 0.5V
0x79	STATUS_WORD	R	2	Reg	-	No	-
0x7D	STATUS_TEMPERATURE	R	1	Reg	-	No	-
0xD0	MFR_CTRL1	R/W	1	Reg	-	Yes	-
0xD1	MFR_CURRENT_LIMIT	R/W	1	Reg	-	Yes	5.4A
0xD2	MFR_CTRL2	R/W	1	Reg	-	Yes	-
0xD3	MFR_CTRL3	R/W	1	Reg	-	Yes	-
0xD4	MFR_CTRL4	R/W	1	Reg	-	Yes	-
0xD8	MFR_STATUS_MASK	R/W	1	Reg	-	Yes	-
0xD9	MFR_OTP_ CONFIGURATION_CODE	R/W	1	Reg	-	Yes	-
0xDA	MFR_OTP_REVISION_ NUMBER	R/W	1	Reg	-	Yes	-

Note:

9) All register values are based on the MP4248-0000.

Data Format

The Linear16 format is used for the V_{OUT} command. Figure 10 shows how to read V_{OUT}.

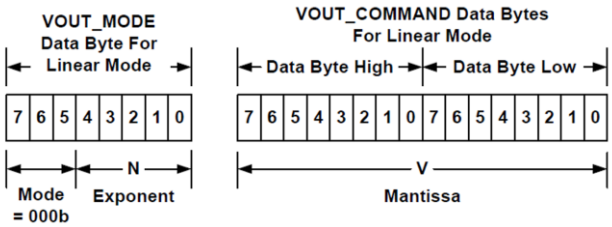


Figure 10: Reading V_{OUT}

The mode bits are set to 000b. The voltage (in V) can be calculated with Equation (3):

$$\text{Voltage} = V \times 2^{N} \quad (3)$$

Where Voltage is the parameter of interest (in V), *V* is a 16-bit unsigned binary integer, and *N* is a 5-bit, two's complement, binary integer.

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2024 MPS. All Rights Reserved.

PMBUS COMMAND INTRODUCTION

OPERATION (01h)

Format: Unsigned binary

The OPERATION command configures the converter's operational state.

Bits	Access	Bit Name	Description
7:0	R/W	OPERATION	Puts the converter in the on/off state. The EN pin has a higher control priority than this bit. 8'b 0000 0000: The output is off 8'b 1000 0000: The output is on (default)

CLEAR_FAULTS

The CLEAR_FAULTS command clears any fault bits that have been set. This command clears all bits in all status registers simultaneously. At the same time, the device negates (clears, releases) its ALT# signal output if the device asserts the ALT# signal.

The CLEAR_FAULTS command does not cause a device that has latched off for a fault condition to restart.

If the fault is still present when the bit is cleared, the fault bit shall immediately be set again and the host is notified by the usual means. This command is write-only**.** See Figure 9 on page 26 for more details.

VOUT_COMMAND (21h)

Format: Linear

The VOUT_COMMAND command sets V_{OUT}. It follows the Linear16 linear data format.

Command	VOUT_COMMAND															
Format	Linear															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	Data Byte High								Data Byte Low							
Reference Voltage (0.5V)	5120 Decimal / 1400 Hexadecimal															

V_{OUT} (in V) can be estimated with Equation (4):

$$V_{OUT} = V \times 2^{-10} \times FB_RATIO / 10 \quad (4)$$

Where *V* is the decimal number corresponding to the 16-bit unsigned binary integer of VOUT_COMMAND, bits[15:0]. FB_RATIO is the feedback resistor ratio and is equal to ((R1 + R2) / R2). See Figure 10 on page 27 for more details.

The recommended feedback resistor ratio should be V_{OUT} / V_{FB} = 10. The default V_{OUT} should be 0.5V x 10 = 5V. See Figure 11 on page 29 for more details.

If V_{OUT} = 28V, the recommended feedback resistor ratio should be V_{OUT} / V_{FB} = 15. Table 1 shows V_{OUT} when FB_RATIO = 10.

Table 1: VOUT_COMMAND Setting Table (FB_RATIO = 10)

V_{OUT}	V_{REF}	VOUT_COMMAND
5V	0.5V	1400h
9V	0.9V	2400h
15V	1.5V	3C00h
20V	2V	5000h

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2024 MPS. All Rights Reserved.

Figure 11 shows the feedback network.

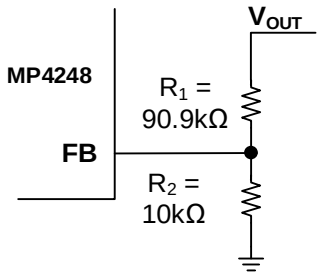


Figure 11: Feedback Network

Table 2 shows V_{OUT} when FB_RATIO = 15.

Table 2: VOUT_COMMAND Setting Table (FB_RATIO = 15)

V_{OUT}	V_{REF}	VOUT_COMMAND
5V	0.333V	D56h
9V	0.6V	1800h
15V	1V	2800h
20V	1.333V	3556h
28V	1.8667V	4AABh

Figure 12 shows the feedback network.

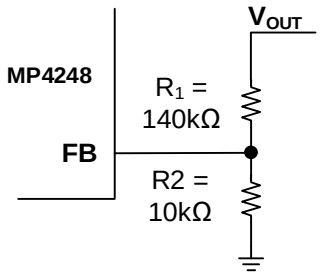


Figure 12: Feedback Network

The internal reference voltage ranges between 0.1V and 2.147V with 1mV steps(total 2047 steps, 11 bit DAC, when DAC input is 11 bit “0”, DAC output is 0.1V).

When the feedback resistor ratio is V_{OUT} / V_{FB} = 10, the VOUT_COMMAND resolution is 10mV. The valid V_{OUT} range is between 1V and 21.47V. V_{OUT} is abnormal when it is beyond this range.

When the MP4248 is used for 28V/5A EPR mode, the recommended feedback resistor ratio is V_{OUT} / V_{FB} = 15. The VOUT_COMMAND resolution is 15mV. The valid V_{OUT} range is between 1V and 32.205V. V_{OUT} is abnormal when it is beyond this range.

If the calculated VOUT_COMMAND is not an integer, set VOUT_COMMAND equal to the integer part plus 1.

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2024 MPS. All Rights Reserved.

STATUS_WORD (79h)

Format: Unsigned binary

The STATUS_WORD command returns 2 bytes of information with a summary of the device's fault conditions. Based on the information in these bytes, the host can obtain more information by reading the appropriate status registers. The PG_STATUS# bit always reflects the current state of the POWER_GOOD signal (if present). It is the only bit that does not remain set.

Byte	Bits	Access	Bit Name	Description
Low	7	R	RESERVED	Reserved. The default value is 0b.
	6	R	RESERVED	Reserved. The default value is 0b.
	5	R	VOUT_OV_FAULT	Indicates whether an output over-voltage (OV) fault has occurred.
	4	R	IOUT_OC_FAULT	Indicates whether an output over-current (OC) fault has occurred. This bit is set if the CC current limit or peak current limit is reached, or if the device enters hiccup mode.
	3	R	RESERVED	Reserved. The default value is 0b.
	2	R	TEMPERATURE	Indicates whether a temperature fault has occurred.
	1	R	RESERVED	Reserved. The default value is 0b.
	0	R	RESERVED	Reserved. The default value is 0b.
High	7	R	VOUT	An output voltage fault or warning has occurred.
	6	R	IOUT/POUT	An I_{OUT} fault has occurred. This bit is set if the CC current limit or peak current limit is reached, or if the device enters hiccup mode.
	5	R	RESERVED	Reserved. The default value is 0b.
	4	R	OC_EXIT	Indicates whether I_{OUT} exits the CC current limit. This bit is only set high when I_{OUT} changes from CC (before enter hiccup) to non-CC mode. This bit is not set when the device recovers from hiccup mode.
	3	R	PG_STATUS#	The POWER_GOOD signal, if present, is negated. When this bit is set 1, the output voltage is not good. When this bit is clear, the output voltage is power good.
	2	R	RESERVED	Reserved. The default value is 0b.
	1	R	RESERVED	Reserved. The default value is 0b.
	0	R	RESERVED	Reserved. The default value is 0b.

STATUS_TEMPERATURE (7Dh)

Format: Unsigned binary

The STATUS_TEMPERATURE command returns 1 data byte with information on the device.

Bits	Bit Name	Access	Description
7	OT_FAULT	R	Indicates whether an over-temperature (OT) fault has occurred. The OTP entry threshold is 160°C.
6	OT_WARNING	R	Indicates whether an OT warning has occurred. The entry threshold is 135°C. It has a 20°C hysteresis.
5	RESERVED	R	Reserved.
4	RESERVED	R	Reserved.
3	OT_WARNING_EXIT	R	The OT_WARNING falling edge sets this bit high.
2	RESERVED	R	Reserved.
1	RESERVED	R	Reserved.
0	RESERVED	R	

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2024 MPS. All Rights Reserved.

I²C REGISTER MAP

Name	REG (0x)	R/W	D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]
MFR_CTRL1	D0	R/W	DITHER_ ENABLE	FREQ		SWA_FET_ _RON		OUTPUT_ OVP_EN	OUTPUT_ DISCHAR GE_EN	PFM/ PWM_ MODE
MFR_CURRENT_ LIMIT	D1	R/W	LDC_ DISABLE	CONSTANT_CURRENT_LIMIT (0.5A to 5.4A/50mA step)						
MFR_CTRL2	D2	R/W	RESERVED						LINE_DROP_ COMPENSATION	
MFR_CTRL3	D3	R/W	SWITCHING_ CURRENT_LIMIT		RSENS	SLEW_RATE _RISE		SLEW_RATE_FALL		FREQ_ MODE
MFR_CTRL4	D4	R/W	CC_BLANK_TIMER		CC_ DISABLE	I2C_ADDRESS (A5:A1)				
MFR_STATUS_MASK	D8	R/W	Masks the ALT# pin indication if any fault or fault event occurs							
MFR_OTP_ CONFIGURATION_ CODE	D9	R/W	OTP_CONFIGURATION_CODE (defined by MPS)							
MFR_OTP_ REVISION_NUMBER	DA	R/W	OTP_REVISION_NUMBER (defined by MPS)							

I²C Slave Address

The I²C slave address is 67h by default.

I²C Address A7:A1	
Binary	**Hex**
1100 111 (Default)	67h
I²C/OTP adjustable for A5:A1	Set by MFR_CTRL4, bits D[4:0]

MFR_CTRL1 (D0h)

Format: Unsigned binary

Reset value: Set via the OTP

The MFR_CTRL1 command configures certain functions.

Bits	Access	Bit Name	Default	Description
D[7]	R/W	DITHER_ENABLE	1'b 0	1'b 0: No dither 1'b 1: Enable the frequency spread spectrum function
D[6:5]	R/W	FREQ	2'b 01	Sets the switching frequency (f_{SW}). 2'b 00: 280kHz 2'b 01: 420kHz 2'b 10: 580kHz 2'b 11: Reserved
D[4:3]	R/W	SWA_FET_RON	2'b 01	Sets the external SWA's on resistance ($R_{DS(ON)}$) under $5V_{GS}$. This value is used for zero-current detection (ZCD). The selected value must match SWA's actual $R_{DS(ON)}$. 2'b 00: 5mΩ 2'b 01: 10mΩ 2'b 10: 15mΩ 2'b 11: 20mΩ
D[2]	R/W	OUTPUT_OVP_EN	1'b 1	Enables output over-voltage protection (OVP). 1'b 0: No output OVP 1'b 1: Enabled

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2024 MPS. All Rights Reserved.

D[1]	R/W	OUTPUT_ DISCHARGE_EN	1'b 1	Enables the output discharge function. For output discharge, a passive discharge resistor connected from VOUT to ground turns on. Discharge works until the maximum 200ms timer ends. 0: Disables the output discharge function during an EN, V_{IN}, or I^2C shutdown 1: The MP4248 turns on the output discharge function during an EN, V_{IN}, or I^2C shutdown until V_{OUT} is fully discharged
D[0]	R/W	PFM/PWM_MODE	1'b 1	Sets the buck-boost work mode. 1'b 0: Auto-PFM/PWM mode 1'b 1: Forced PWM mode

MFR_CURRENT_LIMIT (D1h)

Format: Linear

Reset value: Set via the OTP

The MFR_CURRENT_LIMIT command sets the constant current limit.

Name	LDC_DISABLE	CONSTANT_CURRENT_LIMIT						
Format	Direct, Unsigned Binary Integer							
Bit	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default Value (5.4A)	0	108 Integer						

The real-world IOUT_OC (in A) can be calculated with Equation (5):

$$IOUT_OC\ (A) = IOUT_LIM \times 0.05 \quad (5)$$

Where IOUT_LIM is a 7-bit unsigned binary integer of IOUT_LIM, bits D[6:0]. The IOUT_OC resolution or minimum step is 50mA. The maximum value is 5.4A. Beyond this range, the current limit is clamped at 5.4A.

Bits	Access	Bit Name	Default	Description
D[7]	R/W	LDC_DISABLE	1'b 0	Enables the line drop compensation. 1'b 0: Line drop compensation is controlled by MFR_CTRL2 (D2h) 1'b 1: Line drop compensation is disabled
D[6:0]	R/W	CONSTANT_ CURRENT_LIMIT	6'b 1101100	Sets the output constant current limit.

MFR_CTRL2 (D2h)

Format: Unsigned binary

The MFR_CTRL2 command sets the line drop compensation value.

Bits	Access	Bit Name	Default	Description
D[7:2]	-	RESERVED	-	Reserved.
D[1:0]	R/W	LINE_DROP_ COMPENSATION	2'b 00	Sets the V_{OUT} compensation value at certain load currents. The compensation amplitude is fixed for any V_{OUT}. 2'b 00: No compensation 2'b 01: V_{OUT} compensates 100mV at a 3A I_{OUT} 2'b 10: V_{OUT} compensates 300mV at a 3A I_{OUT} 2'b 11: V_{OUT} compensates 600mV at a 3A I_{OUT}

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2024 MPS. All Rights Reserved.

MFR_CTRL3 (D3h)

Format: Unsigned binary

Reset value: Set via the OTP

The MFR_CTRL3 command configures certain functions.

Bits	Access	Bit Name	Default	Description
D[7:6]	R/W	SWITCHING_ CURRENT_LIMIT	2'b 01	Sets the current limit for SWB and SWC. 2'b 00: 8A SWC peak current limit / 6A SWB valley current limit 2'b 01: 12A SWC peak current limit / 9A SWB valley current limit 2'b 10: 15A SWC peak current limit / 13A SWB valley current limit 2'b 11: 20A SWC peak current limit / 17A SWB valley current limit
D[5]	R/W	RSENS	1'b 0	Selects R_{SENS}. 1'b 0: 5mΩ 1'b 1: 10mΩ
D[4:3]	R/W	SLEW_RATE_RISE	2'b 01	Sets the V_{OUT} rising slew rate, which can be calculated with the following equation: V_{OUT} Slew Rate = V_{REF} Slew Rate x Feedback_Ratio Where Feedback_Ratio = 10. 2'b 00: 0.08mv/µs V_{REF} rising slew rate 2'b 01: 0.16mv/µs V_{REF} rising slew rate 2'b 10: 0.4mv/µs V_{REF} rising slew rate 2'b 11: 0.8mv/µs V_{REF} rising slew rate
D[2:1]	R/W	SLEW_RATE_FALL	2'b 01	Sets the V_{OUT} falling slew rate, which can be calculated with the following equation: V_{OUT} Slew Rate = V_{REF} Slew Rate x Feedback_Ratio Where Feedback_Ratio = 10. 2'b 00: 0.02mv/µs V_{REF} falling slew rate 2'b 01: 0.04mv/µs V_{REF} falling slew rate 2'b 10: 0.1mv/µs V_{REF} falling slew rate 2'b 11: 0.2mv/µs V_{REF} falling slew rate
D[0]	R/W	FREQ_MODE	1'b 0	Sets the frequency mode under buck-boost mode. 1'b 0: Reduce the frequency to half of that in buck or boost mode 1'b 1: Keep the same frequency as that in buck or boost mode

MFR_CTRL4 (D4h)

Format: Unsigned binary

Reset value: Set by OTP

The MFR_CTRL4 command configures certain functions.

Bits	Access	Bit Name	Default	Description
D[7:6]	R/W	CC_BLANK_TIMER	2'b 00	Sets the blanking time before entering CC mode: 2'b 00: 250µs 2'b 01: 3ms 2'b 10: 14.5ms 2'b 11: Reserved

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2024 MPS. All Rights Reserved.

D[5]	R/W	CC_DISABLE	1'b 0	Enables the CC current limit. 1'b 0: Enabled 1'b 1: Disabled
D[4:0]	R/W	I2C_ADDRESS	5'b 00111	Sets the I²C slave address's A5:A1 bits. The default value is 00111b, which is a slave address of 67h.

MFR_STATUS_MASK (D8h)

Format: Unsigned binary

Reset value: Set via the OTP

The MFR_STATUS_MASK command can only mask off the ALT# pin's behavior; the STATUS register still indicates each event.

Bits	Access	Bit Name	Default	Description
D[7]	R/W	VOUT_MSK	1'b 1	1'b 0: No mask 1'b 1: Mask enabled
D[6]	R/W	IOUT/POUT_MSK	1'b 0	1'b 0: No mask. This bit masks IOUT_OC_FAULT, IOUT/POUT, and OC_EXIT 1'b 1: Mask enabled
D[5]	R/W	RESERVED_MSK	1'b 1	1'b 0: No mask 1'b 1: Mask enabled
D[4]	R/W	TEMP_MSK	1'b 1	Masks the temperature-related fault. 1'b 0: No mask 1'b 1: Mask enabled
D[3]	R/W	PG_STATUS#_MSK	1'b 1	Masks the higher-level PG control bit. 1'b 0: No mask 1'b 1: Mask enabled
D[2]	R/W	RESERVED		Reserved.
D[1]	R/W	RESERVED_MSK	1'b 1	1'b 0: No mask 1'b 1: Mask enabled
D[0]	R/W	UNKNOWN_MSK	1'b 1	1'b 0: No mask 1'b 1: Mask enabled

MFR_OTP_CONFIGURATION_CODE (D9h)

Format: Unsigned binary

Reset value: Set via the OTP

The MFR_OTP_CONFIGURATION_CODE command sets the OTP configuration code, which is defined by MPS.

Bits	Access	Bit Name	Description
D[7:0]	R/W	OTP_ CONFIGURATION_ CODE	Sets the OTP configuration code, defined by MPS.

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2024 MPS. All Rights Reserved.

MFR_OTP_REVISION_NUMBER (DAh)

Format: Unsigned binary

Reset value: Set via the OTP

The MFR_OTP_REVISION_NUMBER command sets the OTP software revision number, defined by MPS.

Bits	Access	Bit Name	Description
D[7:0]	R/W	OTP_REVISION_ NUMBER	Sets the OTP software revision number, defined by MPS.

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2024 MPS. All Rights Reserved.

APPLICATION INFORMATION

COMPONENT SELECTION

Selecting the Inductor

MPL Optimized Performance with MPS Inductor MPL-AY1265 Series

Inductor selection should be based on the operation mode. The inductance for buck mode (L_{BUCK}) can be estimated with Equation (6):

$$L_{BUCK} = \frac{V_{OUT}}{f_{SW} \times \Delta I_L} \times (1 - \frac{V_{OUT}}{V_{IN}}) \quad (6)$$

Where ΔI_L is the peak-to-peak inductor ripple current, which is 30% to 50% of the maximum load current.

For boost mode, the inductor should limit the peak-to-peak current ripple (ΔI_L) to be between 30% and 50% of the maximum input current. The inductance for boost mode (L_{BOOST}) can be calculated with Equation (7):

$$L_{BOOST} = \frac{V_{IN} \times (V_{OUT} - V_{IN})}{V_{OUT} \times f_{SW} \times \Delta I_L} \quad (7)$$

Where $I_{LOAD(MAX)}$ is the maximum load current, and ΔI_L is the peak-to-peak ripple current (about 30% to 50% of the maximum input current).

$I_{IN(MAX)}$ can be estimated with Equation (8):

$$I_{IN(MAX)} = \frac{V_{OUT} \times I_{LOAD(MAX)})}{V_{IN} \times \eta} \quad (8)$$

Where η is the efficiency.

Choosing a larger-value inductor reduces the ripple current, but also increases the size of the inductor and reduces the converter's achievable bandwidth by moving the right half-plane zero to lower frequencies. Choose an inductor that meets the application requirements.

MPS inductors are optimized and tested for use with our complete line of integrated circuits.

Table 3 lists our power inductor recommendations. Select a part number based on your design requirements.

Table 3: Power Inductor Selection

Part Number	Inductance	Manufacturer
MPL-AY1265-4R7	4.7µH	MPS
MPL-AY1265-6R8	6.8µH	MPS
MPL-AY1265-100	100µH	MPS

Visit MonolithicPower.com under Products > Inductors for more information.

Selecting the Input Capacitor

In buck mode, the input current is discontinuous, while it is continuous in boost mode. A capacitor must supply the AC current in buck mode while maintaining the DC input voltage. Ceramic capacitors are recommended for the best performance, and these capacitors should be placed as close to the VIN pin as possible. Ceramic capacitors with X5R or X7R dielectrics are recommended because they are fairly stable amid temperature fluctuations. The capacitors must have a ripple current rating greater than the converter's maximum input ripple current. The input ripple current in buck mode (I_{CIN}) can be estimated with Equation (9):

$$I_{CIN} = I_{OUT} \times \sqrt{\frac{V_{OUT}}{V_{IN}} \times (1 - \frac{V_{OUT}}{V_{IN}})} \quad (9)$$

The worst-case condition in buck mode occurs at V_{IN} = 2 x V_{OUT}, calculated with Equation (10):

$$I_{CIN} = \frac{I_{OUT}}{2} \quad (10)$$

For simplification, choose an input capacitor with an RMS current rating greater than half of the maximum load current.

The input capacitance determines the converter's input voltage ripple. If there is an input voltage ripple requirement in the system, choose the input capacitor that meets the specification.

The input voltage ripple (ΔV_{IN}) in buck mode can be estimated with Equation (11):

$$\Delta V_{IN} = \frac{I_{OUT}}{f_{SW} \times C_{IN}} \times \frac{V_{OUT}}{V_{IN}} \times (1 - \frac{V_{OUT}}{V_{IN}}) \quad (11)$$

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2024 MPS. All Rights Reserved.

The worst-case condition occurs at $V_{IN} = 2 \times V_{OUT}$, calculated with Equation (12):

$$\Delta V_{IN} = \frac{1}{4} \frac{I_{OUT}}{f_{SW} \times C_{IN}} \quad (12)$$

The input voltage ripple in boost mode can be estimated with Equation (13):

$$\Delta V_{IN} = \frac{V_{IN}}{8 \times f_{SW}^2 \times L \times C_{IN}} \times (1 - \frac{V_{IN}}{V_{OUT}}) \quad (13)$$

If using polymer, hybrid, or low-ESR electrolytic capacitors, the ESR dominates the impedance at the switching frequency. The input voltage ripple in boost mode can be calculated with Equation (14):

$$\Delta V_{IN} = \frac{V_{IN}}{f_{SW} \times L} \times \left(1 - \frac{V_{IN}}{V_{OUT}}\right) \times \left(R_{ESR} + \frac{1}{8 \times f_{SW} \times C_{IN}}\right) \quad (14)$$

Selecting the Output Capacitor

I_{OUT} is discontinuous in boost mode, so the output capacitor (C_{OUT}) must be able to reduce the output voltage ripple.

A larger-value capacitor may be required to lower the output voltage ripple and transient response. Ceramic, low-ESR capacitors with X5R or X7R dielectrics are recommended. If using ceramic capacitors, the capacitance dominates the impedance at the switching frequency, so the output voltage ripple is independent of the ESR. The output voltage ripple in buck mode can be estimated with Equation (15):

$$\Delta V_{OUT} = \frac{V_{OUT}}{8 \times f_{SW}^2 \times L \times C_{OUT}} \times (1 - \frac{V_{OUT}}{V_{IN}}) \quad (15)$$

Where ΔV_{OUT} is the output ripple voltage, and C_{OUT} is the capacitance of the output capacitor.

If using polymer, hybrid, or low-ESR electrolytic capacitors, the ESR dominates the impedance at the switching frequency. The output voltage ripple in buck mode can be calculated with Equation (16):

$$\Delta V_{OUT} = \frac{V_{OUT}}{f_{SW} \times L} \times (1 - \frac{V_{OUT}}{V_{IN}}) \times (R_{ESR} + \frac{1}{8 \times f_{SW} \times C_{OUT}}) \quad (16)$$

Where R_{ESR} is the output capacitor's ESR.

The output voltage ripple in boost mode can be estimated with Equation (17):

$$\Delta V_{OUT} = \frac{(1 - \frac{V_{IN}}{V_{OUT}}) \times I_{OUT}}{C_{OUT} \times f_{SW}} \quad (17)$$

If using polymer, hybrid, or low-ESR electrolytic capacitors, the ESR dominates the impedance at the switching frequency. The output voltage ripple in boost mode can be calculated with Equation (18):

$$\Delta V_{OUT} = \frac{(1 - \frac{V_{IN}}{V_{OUT}}) \times I_{OUT}}{C_{OUT} \times f_{SW}} + \frac{I_{OUT} \times R_{ESR} \times V_{OUT}}{V_{IN}} \quad (18)$$

Choose output capacitors that satisfy the design's output voltage ripple and load transient response requirements. Consider capacitance derating when designing applications with high output voltages.

External MOSFET Selection for SWA and SWD

The MP4248 requires two external N-channel power MOSFETs. In buck mode, SWA and SWB switch while SWD stays continuously on. In boost mode, SWC and SWD switch while SWA stays continuously on (see Figure 13).

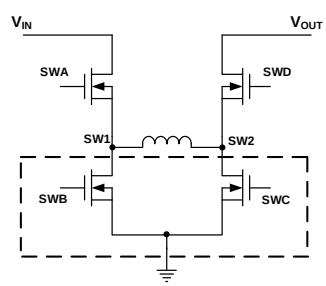


Figure 13: Buck-Boost Topology

The critical parameters when selecting a MOSFET are listed below:

1. Maximum drain-to-source voltage ($V_{DS(MAX)}$): SWA must be able to withstand the maximum V_{IN}. Additionally, SWA must withstand the transient spikes at SW1 during switching. Select SWA and SWB to have a $V_{DS(MAX)}$ that is 1.5 times V_{IN}.

   SWD must be able to handle V_{OUT} and additional transient spikes at SW2 during switching. Select SWD to have a $V_{DS(MAX)}$ that is at least 1.5 times V_{OUT}.

2. The maximum current ($I_{D(MAX)}$).

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2024 MPS. All Rights Reserved.

3. V_{TH}: The MP4248's driver voltages are supplied by VCC, so the gate plateau voltages of the MOSFETs should be below the minimum V_{CC}. Otherwise the MOSFETs may not fully turn on during start-up or under overload conditions.
4. The on resistance ($R_{DS(ON)}$).
5. Total gate charge (Q_G): For the MP4248, all switches' Q_G should be below 30nC (at a 5V GATE condition). The SW1 rising time and SW2 falling time are smaller than 15ns.

SWA

When the MP4248 works in boost mode, SWA is always on. Calculate SWA's conduction power loss ($P_{C_LOSS(SWA)}$) with Equation (19):

$$P_{C_LOSS(SWA)} = (I_{OUT} \times \frac{V_{OUT}}{V_{IN}})^2 \times R_{DSON(SWA)} \quad (19)$$

Assume that the MOSFET's thermal resistance from the junction to ambient is 50°C/W (as determined by the board power dissipation), and the maximum acceptant temperature rise is 50°C, thus. This means that the maximum power loss is 1W, as estimated with Equation (20):

$$P_{C_LOSS(SWA)} < 1W \quad (20)$$

Based on above calculate equation, users can select the MOSFET's on resistance.

When the MP4248 works in buck mode, the conduction loss ($P_{C_LOSS(SWA)}$) and switching loss ($P_{SW_LOSS(SWA)}$) on SWA can be calculated with Equation (21) and Equation (22), respectively:

$$P_{C_LOSS(SWA)} = \frac{V_{OUT}}{V_{IN}} \times I_{OUT}^2 \times R_{DSON(SWA)} \quad (21)$$

$$P_{SW_LOSS(SWA)} = \frac{1}{2} V_{IN} \times I_{OUT} \times (t_{ON} + t_{OFF}) \times f_{sw} \quad (22)$$

Figure 14 shows the switching on/off state.

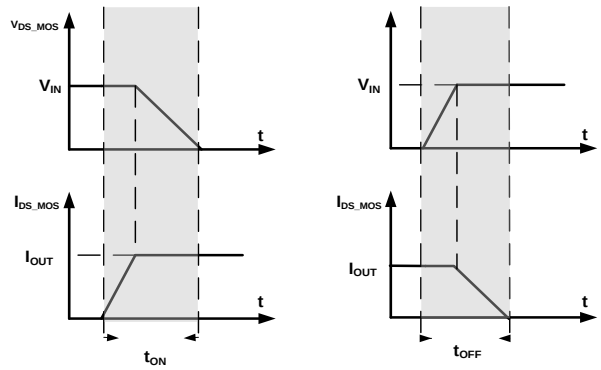


Figure 14: Switch On/Off State

The switching on time (t_{ON}) and the switching off time (t_{OFF}) are based on the MOSFET datasheet's information.

SWD

When the MP4248 works in buck mode, SWD is always on, and its power loss ($P_{C_LOSS(SWD)}$) can be calculated with Equation (23):

$$P_{C_LOSS(SWD)} = I_{OUT}^2 \times R_{DSON(SWD)} \quad (23)$$

Similar to $P_{C_LOSS(SWA)}$, $P_{C_LOSS(SWD)}$ should also be below the maximum power loss.

When the MP4248 works in boost mode, the conduction power loss ($P_{C_LOSS(SWD)}$) can be estimated with Equation (24):

$$P_{C_LOSS(SWD)} = \frac{V_{OUT}}{V_{IN}} \times I_{OUT}^2 \times R_{DS_ON(SWD)} \quad (24)$$

The dead time and LS-FET switching loss can be ignored.

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2024 MPS. All Rights Reserved.

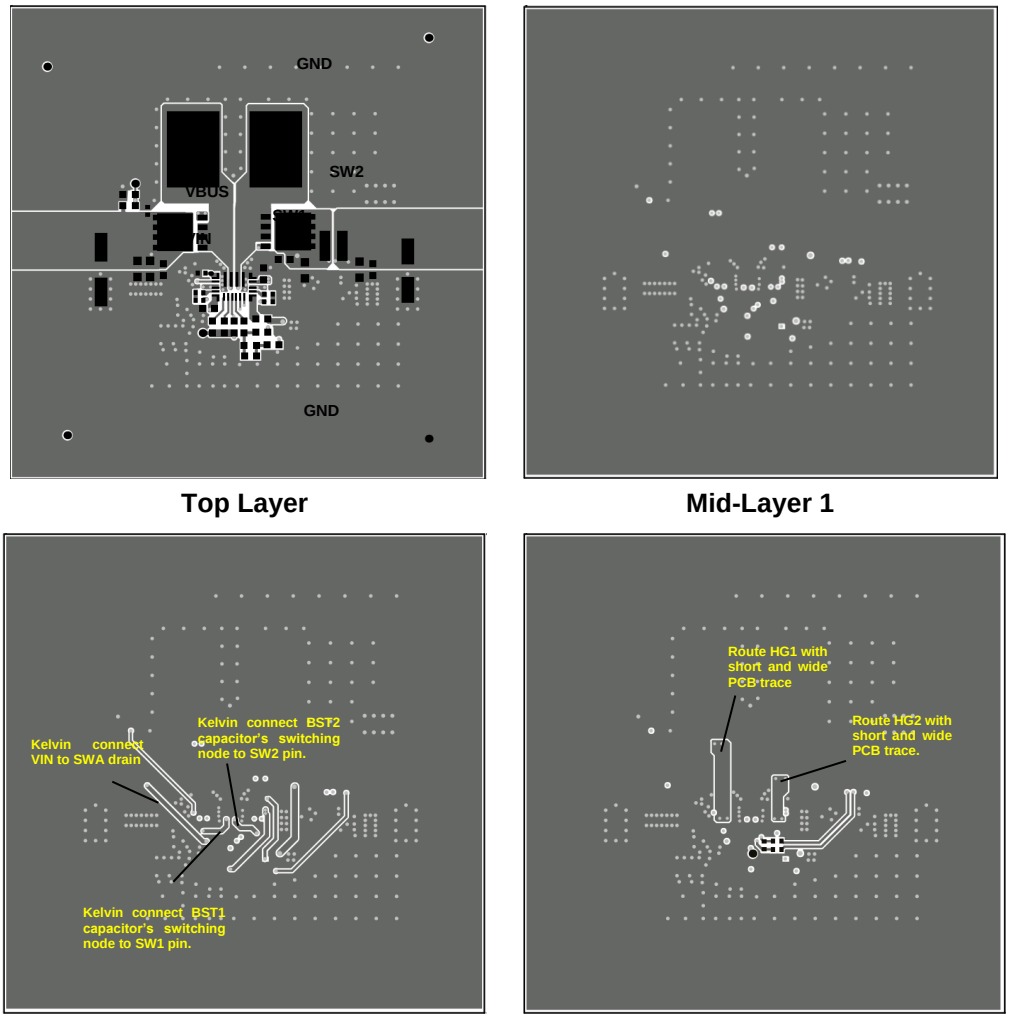
PCB Layout Guidelines [10]

Efficient PCB layout is critical for standard operation and thermal dissipation. For the best results, refer to Figure 15 and follow the guidelines below:

1. In buck mode, place the input power loop — including the input filter capacitor (C_{IN}), the power MOSFET SWA and SW1 node — as close together as possible.
2. In boost mode, place the output power loop — including the output filter capacitor (C_{OUT}), the power MOSFET SWD, and SW2 node — as close together as possible.
3. Use short, direct, and wide traces to connect VOUT.
4. Add vias to GND after the output filter if needed.
5. Use a large copper plane for PGND and add multiple vias to improve thermal dissipation.
6. Connect AGND to PGND.
7. To improve EMI performance, place two ceramic input decoupling capacitors as close as possible to VIN, VOUT, and PGND.
8. Place the VCC decoupling capacitor as close as possible to VCC.
9. The output current-sense traces (ISEN+, ISEN-) must use a Kelvin connection.

Note:

10) The recommended layout is based on Figure 16 on page 40.



Top Layer **Mid-Layer 1**

Mid-Layer 2 **Bottom Layer**

Figure 15: Recommended PCB Layout

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2024 MPS. All Rights Reserved.

TYPICAL APPLICATION CIRCUITS

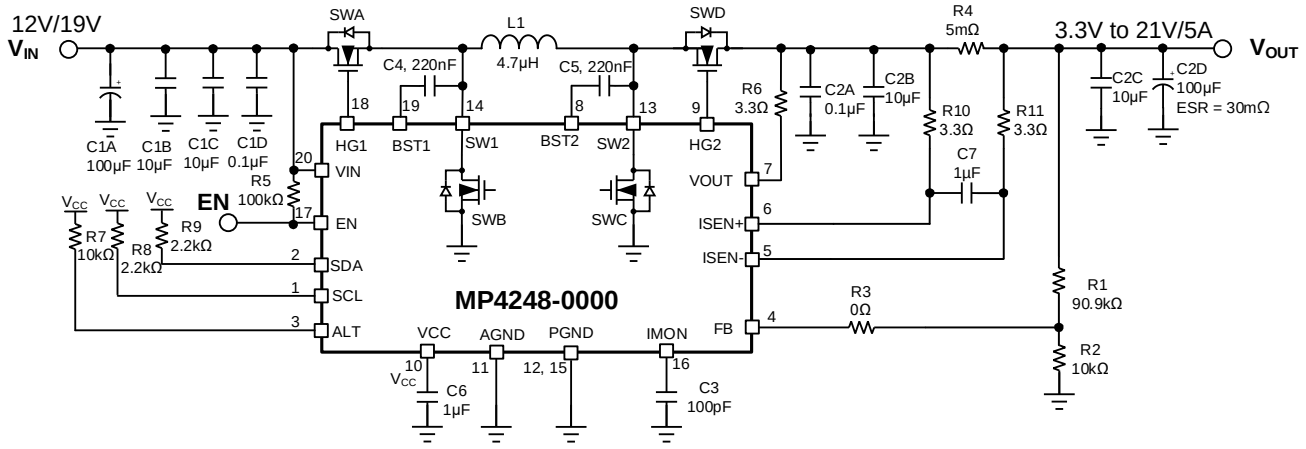


Figure 16: Typical Application Circuit (V_{IN} = 12V/19V, V_{OUT} = 3.3V to 21V/5A, Default On)

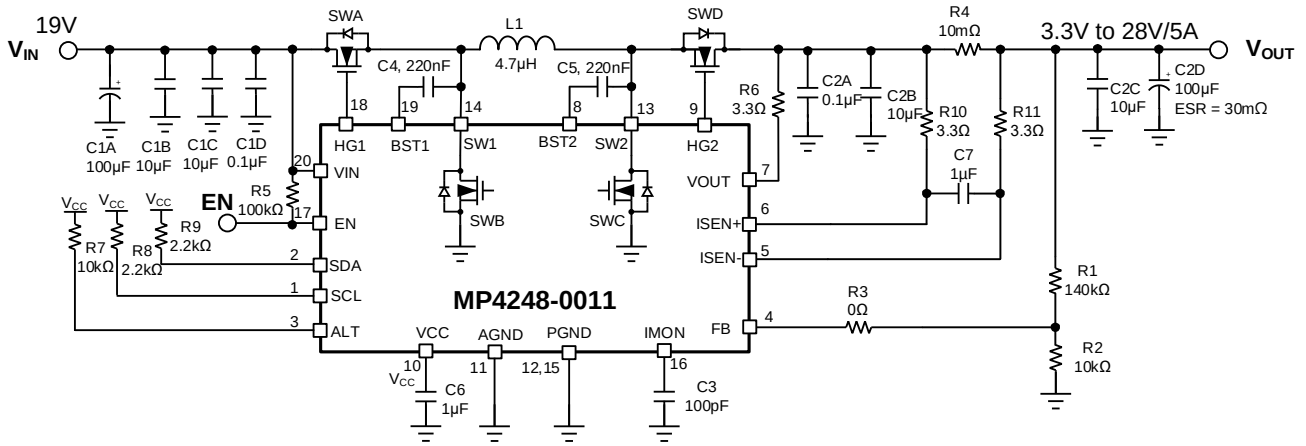


Figure 17: Typical Application Circuit (V_{IN} = 19V, V_{OUT} = 3.3V to 28V/5A, 140W EPR Application) [11]

Note:

11) The output power can reach 140W for V_{IN} ≥ 19V applications. Consider the thermal derating for different SWA/SWD selections and PCB sizes.

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2024 MPS. All Rights Reserved.

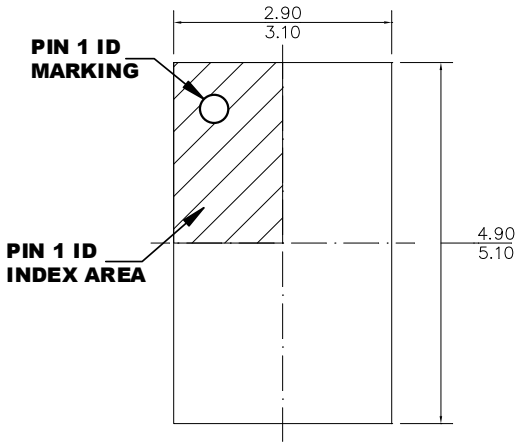
MP4248GQV-0000 CONFIGURATION TABLE

OTP Items	Description	Value
OPERATION	Sets the device's on/off state.	1: On
VOUT_COMMAND	Sets the output voltage.	V_{REF} = 0.5V
DITHER_ENABLE	Enables frequency spread spectrum.	0: Disabled
FREQ	Sets the switching frequency.	01: 420kHz
SWA_FET_RON	Sets SWA's on resistance.	01: 10mΩ
OUTPUT_OVP_EN	Enables output OVP.	1: Enabled (default)
OUTPUT_DISCHARGE_EN	Enables the output discharge function during the VIN, I²C, or EN off period.	1: Enabled (default)
PFM/PWM_MODE	Selects auto-PFM/PWM mode or forced PWM mode.	1: Forced PWM mode (default)
CONSTANT_ CURRENT_LIMIT	Sets the output current limit.	5.4A
LINE_DROP_ COMPENSATION	Sets the output voltage compensation value vs. the load current.	0: Enable line drop compensation (default)
SWITCHING_ CURRENT_LIMIT	Sets the SWB valley current limit and SWC peak current limit.	01: SWC peak12A/SWB valley 9A (default)
RSENS	Selects the value for R_{SENS}.	0: 5mΩ
SLEW_RATE_RISE	Sets the V_{OUT} rising slew rate.	01: 0.16mV/µs(default)
SLEW_RATE_FALL	Sets the V_{OUT} falling slew rate.	01: 0.04mV/µs
FREQ_MODE	Sets the frequency for buck-boost mode	Reduce frequency to half of that in buck and boost mode (default)
CC_DISABLE	Disable CC or enable CC function.	0: Enable CC (default)
CC_BLANK_TIMER	Sets the blanking time before entering CC mode.	00: 250µs (default)
V_{IN} OV Threshold	Select the V_{IN} OV threshold.	0: 38V
V_{IN} UVLO Threshold	Select the V_{IN} UVLO threshold.	0: 2.75V
Absolute Output OVP	Selects the absolute OVP threshold.	1: 39V
OT Warning Function	Enables the OT warning function.	1: Disabled
I2C_ADDRESS	Sets the I²C slave address.	67h
VOUT_MSK	Masks ALT pin indication.	1: Mask
IOUT/POUT_MSK		0: Not Mask
RESERVED_MSK		1: Mask
TEMP_MSK		1: Mask
PG_STATUS#_MSK		1: Mask
PG_ALT_EDGE MSK		1: Mask
GND_SHORT_ VBATT_MSK		1: Mask
UNKNOWN_MSK		1: Mask

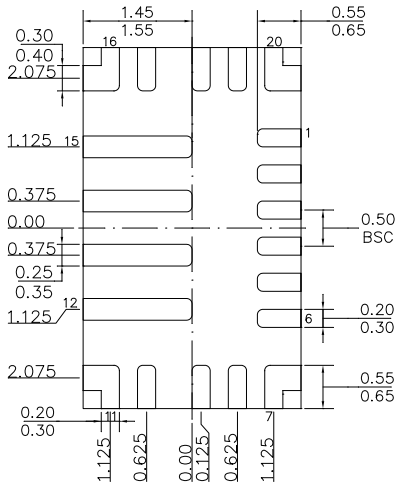
MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2024 MPS. All Rights Reserved.

PACKAGE INFORMATION

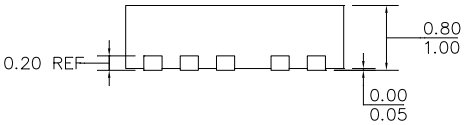
QFN-20 (3mmx5mm)



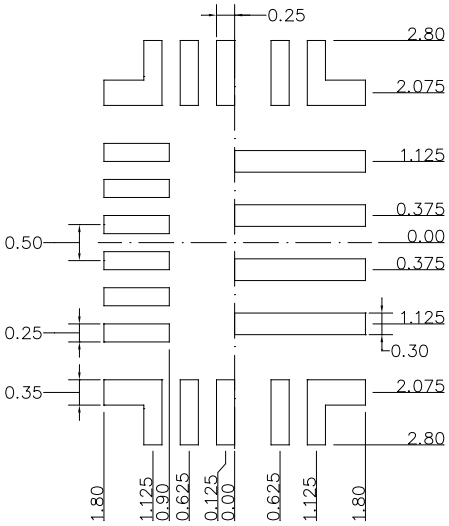
TOP VIEW



BOTTOM VIEW



SIDE VIEW



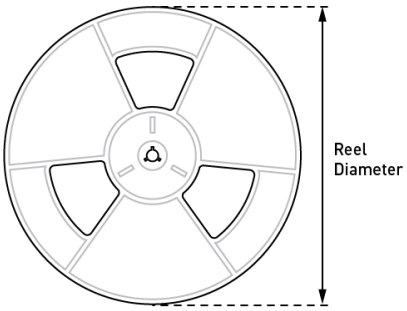
RECOMMENDED LAND PATTERN

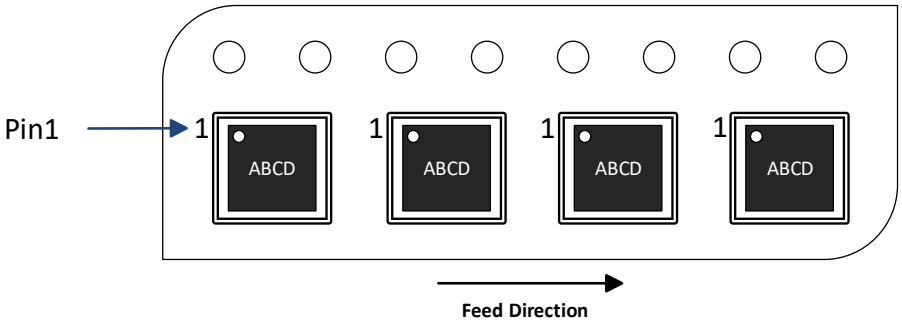
NOTE:

1) ALL DIMENSIONS ARE IN MILLIMETERS.
2) LEAD COPLANARITY SHALL BE 0.08 MILLIMETERS MAX.
3) JEDEC REFERENCE IS MO-220.
4) DRAWING IS NOT TO SCALE.

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2024 MPS. All Rights Reserved.

CARRIER INFORMATION





Part Number	Package Description	Quantity/ Reel	Quantity/ Tube	Quantity/ Tray	Reel Diameter	Carrier Tape Width	Carrier Tape Pitch	Trailer Leader/ Reel
MP4248GQV -0000-Z	QFN-20 (3mmx5mm)	5000	N/A	N/A	13in	12mm	8mm	125&125
MP4248GQV -0011-Z	QFN-20 (3mmx5mm)	5000	N/A	N/A	13in	12mm	8mm	125&125
MP4248GQV -0012-Z	QFN-20 (3mmx5mm)	5000	N/A	N/A	13in	12mm	8mm	125&125
MP4248GQV -xxxx-Z	QFN-20 (3mmx5mm)	5000	N/A	N/A	13in	12mm	8mm	125&125

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2024 MPS. All Rights Reserved.

REVISION HISTORY

Revision #	Revision Date	Description	Pages Updated
1.0	5/23/2024	Initial Release	-

Notice: The information in this document is subject to change without notice. Please contact MPS for current specifications. Users should warrant and guarantee that third-party Intellectual Property rights are not infringed upon when integrating MPS products into any application. MPS will not assume any legal responsibility for any said applications.

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2024 MPS. All Rights Reserved.