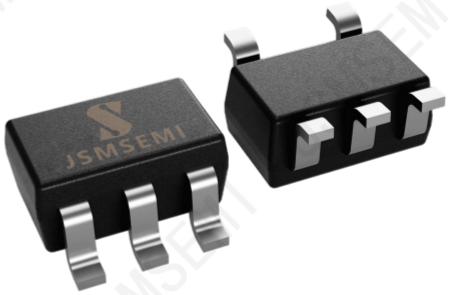
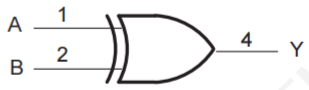
Description

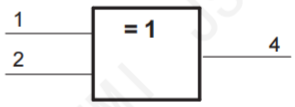
The SN74LVC1G86 device performs the Boolean function $Y = \overline{A}B + A\overline{B}$ in positive logic. This single 2-input exclusive-OR gate is designed for 1.65V to 5.5V V_{CC} operation.

If the input is low, the other input is reproduced in true form at the output. If the input is high, the signal on the other input is reproduced inverted at the output. This device has low power consumption with Typ t_{pd} of 6.7ns at 3.3 V and 15pF capacitive load. The maximum output drive is ±32mA at 4.5 V and ± 24mA at 3V.

This device is fully specified for partial-power-down applications using I_{off}. The I_{off} circuitry disables the outputs, preventing damaging current back flow through the device when it is powered down.







Features

- ESD Protection Exceeds JESD 22
  - 2000-V Human-Body Model
  - 1000-V Charged-Device Model
- Qualified from –40°C to +125°C
- Supports 5V V_{CC} Operation
- Inputs Are Over Voltage Tolerant up to 5.5 V
- Supports Down Translation to V_{CC}
- Typ t_{pd} of 6.7ns at 3.3V
- Low Power Consumption, 1μA Maximum I_{CC} At 85°C
- ±24mA Output Drive at 3V
- I_{off} Supports Partial-Power-Down Mode, and Back-Drive Protection
- Packages: SOT23-6, SOT-363(SC70-6)
- RoSH compatible

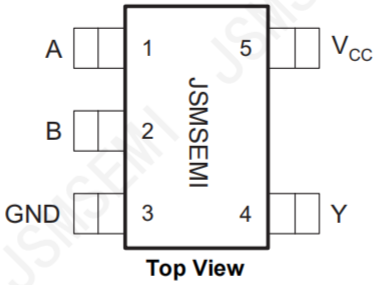
Applications

- Wireless Headsets
- Motor Drives and Controls
- TVs
- Set-Top Boxes
- Audio
- Personal Navigation Device (GPS)
- High-Speed Data Acquisition and Generation

Ordering Information

Order number	Package	Marking	Operation Temperature Range	MSL Grade	Ship,Quantity	Green
SN74LVC1G86DBVR-JSM	SOT-23-5L	C86J	-40 to 125°C	3	TR&3000	Rohs
SN74LVC1G86DCKR-JSM	SOT-353	CH5	-40 to 125°C	3	TR&3000	Rohs

Pin Configuration and Functions



Top View

Pin Functions

PIN		I/O	DESCRIPTION
SOT23-5/SOT353	NAME		
1	A	I	Input A
2	B	I	Input B
3	GND	—	Ground
5	V_{CC}	—	Positive Supply
4	Y	O	Output Y

Specifications

Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

			MIN	MAX	UNIT
V_{CC}	Supply voltage		–0.5	6.5	V
V_I	Input voltage(2)		–0.5	6.5	V
V_O	Voltage applied to any output in the high-impedance or power-off state(2)		–0.5	6.5	V
V_O	Voltage applied to any output in the high or low state(2)(3)		–0.5	V_{CC} + 0.5	V
I_{IK}	Input clamp current	V_I < 0		–50	mA
I_{OK}	Output clamp current	V_O < 0		–50	mA
I_O	Continuous output current			±50	mA
	Continuous current through V_{CC} or GND			±100	mA
T_J	Junction temperature			150	°C
T_{stg}	Storage temperature		–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under Recommended Operating Conditions is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) The input negative-voltage and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
(3) The value of V_{CC} is provided in the Recommended Operating Conditions table.

ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	1000	

Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)(1)

			MIN	MAX	UNIT
V_{CC}	Supply voltage	Operating	1.65	5.5	V
		Data retention only	1.5		
V_{IH}	High-level input voltage	V_{CC} = 1.65 V to 1.95 V	0.65 × V_{CC}		V
		V_{CC} = 2.3 V to 2.7 V	1.7		
		V_{CC} = 3 V to 3.6 V	2		
		V_{CC} = 4.5 V to 5.5 V	0.7 × V_{CC}		
V_{IL}	Low-level input voltage	V_{CC} = 1.65 V to 1.95 V		0.20 × V_{CC}	V
		V_{CC} = 2.3 V to 2.7 V		0.3	
		V_{CC} = 3 V to 3.6 V		0.4	
		V_{CC} = 4.5 V to 5.5 V		0.15 × V_{CC}	
V_I	Input voltage		0	5.5	V
V_O	Output voltage		0	V_{CC}	V
I_{OH}	High-level output current	V_{CC} = 1.65 V		–4	mA
		V_{CC} = 2.3 V		–8	
		V_{CC} = 3 V		–16	
				–24	
		V_{CC} = 4.5 V		–32	
I_{OL}	Low-level output current	V_{CC} = 1.65 V		4	mA
		V_{CC} = 2.3 V		8	
		V_{CC} = 3 V		16	
				24	
		V_{CC} = 4.5 V		32	
$\Delta t/\Delta v$	Input transition rise or fall rate	V_{CC} = 1.8 V ± 0.15 V, 2.5 V ± 0.2 V		20	ns/V
		V_{CC} = 3.3 V ± 0.3 V		10	
		V_{CC} = 5 V ± 0.5 V		5	
T_A	Operating free-air temperature	YZP package	–40	85	°C
		DCK, DBV, and DRL packages	–40	125	

(1) All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation.

Thermal Information

THERMAL METRIC(1)		SN74LVC1G86		UNIT
		SOT-23	SC70	
		5 PINS	5 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	206	252	°C/W

Electrical Characteristics

over recommended operating free-air temperature range (TYP values are at T_A = +25°C, unless otherwise noted.) (1)

PARAMETER		TEST CONDITIONS	V_{CC}	TEMP	MIN	TYP	MAX	UNIT
V_{OH}		I_{OH} = -100μA	1.65V to 5.5V	Full	V_{CC}-0.1			V
		I_{OH} = -4mA	1.65V		1.2			
		I_{OH} = -8mA	2.3V		1.9			
		I_{OH} = -16mA	3V		2.4			
		I_{OH} = -24mA			2.3			
		I_{OH} = -32mA	4.5V		3.8			
V_{OL}		I_{OL} = 100μA	1.65V to 5.5V	Full			0.1	V
		I_{OL} = 4mA	1.65V				0.45	
		I_{OL} = 8mA	2.3V				0.3	
		I_{OL} = 16mA	3V				0.4	
		I_{OL} = 24mA					0.55	
		I_{OL} = 32mA	4.5V				0.55	
I_I	A or B inputs	V_I=5.5V or GND	0V to 5.5V	+25°C		±0.1	±1	μA
				Full			±5	
I_{off}		V_I or V_O=5.5V	0V	+25°C		±0.1	±1	μA
				Full			±10	
I_{CC}		V_I=5.5V or GND, I_O=0	1.65V to 5.5V	+25°C		0.1	1	μA
				Full			10	
ΔI_{CC}		One input at V_{CC}-0.6V, Other inputs at V_{CC} or GND	3V to 5.5V	Full			500	μA

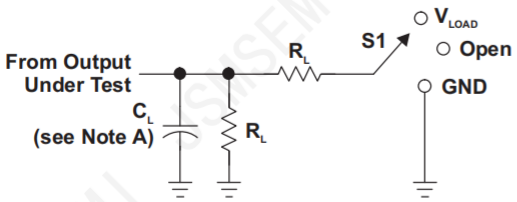
Switching,Operating Characteristics

(T_A =-40°C to +25°C, typical values are at T_A = +25°C, unless otherwise noted.) (1)

PARAMETER	SYMBOL	TEST CONDITIONS		MIN	TYP	MAX	UNIT
Propagation Delay	t_{pd}	V_{CC}=1.8V±0.15V	C_L=30pF, R_L=1kΩ		14.2		ns
		V_{CC}=2.5V±0.2V	C_L=30pF, R_L=500Ω		11.1		
		V_{CC}=3.3V±0.3V	C_L=50pF, R_L=500Ω		6.7		
		V_{CC}=5V±0.5 V	C_L=50pF, R_L=500Ω		5.3		
Input Capacitance	C_i	V_{CC}=3.3V	V_I=V_{CC} or GND		4		pF
Power dissipation capacitance	C_{pd}	V_{CC}=1.8V	f=10MHz		20		pF
		V_{CC}=2.5V			21		
		V_{CC}=3.3V			22		
		V_{CC}=5V			25		

(1) All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation.

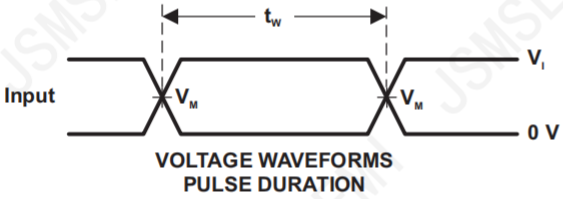
Parameter Measurement Information



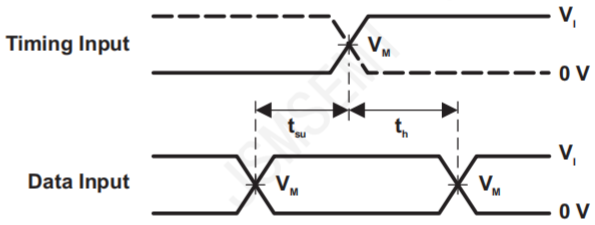
LOAD CIRCUIT

TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	V_{LOAD}
t_{PHZ}/t_{PZH}	GND

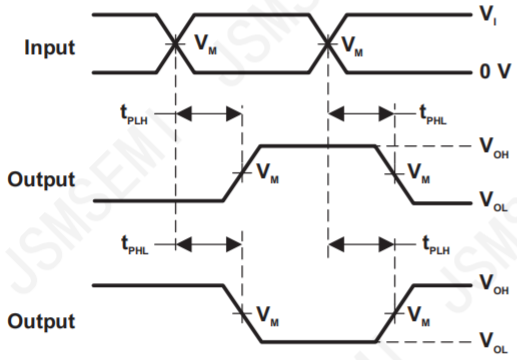
V_{CC}	INPUTS		V_M	V_{LOAD}	C_L		R_L		V_Δ
	V_I	t_r/t_f							
1.8V±0.15V	V_{CC}	≤2ns	$V_{CC}/2$	2 x V_{CC}	15pF	30pF	1MΩ	1kΩ	0.15V
2.5V±0.2V	V_{CC}	≤2ns	$V_{CC}/2$	2 x V_{CC}	15pF	30pF	1MΩ	500Ω	0.15V
3.3V±0.3V	3V	≤2.5ns	1.5V	6V	15pF	50pF	1MΩ	500Ω	0.3V
5V±0.5V	V_{CC}	≤2.5ns	$V_{CC}/2$	2 x V_{CC}	15pF	50pF	1MΩ	500Ω	0.3V



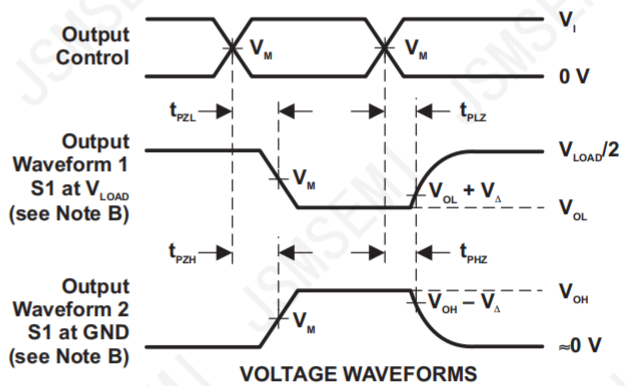
VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
INVERTING AND NONINVERTING OUTPUTS



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING

NOTES: A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω.
D. The outputs are measured one at a time, with one transition per measurement.
E. t_{PLZ} and t_{PHZ} are the same as t_{dis}.
F. t_{PZL} and t_{PZH} are the same as t_{en}.
G. t_{PLH} and t_{PHL} are the same as t_{pd}.
H. All parameters and waveforms are not applicable to all devices.

Figure 1. Load Circuit and Voltage Waveforms

Detailed Description

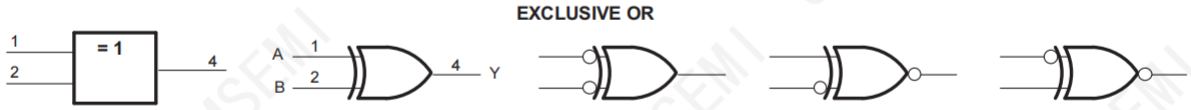
Overview

The SN74LVC1G86 device performs the Boolean function $Y = \overline{A}B + A\overline{B}$ in positive logic. This single 2-input exclusive-OR gate is designed for 1.65-V to 5.5-V V_{CC} operation.

A common application is as a true and complement element. If the input is low, the other input is reproduced in true form at the output. If the input is high, the signal on the other input is reproduced inverted at the output.

This device is fully specified for partial-power-down applications using I_{off}. The I_{off} circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down.

Functional Block Diagram



These are five equivalent exclusive-OR symbols valid for an SN74LVC1G86 gate in positive logic; negation may be shown at any two ports.

Feature Description

Balanced High-Drive CMOS Push-Pull Outputs

A balanced output allows the device to sink and source similar currents. The high drive capability of this device creates fast edges into light loads so routing and load conditions should be considered to prevent ringing. Additionally, the outputs of this device are capable of driving larger currents than the device can sustain without being damaged. It is important for the power output of the device to be limited to avoid thermal runaway and damage due to over-current. The electrical and thermal limits defined the in the Absolute Maximum Ratings must be followed at all times.

Partial Power Down (I_{off})

The inputs and outputs for this device enter a high impedance state when the supply voltage is 0 V. The maximum leakage into or out of any input or output pin on the device is specified by I_{off} in the Electrical Characteristics.

Over-voltage Tolerant Inputs

Input signals to this device can be driven above the supply voltage so long as they remain below the maximum input voltage value specified in the Recommended Operating Conditions.

Function Table

Table 1 lists the functional modes of the SN74LVC1G86 device.

Table 1. Function Table

INPUTS		OUTPUT
A	B	Y
L	L	L
L	H	H
H	L	H
H	H	L

Application Information

The SN74LVC1G86 device can accept input voltages up to 5.5 V at any valid V_{CC} which makes the device suitable for down translation. This feature of the SN74LVC1G86 makes it ideal for various bus interface applications.

Typical Application

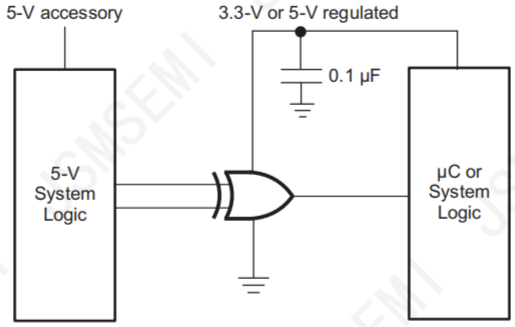


Figure 2. Typical Application Schematic

Design Requirements

This device uses CMOS technology and has balanced output drive. Take care to avoid bus contention because it can drive currents that would exceed maximum limits. The high drive will also create fast edges into light loads, so routing and load conditions should be considered to prevent ringing.

Power Supply Recommendations

The power supply can be any voltage between the minimum and maximum supply voltage rating located in the Recommended Operating Conditions table.

Each V_{CC} pin must have a good bypass capacitor to prevent power disturbance. For devices with a single supply, 0.1 µF is recommended. If there are multiple V_{CC} pins, 0.01 µF or 0.022 µF is recommended for each power pin. It is acceptable to parallel multiple bypass caps to reject different frequencies of noise. A 0.1µF and 1µF are commonly used in parallel. The bypass capacitor must be installed as close to the power pin as possible for best results.

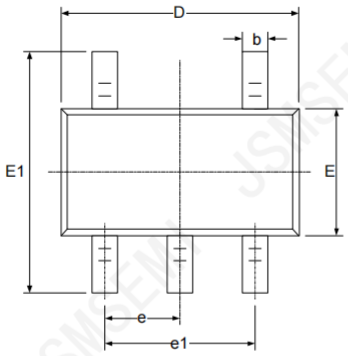
Layout

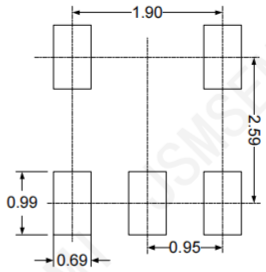
Layout Guidelines

Even low data rate digital signals can have high frequency signal components due to fast edge rates. When a PCB trace turns a corner at a 90° angle, a reflection can occur. A reflection occurs primarily because of the change of width of the trace. At the apex of the turn, the trace width increases to 1.414 times the width. This increase upsets the transmission-line characteristics, especially the distributed capacitance and self–inductance of the trace which results in the reflection. Not all PCB traces can be straight and therefore some traces must turn corners.

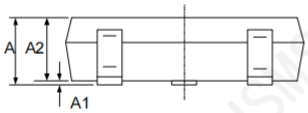
Package Information

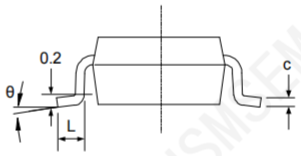
SOT-23-5L





RECOMMENDED LAND PATTERN (Unit: mm)

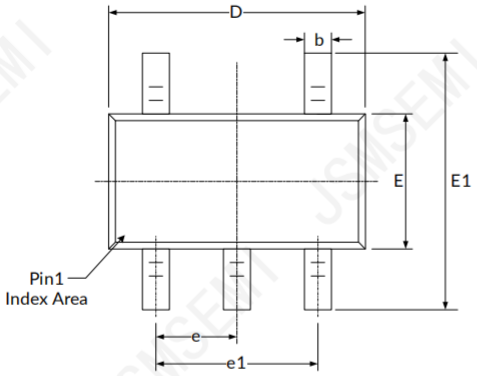


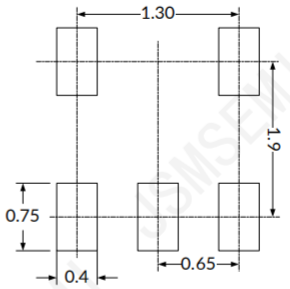


Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	1.050	1.250	0.041	0.049
A1	0.000	0.100	0.000	0.004
A2	1.050	1.150	0.041	0.045
b	0.300	0.500	0.012	0.020
c	0.100	0.200	0.004	0.008
D	2.820	3.020	0.111	0.119
E	1.500	1.700	0.059	0.067
E1	2.650	2.950	0.104	0.116
e	0.950(BSC)		0.037(BSC)	
e1	1.800	2.000	0.071	0.079
L	0.300	0.600	0.012	0.024
θ	0°	8°	0°	8°

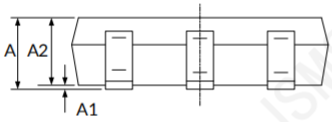
Package Information

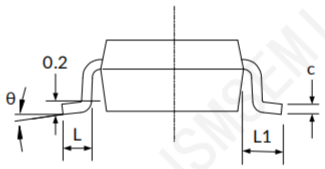
SOT-353(SC70-5)





RECOMMENDED LAND PATTERN (Unit: mm)





Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	0.900	1.100	0.035	0.043
A1	0.000	0.100	0.000	0.004
A2	0.900	1.000	0.035	0.039
b	0.150	0.350	0.006	0.014
c	0.080	0.150	0.003	0.006
D (1)	2.000	2.200	0.079	0.087
E (1)	1.150	1.350	0.045	0.053
E1	2.150	2.450	0.085	0.096
e	0.650(BSC)		0.026(BSC)	
e1	1.300(BSC)		0.051(BSC)	
L	0.260	0.460	0.010	0.018
L1	0.525		0.021	
θ	0°	8°	0°	8°

Revision History

Rev.	Change	Date
V1.0	Initial version	6/27/2021

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