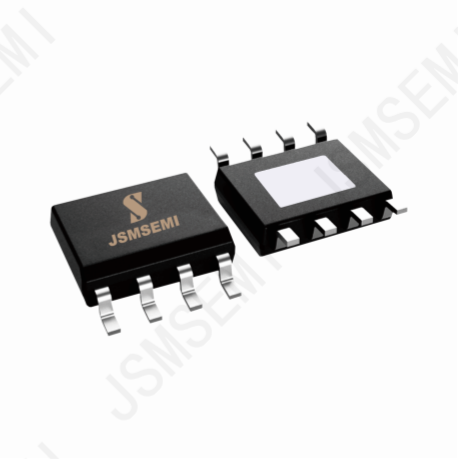
1 Description

The JSM8251 device is an integrated motor driver with N-channel H-bridge, charge pump, current regulation, and protection circuitry. The charge pump improves efficiency by supporting N-channel MOSFET half bridges and 100% duty cycle driving.

The JSM8251 implements a current regulation feature by comparing the analog input VREF and the voltage across a current-sense shunt resistor on the ISEN pin. The ability to limit current can significantly reduce large currents during motor startup and stall conditions.

A low-power sleep mode achieves ultra-low quiescent current draw by shutting down most of the internal circuitry. Internal protection features include supply undervoltage lockout, output overcurrent, and device overtemperature.

The JSM8251 is part of a family of devices which come in pin-to-pin, scalable $R_{DS(on)}$ and supply voltage options to support various loads and supply rails with minimal design changes.

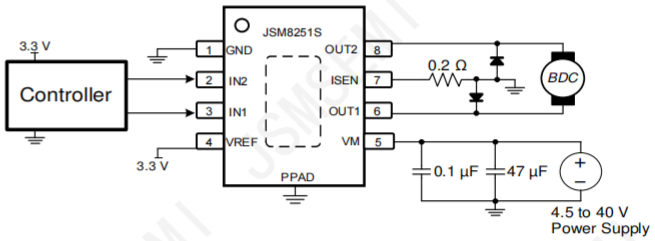


2 Features

- N-channel H-bridge brushed DC motor driver
- 4.5-V to 40-V operating supply voltage range
- Pin-to-pin, $R_{DS(on)}$, voltage, and current sense/ regulation variants
  - JSM8251: 4.5V to 40V, 450mΩ
- High output current capability: 4.0A Peak
- PWM control interface
- Supports 1.8V, 3.3V, and 5V logic inputs
- Integrated current regulation
- Low-power sleep mode
  - <1μA at V_{VM} = 24V, T_J = 25°C
- Small package and footprint
  - ESOP-8
- Integrated protection features
  - VM undervoltage lockout (UVLO)
  - Latched overcurrent protection (OCP)
  - Thermal shutdown (TSD)

3 Applications

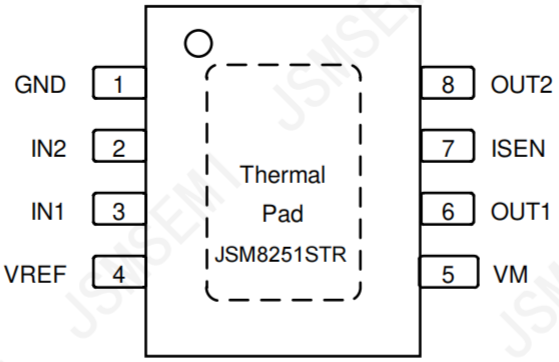
- Printers
- Vacuum robot
- Washer and dryer
- Coffee machine
- POS printer
- Electricity meter
- ATMs (Automated Teller Machines)
- Ventilators
- Surgical equipment
- Electronic hospital bed and bed control
- Fitness machine



Ordering Information

Order number	Package	Marking	Operation Temperature Range	MSL Grade	Ship,Quantity	Green
JSM8251STR	ESOP-8	JSM8251S	-40 to 125°C	3	T&R,4000	Rohs

4 Pin Configuration and Functions



Top View

Pin Functions

PIN		TYPE	DESCRIPTION
NAME	NO.		
GND	1	PWR	Logic ground. Connect to board ground
IN1	3	I	Logic inputs. Controls the H-bridge output.
IN2	2	I	Logic inputs. Controls the H-bridge output.
ISEN	7	PWR	High-current ground path. If using current regulation, connect ISEN to a resistor (low-value, high-power-rating) to ground. If not using current regulation, connect ISEN directly to ground.
OUT1	6	O	H-bridge output. Connect directly to the motor or other inductive load.
OUT2	8	O	H-bridge output. Connect directly to the motor or other inductive load.
VM	5	PWR	4.5-V to 40-V power supply. Connect a 0.1-μF bypass capacitor to ground, as well as sufficient bulk capacitance, rated for the VM voltage.
VREF	4	I	Analog input. Apply a voltage between 0 to 5 V.
PAD		—	Thermal pad. Connect to board ground. For good thermal dissipation, use large ground planes on multiple layers, and multiple nearby vias connecting those planes.

5 Specifications

Absolute Maximum Ratings

over operating temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
Power supply pin voltage	VM	-0.3	40	V
Power supply transient voltage ramp	VM	0	2	V/μs
Logic pin voltage	INx	-0.3	6	V
Reference input pin voltage	VREF	-0.3	6	V
Output pin voltage	OUTx	-0.7	VM + 0.7	V
Current sense input pin voltage	ISEN	-0.5	1	V
Output current	OUTx	Internally Limited	Internally Limited	A
Ambient temperature, T_A		–40	125	°C
Junction temperature, T_J		–40	150	°C
Storage temperature, T_{stg}		–65	150	°C

(1) Operation outside the Absolute Maximum Ratings may cause permanent device damage. Absolute Maximum Ratings do not imply functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions. If used outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.

ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM)	±5000	V
		Charged device model (CDM)	±750	

Recommended Operating Conditions

over operating temperature range (unless otherwise noted)

			MIN	NOM	MAX	UNIT
V_{VM}	Power supply voltage	VM	4.5		38	V
V_{VREF}	Reference voltage	VREF	0		5	V
V_{IN}	Logic input voltage	INx	0		5.5	V
f_{PWM}	PWM frequency	INx	0		200	kHz
I_{OUT} (1)	Peak output current, 4.5 ≤ V_{VM} < 5.5 V	OUTx	0		3.5	A
	Peak output current, V_{VM} ≥ 5.5 V		0		4.0	A
T_A	Operating ambient temperature		–40		125	°C
T_J	Operating junction temperature		–40		150	°C

(1) Power dissipation and thermal limits must be observed

Thermal Information

THERMAL METRIC		JSM8251 (ESOP) 8 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	40.4	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	54.7	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	14.4	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	4.1	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	14.4	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	4.2	°C/W

Electrical Characteristics

Typical values are at T_J = 25 °C and V_{VM} = 24 V.(unless otherwise noted).

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
POWER SUPPLY (VM)						
I_{VMQ}	VM sleep mode current	V_{VM} = 24 V, IN1 = IN2 = 0, T_J = 25°C			5	μA
I_{VM}	VM active mode current	V_{VM} = 24 V, IN1 = IN2 = 1		3	5	mA
t_{WAKE}	Turnon time	Control signal to active mode			250	μs
t_{SLEEP}	Turnoff time	Control signal to sleep mode	0.8		1.5	ms
LOGIC-LEVEL INPUTS (INx)						
V_{IL}	Input logic low voltage				0.5	V
V_{IH}	Input logic high voltage		1.5			V
V_{HYS}	Input hysteresis			200		mV
I_{IL}	Input logic low current	V_{IN} = 0 V	-1		1	μA
I_{IH}	Input logic high current	V_{IN} = 3.3 V		33	100	μA
R_{PD}	Input pulldown resistance	To GND		100		kΩ
DRIVER OUTPUTS (OUTx)						
$R_{DS(on)\_HS}$	High-side MOSFET on resistance	V_{VM} = 24 V, I = 1 A, f_{PWM} = 25 kHz		225		mΩ
$R_{DS(on)\_LS}$	Low-side MOSFET on resistance	V_{VM} = 24 V, I = 1 A, f_{PWM} = 25 kHz		225		mΩ
V_{SD}	Body diode forward voltage	I_{OUT} = 1 A		0.8		V
t_{RISE}	Output rise time	V_{VM} = 24 V, OUTx rising from 10% to 90%		160		ns
t_{FALL}	Output fall time	V_{VM} = 24 V, OUTx falling from 90% to 10%		150		ns
t_{PD}	Input to output propagation delay	INx to OUTx		0.7		μs
t_{DEAD}	Output dead time			300		ns
SHUNT CURRENT SENSE AND REGULATION (ISEN, VREF)						
A_V	ISEN gain	VREF = 2.5 V		10		V/V
t_{OFF}	Current regulation off time			25		μs
t_{BLANK}	Current regulation blanking time			1.5		μs
PROTECTION CIRCUITS						
V_{UVLO}	Supply undervoltage lockout (UVLO)	Supply rising		4.5		V
		Supply falling		4.4		V
V_{UVLO_HYS}	Supply UVLO hysteresis	Rising to falling threshold		100		mV
t_{UVLO}	Supply undervoltage deglitch time			10		μs
I_{OCP}	Overcurrent protection trip point	4.5 ≤ V_{VM} < 5.5 V		3.5		A
		V_{VM} ≥ 5.5 V		4.0		A
t_{RETRY}	Overcurrent protection stabilization time			3		μs
t_{OCP}	Overcurrent protection deglitch time			5		μs
T_{TSD}	Thermal shutdown temperature		150	175		°C
T_{HYS}	Thermal shutdown hysteresis			40		°C

6 Detailed Description

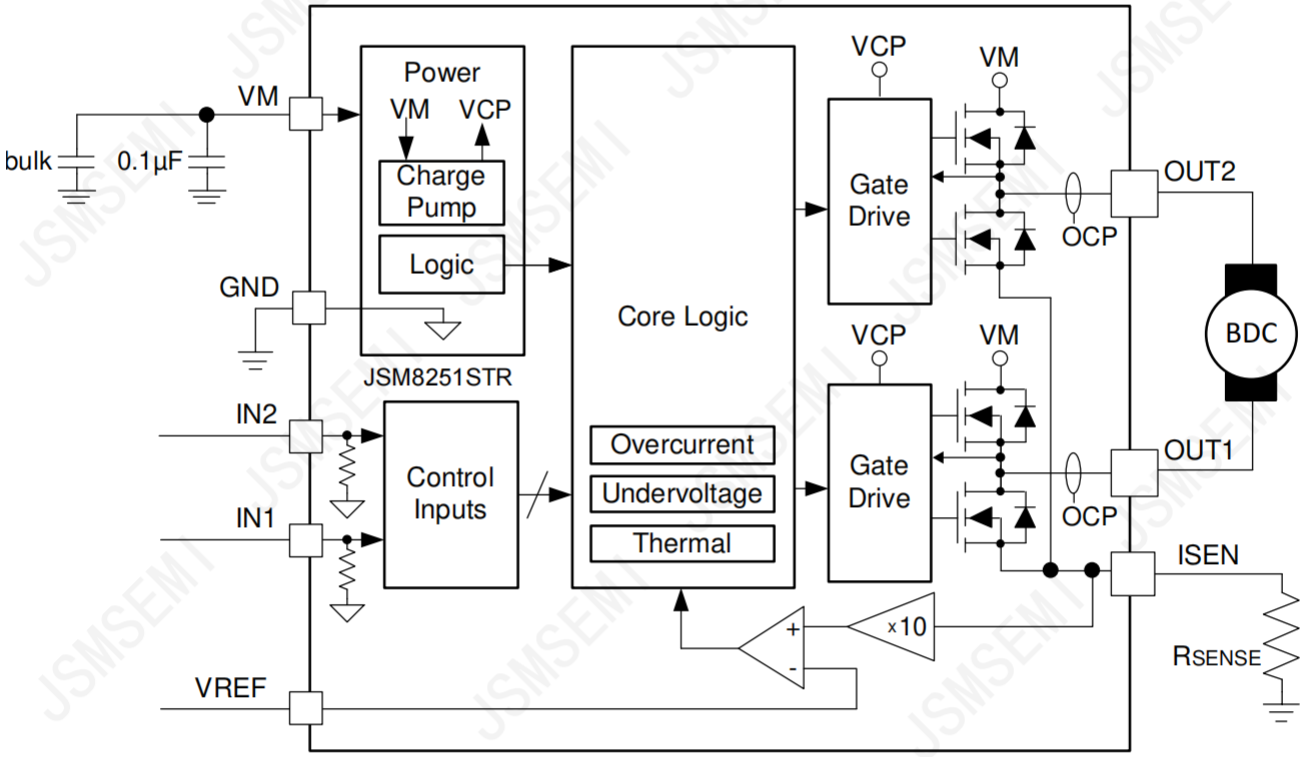
Overview

The JSM8251 is an 8-pin device for driving brushed DC motors from a 4.5-V to 40-V supply rail. Two logic inputs control the H-bridge driver, which consists of four N-channel MOSFETs that have a typical $R_{DS(on)}$ of 450 mΩ (including one high-side and one low-side FET). A single power input, VM, serves as both device power and the motor winding bias voltage. The integrated charge pump of the device boosts VM internally and fully enhances the high-side FETs. Motor speed can be controlled with pulse-width modulation at frequencies between 0 to 100 kHz. The device enters a low-power sleep mode by bringing both inputs low.

The JSM8251 also integrates current regulation using an external shunt resistor on the ISEN pin. This allows the device to limit the output current with a fixed off-time PWM chopping scheme to limit inrush and stall currents. The current regulation level can be configured during motor operation through the VREF pin to limit the load current accordingly to the system demands.

A variety of integrated protection features protect the device in the case of a system fault. These include undervoltage lockout (UVLO), overcurrent protection (OCP), and overtemperature shutdown (TSD).

Functional Block Diagram



External Components

Table 6-1 lists the recommended external components for the device.

Table 6-1. Recommended external components

COMPONENT	PIN 1	PIN 2	RECOMMENDED
C_{VM1}	VM	GND	0.1-µF, low ESR ceramic capacitor, VM-rated.
C_{VM2}	VM	GND	VM-rated.

Feature Description

Bridge Control

The JSM8251 output consists of four N-channel MOSFETs that are designed to drive high current. These outputs are controlled by the two logic inputs IN1 and IN2 as listed in Table 6-2.

Table 6-2. H-Bridge Control

IN1	IN2	OUT1	OUT2	DESCRIPTION
0	0	High-Z	High-Z	Coast; H-bridge disabled to High-Z (sleep entered after 1 ms)
0	1	L	H	Reverse (Current OUT2 → OUT1)
1	0	H	L	Forward (Current OUT1 → OUT2)
1	1	L	L	Brake; low-side slow decay

The inputs can be set to static voltages for 100% duty cycle drive, or they can be pulse-width modulated (PWM) for variable motor speed. When using PWM, switching between driving and braking typically works best. For example, to drive a motor forward with 50% of the maximum RPM, IN1 = 1 and IN2 = 0 during the driving period, and IN1 = 1 and IN2 = 1 during the other period. Alternatively, the coast mode (IN1 = 0, IN2 = 0) for *fast current decay* is also available where the PWM signal is applied to one IN pin and the other IN pin remains at a low leve. Figure 6-1 shows how the motor current flows through the H-bridge. The input pins can be powered before VM is applied.

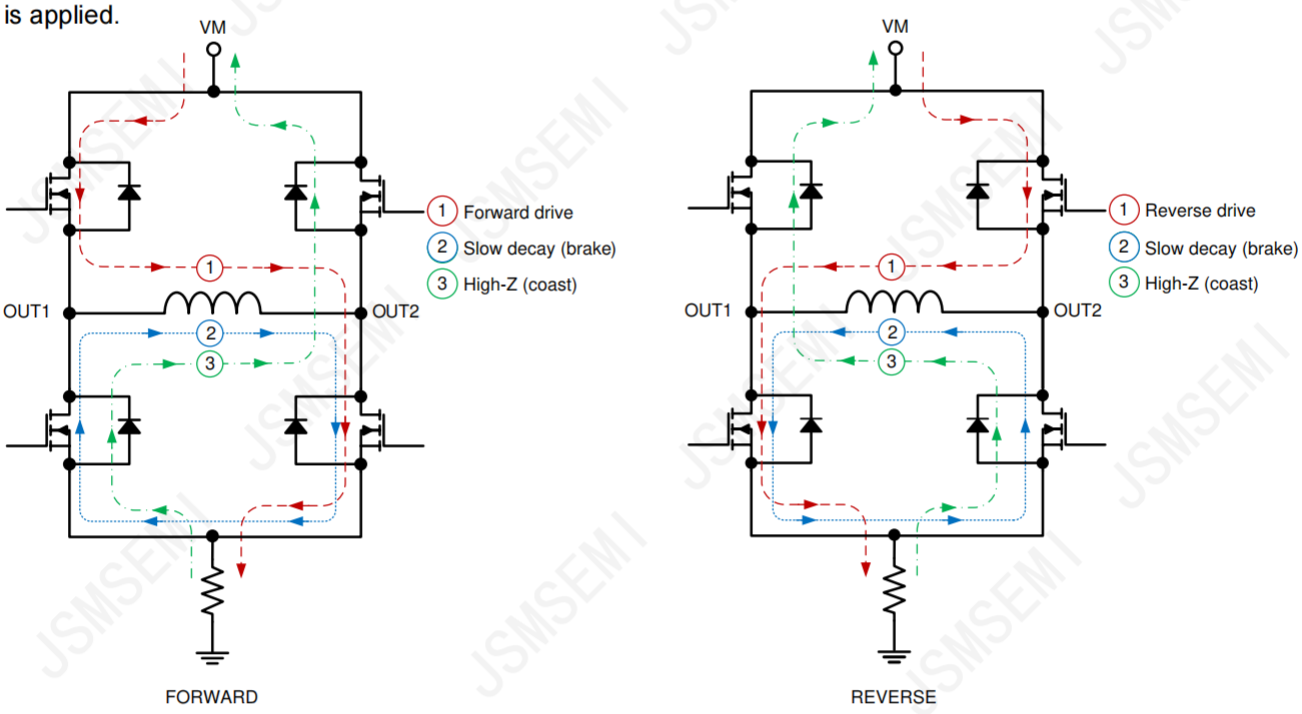


Figure 6-1. H-Bridge Current Paths

When an output changes from driving high to driving low, or driving low to driving high, dead time is automatically inserted to prevent shoot-through. The t_{DEAD} time is the time in the middle when the output is High-Z. If the output pin is measured during t_{DEAD}, the voltage depends on the direction of current. If the current is leaving the pin, the voltage is a diode drop below ground. If the current is entering the pin, the voltage is a diode drop above VM. This diode is the body diode of the high-side or low-side FET.

The propagation delay time (t_{PD}) is measured as the time between an input edge to output change. This time accounts for input deglitch time and other internal logic propagation delays. The input deglitch time prevents noise on the input pins from affecting the output state. Additional output slew delay timing accounts for FET turn on or turn off times (t_{RISE} and t_{FALL}).

Figure 6-2 below shows the timing of the inputs and outputs of the motor driver.

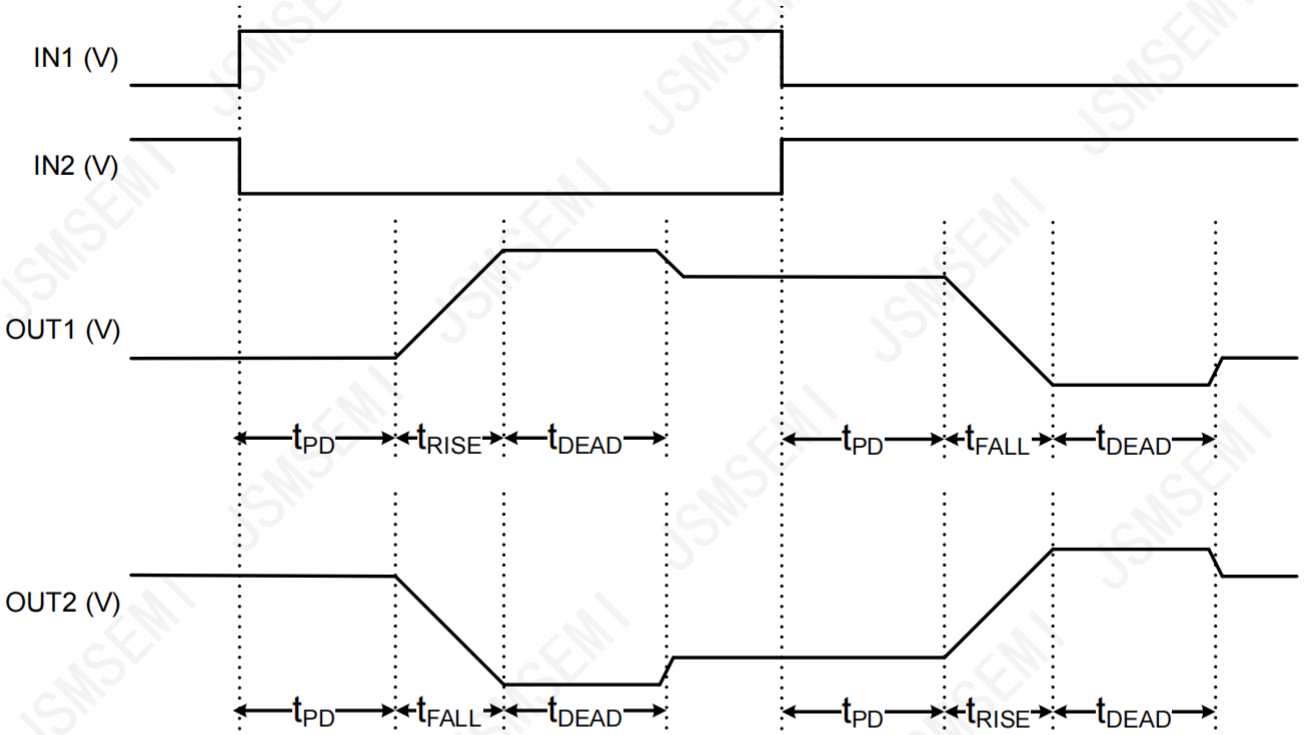


Figure 8-2. H-Bridge Timing Diagram

Current Regulation

The JSM8251 device limits the output current based on the analog input, VREF, and the resistance of an external sense resistor on the ISEN pin, R_{SENSE}, according to the following formula:

$$I_{TRIP} = \frac{VREF}{A_V \times R_{SENSE}} = \frac{VREF}{10 \times R_{SENSE}}$$

By using current regulation, the device input pins can be set for 100% duty cycle, while the device switches the outputs to keep the motor current at the I_{TRIP} level. For example, if VREF = 3.3 V and a R_{SENSE} = 0.15 Ω, the JSM8251 limits motor current to 2.2 A during high torque conditions.

When the motor current exceeds the ITRIP threshold, the output will be triggered to enter a current chopping mode with a fixed off-time (tOFF). During tOFF, the H-bridge will enter a braking slow decay state (both low-side MOSFETs are in a conducting state) for a duration of tOFF after IOut exceeds ITRIP. After tOFF, if IOut is less than ITRIP, the output will be re-enabled based on INx. If the state of INx changes during tOFF, the remaining tOFF time will be ignored, and the output will once again follow the input signal.

The ITRIP comparator features a blanking time (tBLK) to prevent voltage and current transients from affecting current limit regulation during output switching moments.

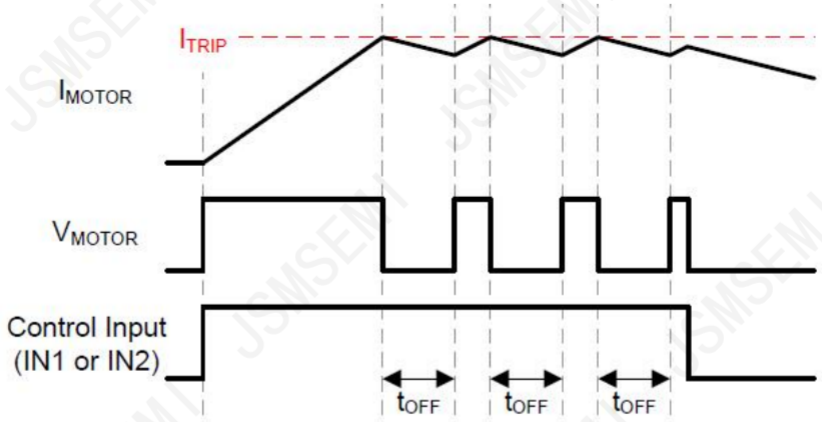


Figure 6-3. Current-limiting regulation waveform

After t_{OFF} elapses, the output is re-enabled according to the two inputs, INx. The drive time (t_{DRIVE}) until reaching another I_{TRIP} event heavily depends on the VM voltage, the back-EMF of the motor, and the inductance of the motor.

Shorting ISEN to GND and setting the VREF pin voltage to 0.3V~5V can disable the internal current limiting adjustment function. This provides the highest-possible peak current which is up to $I_{OCP,min}$ for a few hundred milliseconds (depending on PCB characteristics and the ambient temperature). If current exceeds $I_{OCP,min}$, the device may enter the fault mode due to overcurrent protection (OCP) or overtemperature shutdown (TSD).

Protection Circuits

The JSM8251 device is fully protected against VM undervoltage, overcurrent, and overtemperature events.

Overcurrent Protection (OCP)

Each FET in the H-bridge has a current limiting circuit that controls the gate drive to limit the current through the FET. If the drive current exceeds the threshold I_{OCP} for a duration longer than the overcurrent protection debounce time (t_{OCP}), all FETs in the H-bridge are turned off. After maintaining the OCP retry time (t_{RETRY}), the H-bridge output is restored. If the overcurrent condition persists, the above operation will be repeated.

Overcurrent conditions are detected independently on both high- and low-side FETs. This means that a short to ground, supply, or across the motor winding will all result in an overcurrent shutdown. Overcurrent protection is not used in current detection circuits for current limiting regulation, so its function is not affected by the settings of VREF and ISEN.

Thermal Shutdown (TSD)

If the die temperature exceeds safe limits, all FETs in the H-bridge are disabled. After the die temperature has fallen to a safe level, operation automatically resumes,If the device tends to enter a thermal shutdown (TSD) state, it indicates that the device has excessive power consumption, insufficient heat dissipation, or the ambient temperature exceeds the recommended operating conditions.

VM Undervoltage Lockout (UVLO)

Whenever the voltage on the VM pin falls below the UVLO falling threshold voltage, V_{UVLO}, all circuitry in the device is disabled, the output FETS are disabled, and all internal logic is reset. Operation continues when the V_{VM} voltage rises above the UVLO rising threshold.

Device Functional Modes

Table 6-3 summarizes the JSM8251 functional modes described in this section.

Table 6-3. Modes of Operation

MODE	CONDITION	H-BRIDGE	INTERNAL CIRCUITS
Active Mode	IN1 or IN2 = logic high	Operating	Operating
Low-Power Sleep Mode	IN1 = IN2 = logic low	Disabled	Disabled
Fault Mode	Any fault condition met	Disabled	See Table 6-4

Active Mode

After the supply voltage on the VM pin has crossed the undervoltage threshold V_{UVLO}, the INx pins are in a state other than IN1 = 0 & IN2 = 0, and t_{WAKE} has elapsed, the device enters active mode. In this mode, the H-bridge, charge pump, and internal logic are active and the device is ready to receive inputs.

Low-Power Sleep Mode

When the IN1 and IN2 pins are both low for time t_{SLEEP}, the JSM8251 device enters a low-power sleep mode. In sleep mode, the outputs remain High-Z and the device draws minimal current from the supply pin (I_{VMQ}). If the device is powered up while all inputs are low, it immediately enters sleep mode. After any of the input pins are set high for longer than the duration of t_{WAKE}, the device becomes fully operational.

Fault Mode

The JSM8251 device enters a fault mode when a fault is encountered. This is utilized to protect the device and the output load. The device behavior in the fault mode is described in and depends on the fault condition. The device will leave the fault mode and re-enter the active mode when the recovery condition is met.

Table 6-4. Fault Conditions Summary

FAULT	CONDITION	H-BRIDGE	INTERNAL CIRCUITS	RECOVERY
VM undervoltage (UVLO)	$V_M < V_{UVLO,falling}$	Disabled	Disabled	$V_M > V_{UVLO,rising}$
Overcurrent (OCP)	$I_{OUT} > I_{OCP}$	Disabled	Operating	$I_{OUT} < I_{OCP}$ and device is power cycled or reset using sleep mode
Thermal Shutdown (TSD)	$T_J > T_{TSD}$	Disabled	Operating	$T_J < T_{TSD} - T_{HYS}$

7 Application Information

The JSM8251 device is typically used to drive one brushed DC motor.

Typical Application-Brush DC Motor

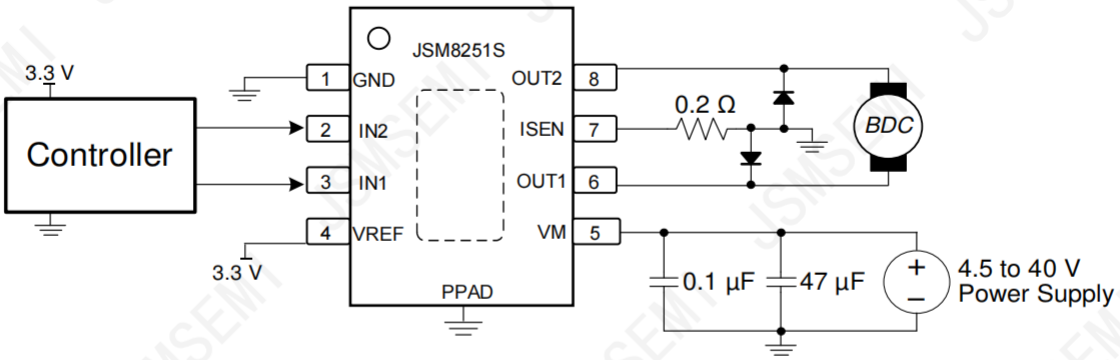


Figure 7-1. Typical Connections

Detailed Design Procedure

Motor Voltage

The motor voltage to use depends on the ratings of the motor selected and the desired RPM. A higher voltage spins a brushed DC motor faster with the same PWM duty cycle applied to the power FETs. A higher voltage also increases the rate of current change through the inductive motor windings.

Motor Current

Motors experience large currents at low speed, initial startup, and stalled rotor conditions. The large current at motor startup is sometimes called inrush current. The current regulation feature in the JSM8251 can help to limit these large currents.

Alternatively, the microcontroller may limit the inrush current by ramping the PWM duty cycle during the startup time,The maximum RMS current is related to PCB design, ambient temperature, and PWM frequency. Generally, a PWM frequency of 200kHz results in a 20% increase in switching losses compared to 20kHz.

Sense Resistor

For optimal performance, the sense resistor must have the following characteristics:

- Surface-mount
- Low inductance
- Rated for high enough power
- Try to get as close as possible to the ISEN pin of the chip

The power dissipated by the sense resistor equals $(I_{AVG})^2 \times R$. For example, if peak motor current is 3 A, average motor current is 1.5 A, and a 0.2Ω sense resistor is used, the resistor dissipates $1.5\ A^2 \times 0.2\ \Omega = 0.45$ W . The power quickly increases with higher current levels.

Resistors typically have a rated power within some ambient temperature range, along with a derated power curve for high ambient temperatures. When a PCB is shared with other components generating heat, the system designer should add margin. Measuring the actual sense resistor temperature in a final system is always best.

Because power resistors are larger and more expensive than standard resistors, using multiple standard resistors in parallel, between the sense node and ground, is common and distributes the current and heat dissipation.

Selection of anti-kickback diode

When driving a high-current motor, a large kickback current will be generated during braking. To prevent damage to the chip, it is recommended to connect OUT1 and OUT2 to ground through inverting diodes, in order to increase the inverting freewheeling capability of the lower transistor.

Typical Application-Relay Driving

The PWM interface may also be used to drive single- and dual-coil latching relays, as shown in the figures below.

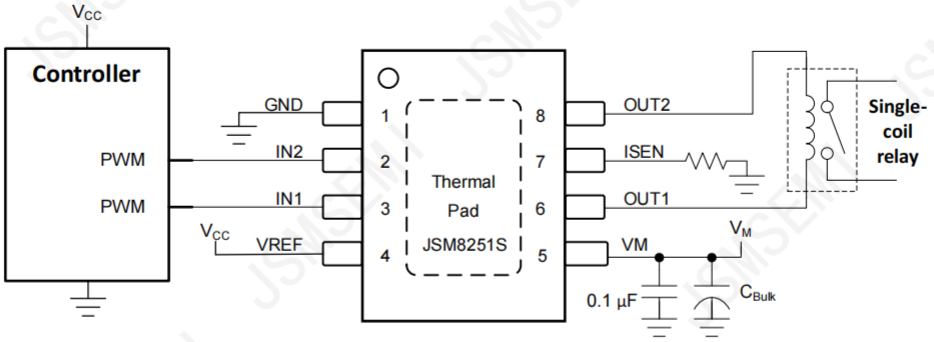


Figure 7-2. Single-Coil Relay Driving

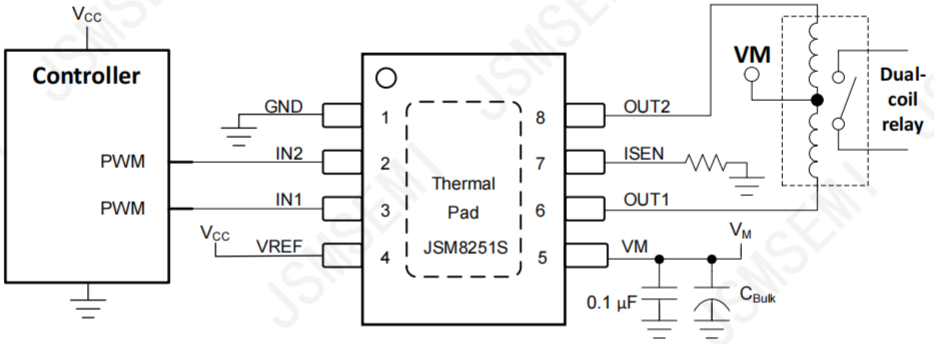


Figure 7-3. Dual-Coil Relay Driving

Design Requirements

Table 7-3 provides example requirements for a single- or dual-coil relay application. Current regulation may also be configured to ensure the relay current is within the relay specification. This is important if the VM supply voltage is higher than the voltage rating of the relay.

Table 7-1. System design requirements

DESIGN PARAMETER	REFERENCE	EXAMPLE VALUE
Motor supply voltage	V_M	12 V
Microcontroller supply voltage	V_{CC}	3.3 V
Single coil relay current	I_{Relay}	500 mA pulse for 200 ms
Dual coil relay current	I_{OUT1}, I_{OUT2}	100 mA pulse for 200 ms

Detailed Design Procedure

Control Interface for Single-Coil Relays

The PWM interface can be used to drive single-coil relays. To actuate the relay, the driver needs to drive current with either the forward or reverse states in the PWM table. After driving the relay, the outputs can be disabled (IN1=IN2=0) to put the driver to sleep and save energy. Alternatively, the outputs can be put into brake mode briefly after actuation to avoid back EMF effects from the relay or causing current to flow back from the relay into the VM supply node.

Control Interface for Dual-Coil Relays

A dual coil relay only require two low-side drivers if the center tap is connected to VM. The body diodes of the unused FETs act as freewheeling diodes, so additional freewheeling diodes are not needed when driving a dual-coil relay with the JSM8251. The PWM interface can be used to control the dual-coil relay.

8 Power Supply Recommendations

Bulk Capacitance

Having appropriate local bulk capacitance is an important factor in motor drive system design. Having more bulk capacitance is generally beneficial, while the disadvantages are increased cost and physical size.

The amount of local capacitance needed depends on a variety of factors, including:

- The highest current required by the motor system
- The capacitance of the power supply and ability to source current
- The amount of parasitic inductance between the power supply and motor system
- The acceptable voltage ripple
- The type of motor used (brushed DC, brushless DC, stepper)
- The motor braking method

The inductance between the power supply and motor drive system limits how the rate current can change from the power supply. If the local bulk capacitance is too small, the system responds to excessive current demands or dumps from the motor with a change in voltage. When adequate bulk capacitance is used, the motor voltage remains stable and high current can be quickly supplied.

The data sheet generally provides a recommended value, but system-level testing is required to determine the appropriate sized bulk capacitor.

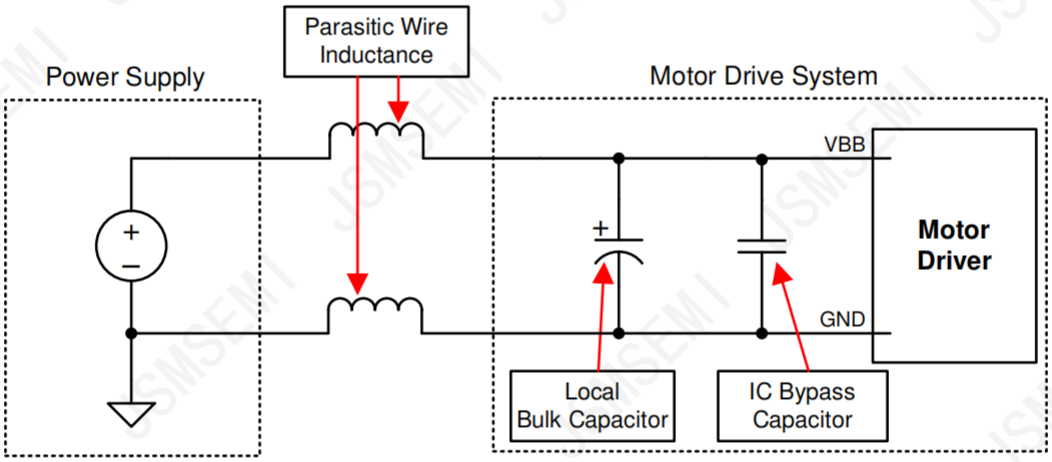


Figure 8-1. Example Setup of Motor Drive System With External Power Supply

The voltage rating for bulk capacitors should be higher than the operating voltage, to provide margin for cases when the motor transfers energy to the supply.

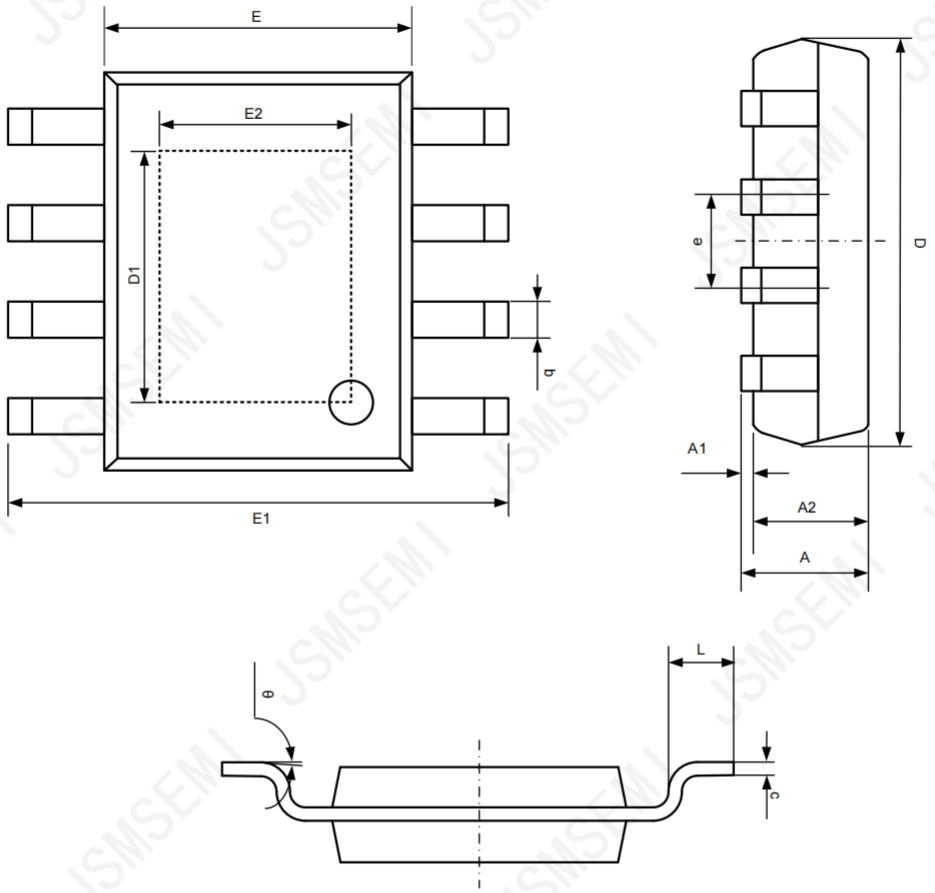
9 Layout Guidelines

Since the JSM8251 integrates power MOSFETs capable of driving high current, careful attention should be paid to the layout design and external component placement. Some design and layout guidelines are provided below.

- Low ESR ceramic capacitors should be utilized for the VM to GND bypass capacitor. X5R and X7R types are recommended.
- The VM power supply capacitors should be placed as close to the device as possible to minimize the loop inductance.
- The VM power supply bulk capacitor can be of ceramic or electrolytic type, but should also be placed as close as possible to the device to minimize the loop inductance.
- VM, OUT1, OUT2, and PGND carry the high current from the power supply to the outputs and back to ground. Thick metal routing should be utilized for these traces as is feasible.
- The device thermal pad should be attached to the PCB top layer ground plane and internal ground plane (when available) through thermal vias to maximize the PCB heat sinking.
- A recommended land pattern for the thermal vias is provided in the package drawing section.
- The copper plane area attached to the thermal pad should be maximized to ensure optimal heat sinking.

Package Information

ESOP-8



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	1.350	1.750	0.053	0.069
A1	0.050	0.150	0.002	0.006
A2	1.350	1.550	0.053	0.061
b	0.330	0.510	0.013	0.020
c	0.170	0.250	0.007	0.010
D	4.700	5.100	0.185	0.200
D1	2.8	3.420	0.11	0.134
E	3.800	4.000	0.150	0.157
E1	5.800	6.200	0.228	0.244
E2	2.11	2.7	0.083	0.106
e	1.270(BSC)		0.050(BSC)	
L	0.400	1.270	0.016	0.050
θ	0°	8°	0°	8°

Revision History

Rev.	Change	Date
V1.0	Initial version	3/27/2023

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