

Description

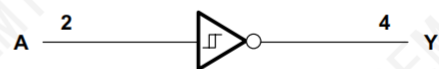
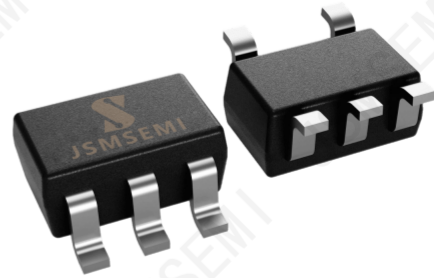
The 74AHCT1G14 contains a single inverter gate.

The device performs the Boolean function $Y = A$.

The device functions as an independent inverter with Schmitttrigger inputs, so the device has different input threshold levels for positive-going (V_{T+}) and negative going (V_{T-}) signals to provide hysteresis (ΔV_T) which makes the device tolerant to slow or noisy input signals.

This device is fully specified for partial-power-down applications using Ioff. The Ioff circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down.

The 74AHCT1G14 is available in Green SOT23-5 and SOT-353 packages. It operates over an ambient temperature range of -40°C to $+125^{\circ}\text{C}$.



Logic Diagram (positive Logic)

INPUTS	OUTPUT
A	Y
H	L
L	H

Features

- Operating Range: 2.0 V to 5.5 V
- Typ t_{pd} of 7.6ns at 5V
- Low power consumption, 1 μA max I_{CC}
- $\pm 32\text{mA}$ output drive at 5V
- Inputs are TTL-voltage compatible
- Ioff Supports Partial-Power-Down Mode Operation
- Operating Temperature Range: -40°C to $+125^{\circ}\text{C}$
- Packages: SOT23-5, SC70-5
- RoSH compatible

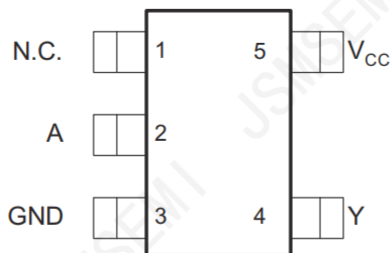
Applications

- Enable or disable a digital signal
- Controlling an indicator LED
- AC Receiver
- Blu-ray Players and Home Theaters
- Desktops or Notebook PCs
- Digital Video Cameras (DVC)
- Mobile Phones
- Personal Navigation Device (GPS)
- Portable Media Player
- Translation between communication modules and system controllers

Ordering Information

Order number	Package	Marking	Operation Temperature Range	MSL Grade	Ship,Quantity	Green
74AHCT1G14GV,125-JSM	SOT-23-5L	B14S	-40 to 125°C	3	TR&3000	Rohs
74AHCT1G14GW,125-JSM	SOT-353	BFG	-40 to 125°C	3	TR&3000	Rohs

Pin Configuration and Functions



SOT-23-5L, SOT-353 (Top View)

Pin Functions

PIN		TYPE ⁽¹⁾	DESCRIPTION
NO.	NAME		
1	NC	—	No connect
2	A	I	Data Input
3	GND	—	Ground
4	Y	O	Data Output
5	V _{CC}	—	Power

(1) Signal Types: I = Input, O = Output, I/O = Input or Output

Specifications

Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)⁽¹⁾

		MIN	MAX	UNIT
V _{CC}	Supply voltage range	−0.5	6.5	V
V _I ⁽²⁾	Input voltage range	−0.5	6.5	V
V _O ⁽²⁾	Output voltage range	−0.5	V _{CC} + 0.5	V
I _{IK}	Input clamp current (V _I < 0)		−50	mA
I _{OK}	Output clamp current (V _O < 0 or V _O > V _{CC})		±50	mA
I _O	Continuous output current (V _O = 0 to V _{CC})		±50	mA
	Continuous current through V _{CC} or GND		±100	mA
T _{stg}	Storage temperature range	−65	150	°C

(1) Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under Recommended Operating Conditions. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

(2) The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)⁽¹⁾

		MIN	MAX	UNIT
V _{CC}	Supply voltage	2.0	5.5	V
V _I	Input voltage	0	5.5	V
V _O	Output voltage	0	V _{CC}	V
I _{OH}	High-level output current		−8	mA
I _{OL}	Low-level output current		8	mA
T _A	Operating free-air temperature	−40	125	°C

(1) All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation.

Thermal Information

THERMAL METRIC ⁽¹⁾	74AHCT1G14		UNIT
	SOT-23-5L	SOT-353	
	5 PINS	5 PINS	
$R_{\theta JA}$ Junction-to-ambient thermal resistance	208	283	°C/W

Electrical Characteristics—DC Limit Changes

over recommended operating free-air temperature range (TYP values are at $T_A = +25^\circ\text{C}$, Full= -40°C to 125°C , unless otherwise noted.)

PARAMETER	TEST CONDITIONS	V_{CC}	TEMP	MIN ⁽²⁾	TYP ⁽³⁾	MAX ⁽²⁾	UNIT
V_{T+}	Positive going input threshold voltage	2.0V	Full	0.7		1.2	V
		3.3V		1		1.5	
		4.5V to 5.5V		1.2		2	
V_{T-}	Negative going input threshold voltage	2.0V	Full	0.3		0.6	V
		3.3V		0.5		0.9	
		4.5V to 5.5V		0.6		1.2	
ΔV_T	Hysteresis ($V_{T+}-V_{T-}$)	2.0V	Full	0.3		0.8	V
		3.3V		0.3		1	
		4.5V to 5.5V		0.3		1.2	
V_{OH}	$I_{OH} = -100\mu\text{A}$	2.0V to 5.5V	Full	$V_{CC}-0.1$			V
	$I_{OH} = -8\text{mA}$	2.0V		1.6			
	$I_{OH} = -24\text{mA}$	3.3V		2.5			
		4.5V		3.8			
	$I_{OH} = -32\text{mA}$	5.0V		4.2			
		5.5V		4.8			
V_{OL}	$I_{OL} = 100\mu\text{A}$	2.0V to 5.5V	Full			0.1	V
	$I_{OL} = 8\text{mA}$	2.0V				0.45	
	$I_{OL} = 24\text{mA}$	3.3V				0.55	
		4.5V				0.55	
	$I_{OL} = 32\text{mA}$	5.0V				0.5	
		5.5V				0.45	
I_i	A input	$V_i=5.5\text{V}$ or GND	0V to 5.5V	+25°C	± 0.1	± 1	μA
				Full		± 10	
I_{off}	V_i or $V_o=5.5\text{V}$	0V		+25°C	± 0.1	± 1	μA
				Full		± 10	
I_{CC}	$V_i=5.5\text{V}$ or GND, $I_o=0$	2.0V to 5.5V		+25°C	0.1	1	μA
				Full		10	
I_{CCT}	One input at 3.4V, Other inputs at V_{CC} or GND	5.5V	Full			500	μA

(1) All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation.

(2) Limits are 100% production tested at 25°C . Limits over the operating temperature range are ensured through correlations using statistical quality control (SQC) method.

(3) Typical values represent the most likely parametric norm as determined at the time of characterization. Actual typical values may vary over time and will also depend on the application and configuration.

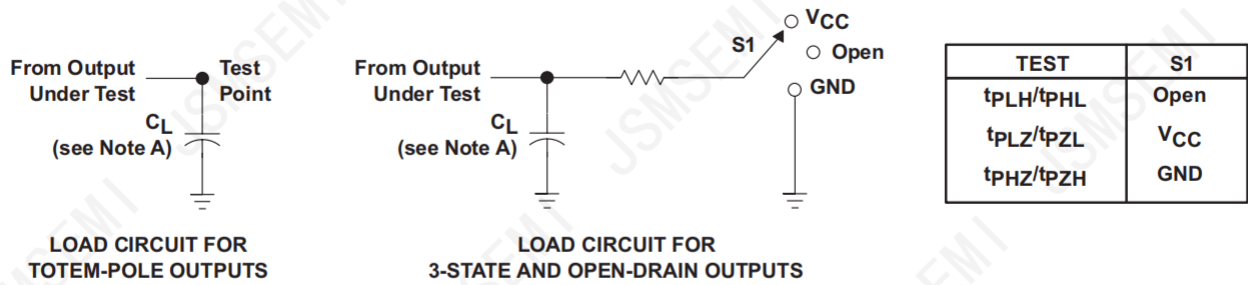
Electrical Characteristics—AC Limit Changes

PARAMETER	SYMBOL	TEST CONDITIONS		TEMP	MIN ⁽²⁾	TYP ⁽³⁾	MAX ⁽²⁾	UNIT
Propagation Delay	t_{pd}	$V_{CC}=2.0V\pm0.2V$	$C_L=30pF, R_L=500\Omega$	$+25^\circ C$		29		ns
		$V_{CC}=3.3V\pm0.3V$	$C_L=50pF, R_L=500\Omega$			10.4		
		$V_{CC}=5V\pm0.5V$	$C_L=50pF, R_L=500\Omega$			7.6		
Input Capacitance	C_i	$V_{CC}=5V$	$V_I=V_{CC}$ or GND	$+25^\circ C$		4.2		pF
Power dissipation capacitance	C_{pd}	$V_{CC}=5V$	$f=10MHz$	$+25^\circ C$		16.6		pF

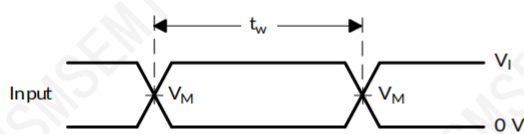
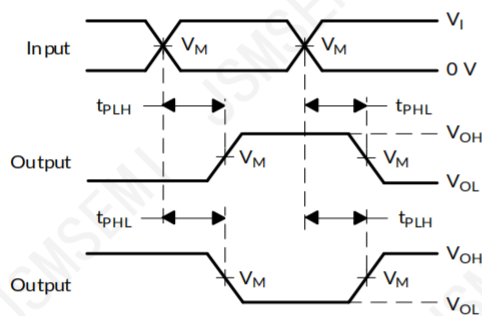
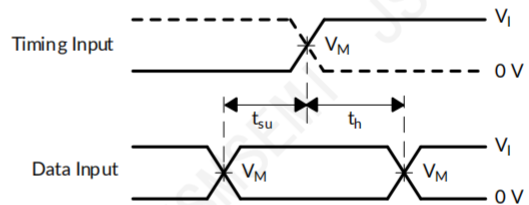
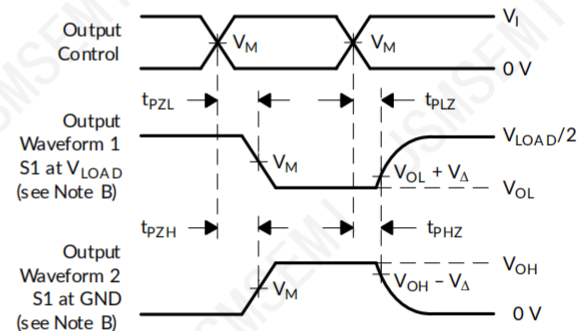
(1) All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation.

(2) This parameter is ensured by design and/or characterization and is not tested in production.

(3) Typical values represent the most likely parametric norm as determined at the time of characterization. Actual typical values may vary over time and will also depend on the application and configuration.

Parameter Measurement Information


V_{CC}	INPUTS		V_M	V_{LOAD}	C_L	R_L	V_{Δ}
	V_I	t_r/t_f					
$2.0V \pm 0.2V$	V_{CC}	$\leq 2ns$	$V_{CC}/2$	$2 \times V_{CC}$	30pF	500Ω	0.15V
$3.3V \pm 0.3V$	3V	$\leq 2.5ns$	1.5V	6V	50pF	500Ω	0.3V
$5V \pm 0.5V$	V_{CC}	$\leq 2.5ns$	$V_{CC}/2$	$2 \times V_{CC}$	50pF	500Ω	0.3V


**VOLTAGE WAVEFORMS
PULSE DURATION**

**VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
INVERTING AND NONINVERTING OUTPUTS**

**VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES**

**VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING**
NOTES:

- CL includes probe and jig capacitance.
- Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control.
Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
- All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, ZO = 50Ω.
- The outputs are measured one at a time, with one transition per measurement.
- tPLZ and tPHZ are the same as tdis.
- tPZL and tPZH are the same as ten.
- tPLH and tPHL are the same as tpd.
- All parameters and waveforms are not applicable to all devices.

Figure1. Load Circuit and Voltage Waveforms

Detailed Description

Overview

The 74AHCT1G14 contains a single inverter gate. The device performs the Boolean function $Y = \bar{A}$.

The device functions as an independent inverter gate, but because of the Schmitt action, gates may have different input threshold levels for positive- (V_{T+}) and negative-going (V_{T-}) signals.

Functional Block Diagram



Device Functional Modes

INPUTS ⁽¹⁾	OUTPUT ⁽²⁾
A	Y
H	L
L	H

(1) H = High Voltage Level, L = Low Voltage Level, X = Don't Care

(2) H = Driving High, L = Driving Low, Z = High Impedance State

Application Information

In this application, three 2-input AND gates are combined to produce a 4-input AND gate function as shown in Typical Application Block Diagram. The fourth gate can be used for another application in the system, or the inputs can be grounded and the channel left unused.

The 74AHCT1G14 is used to directly control the $\overline{\text{RESET}}$ pin of a motor controller. The controller requires four input signals to all be HIGH before being enabled, and should be disabled in the event that any one signal goes LOW. The 4-input AND gate function combines the four individual reset signals into a single active-low reset signal.

Typical Application

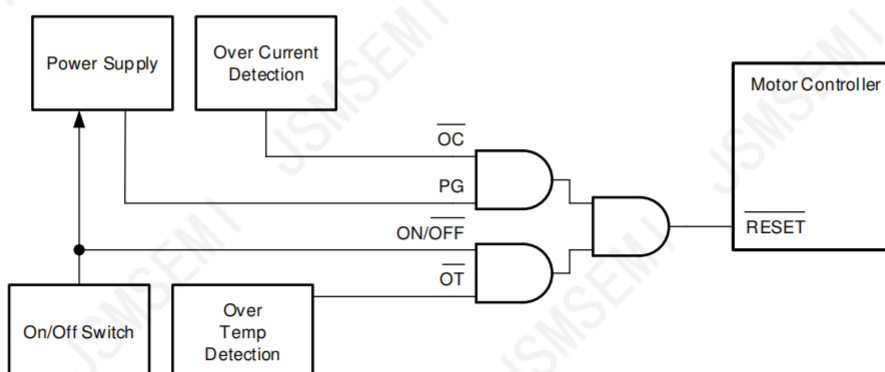


Figure 2. Typical Application Block Diagram

Design Requirements

Power Considerations

Ensure the desired supply voltage is within the range specified in the *Recommended Operating Conditions*. The supply voltage sets the electrical characteristics of the device as described in the *Electrical Characteristics* section.

The positive voltage supply must be capable of sourcing current equal to the maximum static supply current, I_{CC} , listed in the *Electrical Characteristics*, and any transient current required for switching.

The ground must be capable of sinking current equal to the total current to be sunk by all outputs of the 74AHCT1G14 plus the maximum supply current, I_{CC} , listed in the *Electrical Characteristics*, and any transient current required for switching. The logic device can only sink as much current that can be sunk into its ground connection. Be sure to not exceed the maximum total current through GND listed in the *Absolute Maximum Ratings*.

The 74AHCT1G14 can drive a load with a total capacitance less than or equal to 50 pF while still meeting all of the data sheet specifications. Larger capacitive loads can be applied; however, it is not recommended to exceed 50 pF.

The 74AHCT1G14 can drive a load with total resistance described by $R_L \geq V_O / I_O$, with the output voltage and current defined in the *Electrical Characteristics* table with V_{OL} . When outputting in the HIGH state, the output voltage in the equation is defined as the difference between the measured output voltage and the supply voltage at the V_{CC} pin.

Total power consumption can be calculated using the information provided in the CMOS Power Consumption and Cpd Calculation application note.

Thermal increase can be calculated using the information provided in the Thermal Characteristics of Standard Linear and Logic (SLL) Packages and Devices application note.

Input Considerations

Input signals must cross to be considered a logic LOW, and to be considered a logic HIGH. Do not exceed the maximum input voltage range found in the *Absolute Maximum Ratings*.

Unused inputs must be terminated to either V_{CC} or ground. The unused inputs can be directly terminated if the input is completely unused, or they can be connected with a pull-up or pull-down resistor if the input will be used sometimes, but not always. A pull-up resistor is used for a default state of HIGH, and a pull-down resistor is used for a default state of LOW. The drive current of the controller, leakage current into the 74AHCT1G14 (as specified in the *Electrical Characteristics*), and the desired input transition rate limits the resistor size. A 10-k Ω resistor value is often used due to these factors.

Refer to the *Feature Description* section for additional information regarding the inputs for this device.

Output Considerations

The ground voltage is used to produce the output LOW voltage. Sinking current into the output will increase the output voltage as specified by the V_{OL} specification in the *Electrical Characteristics*.

Unused outputs can be left floating. Do not connect outputs directly to V_{CC} or ground.

Refer to the *Feature Description* section for additional information regarding the outputs for this device.

Power Supply Recommendations

The power supply can be any voltage between the minimum and maximum supply voltage rating located in *Recommended Operating Conditions*.

Each V_{CC} pin must have a good bypass capacitor to prevent power disturbance. Recommends a 0.1 μ F capacitor for devices with a single supply; and a 0.01 μ F or 0.022 μ F capacitor for each power pin if there are multiple V_{CC} pins. It is ok to parallel multiple bypass capacitors to reject different frequencies of noise. 0.1 μ F and 1 μ F capacitors are commonly used in parallel. The bypass capacitor must be installed as close to the power pin as possible for best results.

Layout

Layout Guidelines

When using multiple bit logic devices inputs must not ever float. In many cases, functions or parts of functions of digital logic devices are unused; for example, when only two inputs of a triple-input AND gate are used or only 3 of the 4 buffer gates are used. Such input pins must not be left unconnected because the undefined voltages at the outside connections result in undefined operational states. Observe the following rules under all circumstances.

- All unused inputs of digital logic devices must be connected to a high or low bias to prevent them from floating.
- The logic level that must be applied to any particular unused input depends on the function of the device. Generally they will be tied to GND or V_{CC} , whichever make more sense or is more convenient.

Layout Example

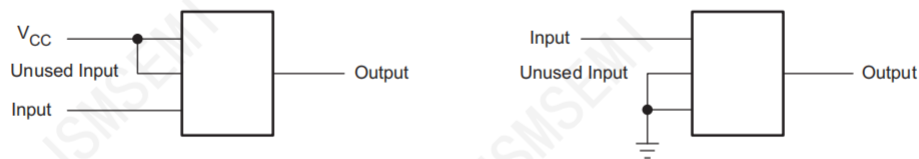
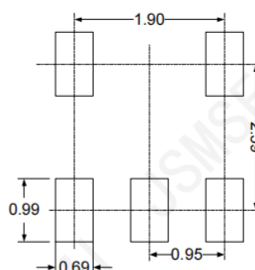
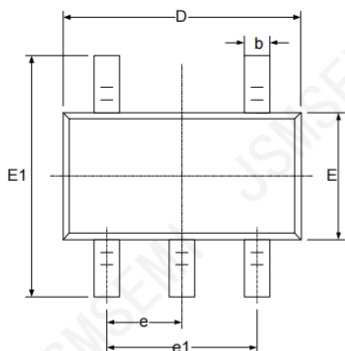


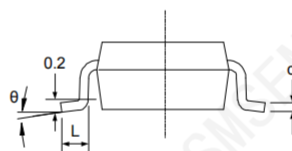
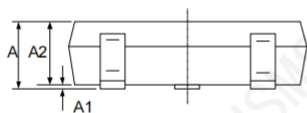
Figure 3 .Layout Diagram

Package Information

SOT-23-5L



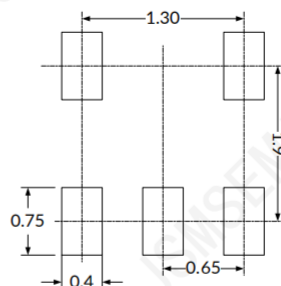
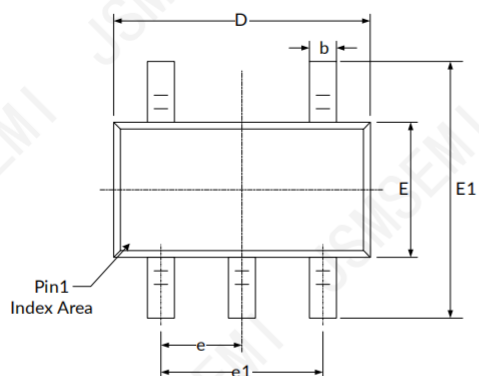
RECOMMENDED LAND PATTERN (Unit: mm)



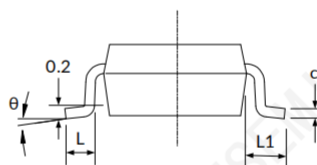
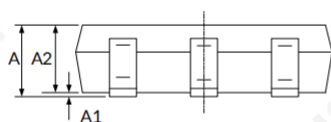
Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	1.050	1.250	0.041	0.049
A1	0.000	0.100	0.000	0.004
A2	1.050	1.150	0.041	0.045
b	0.300	0.500	0.012	0.020
c	0.100	0.200	0.004	0.008
D	2.820	3.020	0.111	0.119
E	1.500	1.700	0.059	0.067
E1	2.650	2.950	0.104	0.116
e	0.950(BSC)		0.037(BSC)	
e1	1.800	2.000	0.071	0.079
L	0.300	0.600	0.012	0.024
θ	0°	8°	0°	8°

Package Information

SOT-353(SC70-5)



RECOMMENDED LAND PATTERN (Unit: mm)



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	0.900	1.100	0.035	0.043
A1	0.000	0.100	0.000	0.004
A2	0.900	1.000	0.035	0.039
b	0.150	0.350	0.006	0.014
c	0.080	0.150	0.003	0.006
D ⁽¹⁾	2.000	2.200	0.079	0.087
E ⁽¹⁾	1.150	1.350	0.045	0.053
E1	2.150	2.450	0.085	0.096
e	0.650(BSC)		0.026(BSC)	
e1	1.300(BSC)		0.051(BSC)	
L	0.260	0.460	0.010	0.018
L1	0.525		0.021	
θ	0°	8°	0°	8°

Revision History

Rev.	Change	Date
V1.0	Initial version	3/17/2023

Important Notice

JSMSEMI Semiconductor (JSMSEMI) PRODUCTS ARE NEITHER DESIGNED NOR INTENDED FOR USE IN MILITARY AND/OR AEROSPACE, AUTOMOTIVE OR MEDICAL DEVICES OR SYSTEMS UNLESS THE SPECIFIC JSMSEMI PRODUCTS ARE SPECIFICALLY DESIGNATED BY JSMSEMI FOR SUCH USE. BUYERS ACKNOWLEDGE AND AGREE THAT ANY SUCH USE OF JSMSEMI PRODUCTS WHICH JSMSEMI HAS NOT DESIGNATED FOR USE IN MILITARY AND/OR AEROSPACE, AUTOMOTIVE OR MEDICAL DEVICES OR SYSTEMS IS SOLELY AT THE BUYER' S RISK.

JSMSEMI assumes no liability for application assistance or customer product design. Customers are responsible for their products and applications using JSMSEMI products.

Resale of JSMSEMI products or services with statements diferent from or beyond the parameters stated by JSMSEMI for that product or service voids all express and any implied warranties for the associated JSMSEMI product or s ervice. JSMSEMI is not responsible or liable for any such statements.

JSMSEMI All Rights Reserved. Information and data in this document are owned by JSMSEMI wholly and may not be edited, reproduced, or redistributed in any way without the express written consent from JSMSEMI.

Any and all information described or contained herein are subject to change without notice due to product/technology improvement, etc. When designing equipment, refer to the "Delivery Specification" for the JSMSEMI product that you intend to use.

For additional information please contact Kevin@jsmsemi.com or visit www.jsmsemi.com