



# MPQ7210

## 60V, 2A, Synchronous, Dual-Buck LED Driver with SPI, AEC-Q100 Qualified

### DESCRIPTION

The MPQ7210 is a synchronous, dual-buck LED driver designed to operate as a constant current source to drive 2 independent LED channels. Each channel can support up to 2A of output current ( $I_{OUT}$ ), and they can also be connected in parallel to support up to 4A of current.

The 4.5V to 60V input voltage ( $V_{IN}$ ) range allows a string of up to 12 LEDs to be connected in series per channel. When paired with a matrix manager, the MPQ7210 can achieve an ideal architecture to drive adaptive driving beams or matrix headlights.

The safety protection suite includes a fault (/FS) pin used to report over-current protection (OCP), under-voltage lockout (UVLO), early thermal warning, and thermal shutdown. These features can be used to assist the system in meeting functional safety requirements.

An integrated 10-bit analog-to-digital converter (ADC) monitors  $V_{IN}$ , the output voltage ( $V_{OUT}$ ), VCC voltage ( $V_{CC}$ ), and junction temperature ( $T_J$ ), and logs the data into the internal registers. These diagnostics can be read back by a microcontroller (MCU) through the serial peripheral interface (SPI). The SPI can also be used to preset dimming profiles within the registers and mask undesired signals on the fault (/FS) pin.

The MPQ7210 minimizes the need for a number of external components and is available in a QFN-26 (5mmx5mm) package. It is available in AEC-Q100 Grade 1.

### FEATURES

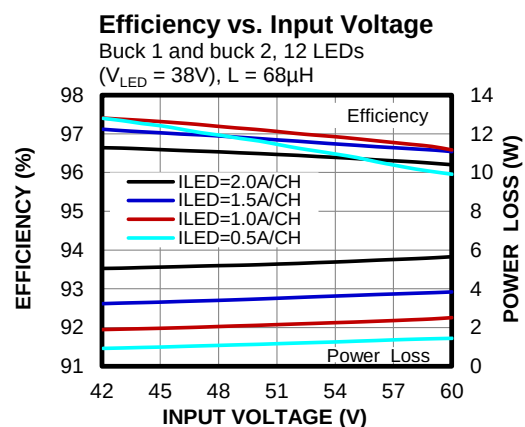
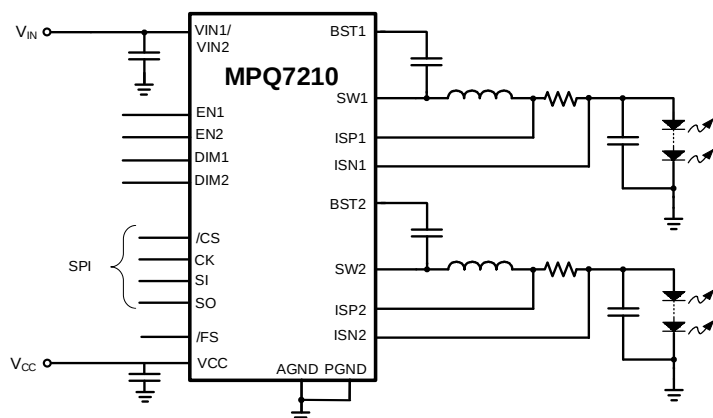
- Built for Automotive LED Applications
  - Wide 4.5V to 60V Input Voltage ( $V_{IN}$ ) Range
  - 2A Dual-Channel Buck
  - 4A Single-Channel Buck
  - $\pm 3\%$  LED Current Accuracy
  - Operating Junction Temperature ( $T_J$ ) from  $-40^{\circ}\text{C}$  to  $+150^{\circ}\text{C}$
  - 8-Bit Analog Dimming
  - 12-Bit PWM Dimming
- Optimized for EMC/EMI
  - Selectable 220kHz, 420kHz, 1.1MHz, and 2.3MHz Switching Frequency ( $f_{SW}$ )
  - Frequency Spread Spectrum (FSS)
  - CISPR25 Class 5 Compliant
  - Safety
- Safety Protection Suites
  - Analog-to-Digital Converter (ADC) to Monitor the  $V_{IN}$ , Output Voltage ( $V_{OUT}$ ), VCC Voltage ( $V_{CC}$ ), and  $T_J$
  - Failsafe (/FS) Pin and Registers
  - Output Under-Voltage Protection (UVP)
  - Over-Current Protection (OCP)
  - Early Thermal Warning
  - Thermal Shutdown
  - Serial Peripheral Interface (SPI) with Configurable Features
  - Current Limit
- Additional Features
  - Multi-Page One-Time Programmable (OTP) Memory
  - Available in a QFN-26 (5mmx5mm) Package with Wettable Flanks
  - Available in AEC-Q100 Grade 1

### APPLICATIONS

- Adaptive Driving Beam Headlights
- Matrix Headlights
- Daytime Running Lights (DRLs)
- Side Markers

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## TYPICAL APPLICATION



## ORDERING INFORMATION

| Part Number*                  | Package          | Top Marking | MSL Rating** |
|-------------------------------|------------------|-------------|--------------|
| MPQ7210GUE-xxxx-AEC1***, **** | QFN-26 (5mmx5mm) | See Below   | 2            |

\* For Tape & Reel, add suffix -Z (e.g. MPQ7210GUE-xxxx-AEC1-Z).

\*\* Moisture Sensitivity Level Rating

\*\*\* “xxxx” is the configuration code identifier for the register settings stored in the OTP register. Each “x” can be a hexadecimal value between 0 and F. The default code is “0000”. Contact an MPS FAE to create this unique number.

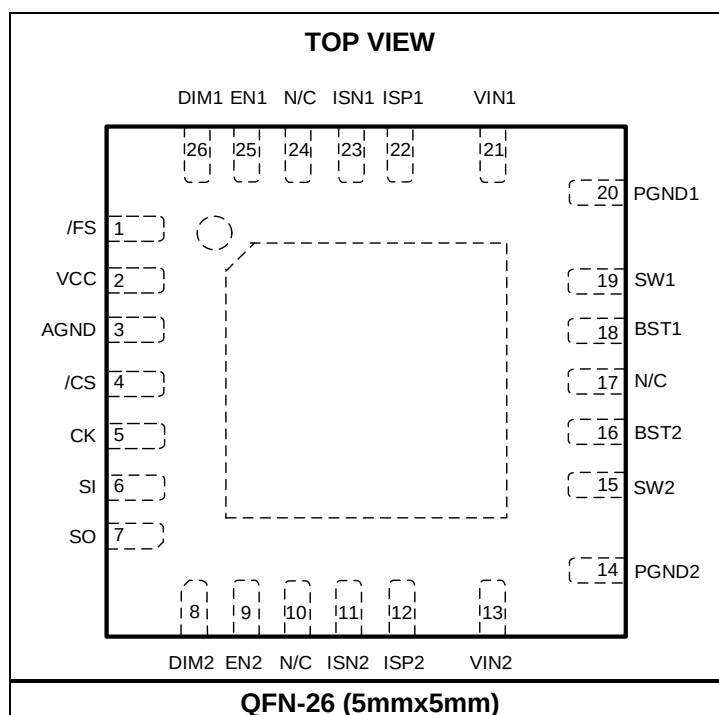
\*\*\*\* Wettable flank

## TOP MARKING

**MPSYYWW**  
**MP7210**  
**LLLLLLL**  
**E**

MPS: MPS prefix  
YY: Year code  
WW: Week code  
MP7210: Part number  
LLLLLLL: Lot number  
E: Wettable Flank

## PACKAGE REFERENCE



## PIN FUNCTIONS

| Pin #         | Name            | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                    |
|---------------|-----------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 1             | /FS             | <b>/FS indicator.</b> The /FS pin is an open-drain output that is active low. Pull /FS to VCC through a resistor. /FS pulls low when over-current protection (OCP), output under-voltage protection (UVP), thermal warning (TW), or thermal shutdown (TSD) occur. If EN1 and EN2 pull low at the same time, or V <sub>CC</sub> or V <sub>IN</sub> under-voltage lockout (UVLO) occurs, the /FS pin de-asserts and returns to normal. The microcontroller (MCU) can write to register 0x0A to clear /FS error flags.                                                                                            |
| 2             | VCC             | <b>Internal bias supply.</b> The VCC pin supplies power to the internal circuit. Place a ≥4.7μF decoupling capacitor from VCC to ground, and close to VCC. There is no internal VCC regulator from VIN. VCC can only be powered from an external 5V source.                                                                                                                                                                                                                                                                                                                                                    |
| 3             | AGND            | <b>Analog ground.</b> The AGND pin is the reference ground of the internal logic circuit.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                      |
| 4             | /CS             | <b>SPI chip selection input.</b> Connect the /CS pin to the master CS.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                         |
| 5             | CK              | <b>SPI clock input.</b> Connect the CK pin to the master CK.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                   |
| 6             | SI              | <b>SPI data input.</b> Connect the SI pin to the master MOSI.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                  |
| 7             | SO              | <b>SPI data output.</b> Connect the SO pin to the master MISO.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                 |
| 8, 26         | DIM2,<br>DIM1   | <b>Dimming control.</b> In PWM dimming mode 1, pull this pin high for X% dimming duty, and pull this pin low for 0%, dimming duty (where X% can be set from 0% to 100% via the SPI with a register change). In PWM dimming mode 2, the LED current follows the DIM pin. Apply a 100Hz to 2kHz external clock to the DIM pin for PWM dimming. In dimming mode 3, pull this pin high for a 100% dimming duty cycle, and pull this pin low for X% dimming duty (where X% can be set from 0% to 100% by the internal register). For more details, see the Pulse-Width Modulation (PWM) Dimming section on page 27. |
| 9, 25         | EN2,<br>EN1     | <b>Enable control.</b> Pull the EN1 and EN2 pin high to enable the part; pull EN1 and EN2 low to shut down the part.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                           |
| 10, 17,<br>24 | N/C             | <b>No connection.</b>                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                          |
| 11, 23        | ISN2,<br>ISN1   | <b>Negative current-sense input.</b> Connect the ISN2 and ISN1 pin to the negative terminals of the current feedback resistors.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                |
| 12, 22        | ISP2,<br>ISP1   | <b>Positive current-sense input.</b> Connect the ISP2 and ISP1 pin to the positive terminals of the current feedback resistors. This pin is also used as the sensing signal for the output voltage (V <sub>OUT</sub> ).                                                                                                                                                                                                                                                                                                                                                                                        |
| 13, 21        | VIN2,<br>VIN1   | <b>Input supply.</b> The MPQ7210 operates from a 4.5V to 60V input rail. Use an input capacitor (C <sub>IN</sub> ) to decouple the input rail. VIN1 and VIN2 are independent. Make the VINx connections with a wide PCB trace.                                                                                                                                                                                                                                                                                                                                                                                 |
| 14, 20        | PGND2,<br>PGND1 | <b>Power ground.</b> The PGND pin is the reference ground of the power device and requires careful consideration during PCB layout. It is typically used to dissipate the thermal heat.                                                                                                                                                                                                                                                                                                                                                                                                                        |
| 15, 19        | SW2,<br>SW1     | <b>Switch node.</b> The SW2 and SW1 pin is the middle point of the high-side and low-side MOSFET (HS-FET and LS-FET, respectively). To reduce the noise coupling and improve EMI, it is recommended to make a wide SW trace and minimize the SW node's size.                                                                                                                                                                                                                                                                                                                                                   |
| 16, 18        | BST2,<br>BST1   | <b>Bootstrap.</b> The BST2 and BST1 pin typically requires a 0.1μF capacitor connected between the SWx and BSTx pins to form a floating supply across the HS-FET driver. A resistor can be placed between SWx and BSTx to reduce the SW voltage spike and improve EMI performance.                                                                                                                                                                                                                                                                                                                             |
| -             | EP              | <b>Exposure thermal pad.</b> The exposed pad has no internal electrical connection to GND. Connect the exposed pad to the external GND plane on the board for optimal thermal performance.                                                                                                                                                                                                                                                                                                                                                                                                                     |

## ABSOLUTE MAXIMUM RATINGS <sup>(1)</sup>

|                                                                                    |                                          |
|------------------------------------------------------------------------------------|------------------------------------------|
| $V_{INX} - V_{PGND/AGND}$ .....                                                    | -0.3V to +65V                            |
| $V_{SWX} - V_{PGND/AGND}$ .....                                                    | .....                                    |
| .....                                                                              | -0.3V to $V_{IN} - V_{PGND/AGND} + 0.3V$ |
| $V_{BSTX}$ .....                                                                   | $V_{SW} + 5.5V$                          |
| $V_{ISPX} - V_{PGND/AGND}$ .....                                                   | -0.3V to +60V                            |
| $V_{ISNX} - V_{PGND/AGND}$ .....                                                   | -0.3V to +60V                            |
| $V_{ISPX} - V_{ISNX}$ .....                                                        | -0.3V to +0.3V                           |
| All other pins - $V_{PGND/AGND}$ .....                                             | -0.3V to +5.5V                           |
| Continuous power dissipation ( $T_A = 25^{\circ}C$ ) <sup>(2)</sup> <sup>(6)</sup> |                                          |
| QFN-26 (5mmx5mm) .....                                                             | 4.48W                                    |
| Junction temperature ( $T_J$ ) .....                                               | 150°C                                    |
| Lead temperature .....                                                             | 260°C                                    |
| Storage temperature .....                                                          | -65°C to +150°C                          |

## ESD Ratings

|                                  |                          |
|----------------------------------|--------------------------|
| Human body model (HBM) .....     | Class 2 <sup>(3)</sup>   |
| Charged-device model (CDM) ..... | Class C2b <sup>(4)</sup> |

## Recommended Operating Conditions

|                                                |                 |
|------------------------------------------------|-----------------|
| Supply voltage ( $V_{IN} - V_{PGND}$ ) .....   | 4.5V to 60V     |
| Supply voltage ( $V_{CC} - V_{PGND}$ ) .....   | 4.5V to 5.5V    |
| LED current ( $I_{LED}$ ) (dual-channel) ..... | Up to 2A        |
| $I_{LED}$ (single-channel) .....               | Up to 4A        |
| Operating junction temp ( $T_J$ ) ....         | -40°C to +150°C |

## Thermal Resistance $\theta_{JA}$ $\theta_{JC}$

|                    |           |                             |
|--------------------|-----------|-----------------------------|
| QFN-26 (5mmx5mm)   |           |                             |
| JESD51-7 .....     | 35.5..... | 4.8.....°C/W <sup>(5)</sup> |
| EVQ7210-U-00A..... | 27.9..... | 2.7.....°C/W <sup>(6)</sup> |

### Notes:

- 1) Absolute maximum ratings are rated under room temperature, unless otherwise noted. Exceeding these ratings may damage the device.
- 2) The maximum allowable power dissipation is a function of the maximum junction temperature,  $T_J$  (MAX), the junction-to-ambient thermal resistance,  $\theta_{JA}$ , and the ambient temperature,  $T_A$ . The maximum allowable continuous power dissipation at any ambient temperature is calculated by  $P_D$  (MAX) =  $(T_J$  (MAX) -  $T_A$ ) /  $\theta_{JA}$ . Exceeding the maximum allowable power dissipation can produce an excessive die temperature, and the regulator may go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
- 3) Per AEC-Q100-002.
- 4) Per AEC-Q100-011.
- 5) Measured on a JESD51-5/7, 4-layer PCB, where there is a thermal via array under the exposed pad. The values given in this table are only valid for comparison with other packages and cannot be used for design purposes. These values were calculated in accordance with JESD51-5/7, and simulated on a specified JEDEC board. They do not represent the performance obtained in an actual application. The value of  $\theta_{JC}$  shows the thermal resistance from the junction-to-case bottom.
- 6) Measured on a standard EVB for the MPQ7210, 83.5mmx83.5mm, 4-layer PCB, 2oz. The value of  $\theta_{JC}$  shows the thermal resistance from junction-to-case top.

## ELECTRICAL CHARACTERISTICS

$V_{IN} = 12V$ ,  $V_{EN} = 3.3V$ ,  $T_J = -40^{\circ}C$  to  $+150^{\circ}C$ , typical values are at  $T_J = 25^{\circ}C$ , unless otherwise noted.

| Parameter                                                                | Symbol            | Condition                                                       | Min | Typ        | Max  | Units      |
|--------------------------------------------------------------------------|-------------------|-----------------------------------------------------------------|-----|------------|------|------------|
| <b>Input Supply</b>                                                      |                   |                                                                 |     |            |      |            |
| VIN supply current (shutdown)                                            | $I_{SD}$          | $V_{ENx} = 0V$ , $V_{DIMx} = 0V$ , $V_{CC} = 5V$                |     | 1          | 8.5  | $\mu A$    |
| VIN supply current (standby)                                             | $I_{STD}$         | $V_{ENx} = 3.3V$ , $V_{DIMx} = 0V$ , $V_{CC} = 5V$              |     | 32         | 80   | $\mu A$    |
| Input voltage ( $V_{IN}$ ) under-voltage lockout (UVLO) rising threshold | $V_{INUVLO\_R}$   | $V_{IN} - V_{PGND}$                                             | 3.8 | 4.2        | 4.6  | V          |
| VIN UVLO falling threshold                                               | $V_{INUVLO\_F}$   | $V_{IN} - V_{PGND}$                                             | 3.6 | 4          | 4.4  | V          |
| VIN UVLO threshold hysteresis                                            | $V_{INUVLO\_H}$   | $V_{IN} - V_{PGND}$                                             |     | 0.2        |      | V          |
| <b>VCC Supply</b>                                                        |                   |                                                                 |     |            |      |            |
| VCC supply current (shutdown)                                            | $I_{VCC(SD)}$     | $V_{ENx} = 0V$ , $V_{DIMx} = 0V$ , $V_{CC} = 5V$                |     | 3.2        | 50   | $\mu A$    |
| VCC supply current (standby)                                             | $I_{VCC(STD)}$    | $V_{ENx} = 3.3V$ , $V_{DIMx} = 0V$ , $V_{CC} = 5V$              |     | 2          | 3.5  | mA         |
| VCC supply current (switching)                                           | $I_{VCC(SW)}$     | $V_{ENx} = V_{DIMx} = 3.3V$ , $V_{CC} = 5V$ , $f_{SW} = 420kHz$ |     | 3.5        |      | mA         |
| VCC voltage ( $V_{CC}$ ) UVLO rising threshold                           | $V_{CCUVLO\_R}$   | $V_{CC} - V_{AGND}$                                             | 3.8 | 4.2        | 4.6  | V          |
| VCC UVLO falling threshold                                               | $V_{CCUVLO\_F}$   | $V_{CC} - V_{AGND}$                                             | 3.6 | 4          | 4.4  | V          |
| VCC UVLO threshold hysteresis                                            | $V_{CCUVLO\_H}$   | $V_{CC} - V_{AGND}$                                             |     | 0.2        |      | V          |
| <b>Switch and Frequency</b>                                              |                   |                                                                 |     |            |      |            |
| High-side (HS) switch on resistance                                      | $R_{DS(ON)-HS}$   | $V_{BST-SW} = 5V$ , $I_{LED} = 1A$                              |     | 235        | 445  | m $\Omega$ |
| Low-side (LS) switch on resistance                                       | $R_{DS(ON)-LS}$   | $V_{CC} = 5V$ , $I_{LED} = 1A$                                  |     | 235        | 445  | m $\Omega$ |
| Switch leakage                                                           | $SW_{LKG}$        | $V_{ENx} = 0V$ , $V_{SW} = 12V$                                 |     |            | 5    | $\mu A$    |
| Peak current limit <sup>(7)</sup>                                        | $I_{LIMIT\_PEAK}$ | Register setting = 3.5A                                         | 2.5 | 3.5        | 4.5  | A          |
| Zero-current detection (ZCD) <sup>(7)</sup>                              | $I_{ZCD}$         | Zero-current detection                                          |     | 0          |      | mA         |
| Switching frequency                                                      | $f_{SW}$          | Register setting = 220kHz                                       | 180 | 220        | 320  | kHz        |
|                                                                          |                   | Register setting = 420kHz                                       | 360 | 420        | 470  | kHz        |
|                                                                          |                   | Register setting = 1.1MHz                                       | 0.8 | 1.1        | 1.35 | MHz        |
|                                                                          |                   | Register setting = 2.3MHz                                       | 2.0 | 2.3        | 2.6  | MHz        |
| Maximum duty cycle <sup>(7)</sup>                                        |                   |                                                                 | 93% | 95%        |      |            |
| Spread spectrum frequency <sup>(7)</sup>                                 |                   |                                                                 |     | 10         |      | kHz        |
| Spread spectrum frequency range <sup>(7)</sup>                           |                   |                                                                 |     | $\pm 10\%$ |      | $f_{SW}$   |
| Minimum on time <sup>(7)</sup>                                           | $t_{ON\_MIN}$     |                                                                 |     | 125        |      | ns         |
| Minimum off time <sup>(7)</sup>                                          | $t_{OFF\_MIN}$    |                                                                 |     | 120        |      | ns         |

## ELECTRICAL CHARACTERISTICS (continued)

$V_{IN} = 12V$ ,  $V_{EN} = 3.3V$ ,  $T_J = -40^{\circ}C$  to  $+150^{\circ}C$ , typical values are at  $T_J = 25^{\circ}C$ , unless otherwise noted.

| Parameter                                           | Symbol                | Condition                                                                  | Min   | Typ   | Max   | Units |
|-----------------------------------------------------|-----------------------|----------------------------------------------------------------------------|-------|-------|-------|-------|
| EN                                                  |                       |                                                                            |       |       |       |       |
| EN1/EN2 rising threshold                            | V <sub>EN_R</sub>     | V <sub>EN</sub> - V <sub>AGND</sub>                                        | 0.8   | 1.0   | 1.2   | V     |
| EN1/EN2 falling threshold                           | V <sub>EN_F</sub>     | V <sub>EN</sub> - V <sub>AGND</sub>                                        | 0.65  | 0.85  | 1.05  | V     |
| EN1/EN2 threshold hysteresis                        | V <sub>EN_H</sub>     | V <sub>EN</sub> - V <sub>AGND</sub>                                        |       | 150   |       | mV    |
| EN1/EN2 input current                               | I <sub>EN</sub>       | V <sub>EN</sub> - V <sub>AGND</sub> = 2V                                   |       | 2     | 5     | μA    |
|                                                     |                       | V <sub>EN</sub> - V <sub>AGND</sub> = 0V                                   |       | 0     | 0.2   | μA    |
| DIM                                                 |                       |                                                                            |       |       |       |       |
| DIM1/DIM2 high threshold                            | V <sub>DIM_R</sub>    | V <sub>DIM</sub> - V <sub>AGND</sub>                                       |       | 1.25  | 2     | V     |
| DIM1/DIM2 low threshold                             | V <sub>DIM_F</sub>    | V <sub>DIM</sub> - V <sub>AGND</sub>                                       | 0.8   | 1.15  |       | V     |
| DIM1/DIM2 input current                             | I <sub>DIM</sub>      | V <sub>DIM</sub> - V <sub>AGND</sub> = 2V                                  |       | 0     | 0.2   | μA    |
|                                                     |                       | V <sub>DIM</sub> - V <sub>AGND</sub> = 0V                                  |       | 0     | 0.2   | μA    |
| Current-Sense and Analog-to-Digital Converter (ADC) |                       |                                                                            |       |       |       |       |
| Current-sense accuracy                              | V <sub>SEN</sub>      | V <sub>ISP1</sub> = 48V, V <sub>ISN1</sub> = 47.8V, ANA_DIMx = 2'b11001000 | 194   | 200   | 206   | mV    |
|                                                     |                       | V <sub>ISP1</sub> = 5V, V <sub>ISN1</sub> = 4.8V, ANA_DIMx = 2'b11001000   | 194   | 200   | 206   | mV    |
| ADC full scale                                      |                       |                                                                            | 2     | 2.048 | 2.095 | V     |
| ADC resolution (10 bits) <sup>(7)</sup>             |                       |                                                                            |       | 2     |       | mV    |
| Analog dimming reference voltage                    | V <sub>REF</sub>      | Register = 100%                                                            | 1.188 | 1.203 | 1.217 | V     |
|                                                     |                       | Register = 50%                                                             | 0.592 | 0.6   | 0.608 | V     |
|                                                     |                       | Register = 5%                                                              | 56.7  | 60    | 63.3  | mV    |
| Output under-voltage threshold                      | V <sub>UV_TH</sub>    |                                                                            | 2.1   | 2.3   | 2.5   | V     |
| /FS Indicator                                       |                       |                                                                            |       |       |       |       |
| /FS assertion deglitch time after start-up          | t <sub>FS_TD</sub>    |                                                                            |       |       | 10    | μs    |
| /FS pull-down resistor                              |                       |                                                                            |       | 10    | 20    | Ω     |
| Thermal warning flag threshold <sup>(7)</sup>       | T <sub>WARN</sub>     |                                                                            | 105   | 125   | 145   | °C    |
| Thermal warning flag hysteresis <sup>(7)</sup>      | T <sub>WARN_HYS</sub> |                                                                            |       | 20    |       | °C    |
| Thermal shutdown threshold <sup>(7)</sup>           | T <sub>SD</sub>       |                                                                            | 155   | 170   | 185   | °C    |
| Thermal shutdown hysteresis <sup>(7)</sup>          | T <sub>SD_HYS</sub>   |                                                                            |       | 20    |       | °C    |

## SPI CHARACTERISTICS

$V_{IN} = 12V$ ,  $V_{EN} = 2V$ ,  $T_J = -40^{\circ}C$  to  $+150^{\circ}C$ , typical values are at  $T_J = 25^{\circ}C$ , unless otherwise noted.

| Parameters                                                              | Symbol           | Condition                                             | Min  | Typ | Max | Units   |
|-------------------------------------------------------------------------|------------------|-------------------------------------------------------|------|-----|-----|---------|
| <b>Serial Peripheral Interface (SPI) Timing Requirements</b>            |                  |                                                       |      |     |     |         |
| CK period <sup>(7)</sup>                                                | $t_{SPI}$        |                                                       |      |     | 250 | ns      |
| CK low time <sup>(7)</sup>                                              | $t_{CKL}$        |                                                       |      | 125 |     | ns      |
| CK high time <sup>(7)</sup>                                             | $t_{CKH}$        |                                                       |      | 125 |     | ns      |
| Time between the falling edge of /CS and SO output valid <sup>(7)</sup> | $t_{FSIV}$       | Falling: $SO < 0.4V$ , rising: $SO > 2V$              | 125  |     |     | ns      |
| Time between falling edge of CK and SO data valid <sup>(7)</sup>        | $t_{SOV}$        | Falling: $SO < 0.4V$ , rising: $SO > 2V$ , open drain |      |     | 60  |         |
| Set-up time of SI before the rising edge of CK <sup>(7)</sup>           | $t_{SIS}$        |                                                       | 30   |     |     | ns      |
| Hold time for SI after the rising edge of CK <sup>(7)</sup>             | $t_{SIH}$        |                                                       | 30   |     |     | ns      |
| Hold time of /CS after the last rising edge of CK <sup>(7)</sup>        | $t_{HCS}$        |                                                       | 62.5 |     |     | ns      |
| Delay between the rising edge of /CS and SO tri-state <sup>(7)</sup>    | $t_{SOTRI}$      |                                                       |      |     | 120 | ns      |
| Minimum time between two SPI commands <sup>(7)</sup>                    | $t_{MIN2SPI}$    |                                                       | 2    |     |     | $\mu s$ |
| High level input voltage                                                | $V_{I\_HIGH}$    | CS, CK, SI; $V_{IO} = 3.3V, 5V$                       | 2    |     |     | V       |
| Low level input voltage                                                 | $V_{I\_LOW}$     | CS, CK, SI; $V_{IO} = 3.3V, 5V$                       |      |     | 0.8 | V       |
| Input voltage hysteresis                                                | $V_{I\_HYS}$     | CS, CK, SI; $V_{IO} = 3.3V, 5V$                       |      | 130 |     | mV      |
| SO output high voltage                                                  | $V_{O\_HIGH}$    | $V_{CC} = 5V$                                         | 1.8  |     |     | V       |
| SO output low voltage                                                   | $V_{O\_LOW}$     | $V_{CC} = 5V$ , $I_{SO} = 10mA$                       |      |     | 0.6 | V       |
| SO capacitance <sup>(7)</sup>                                           | $C_{SO}$         | Pull-up resistor = 250 $\Omega$                       |      |     | 50  | pF      |
| Deglitch time for CK <sup>(7)</sup>                                     | $t_{CK\_FILTER}$ |                                                       | 50   |     | 85  | ns      |

### Notes:

7) Not tested in production. Guaranteed by design and characterization.

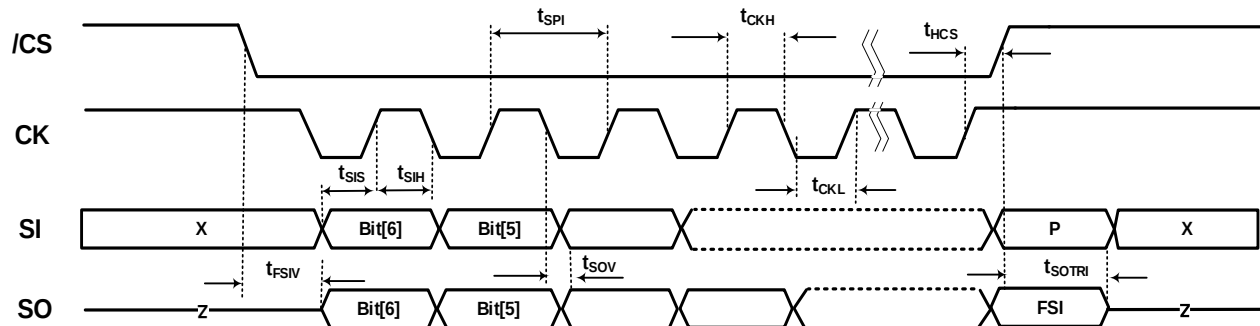
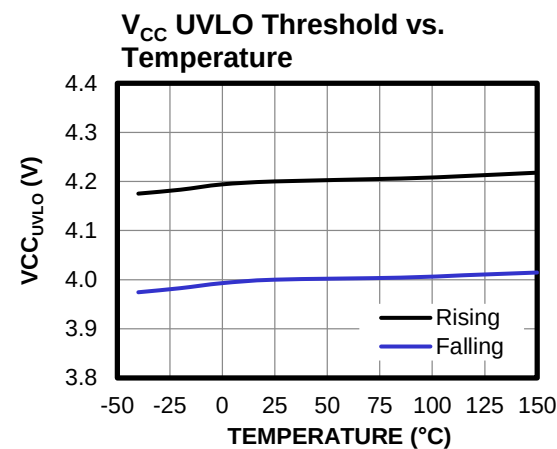
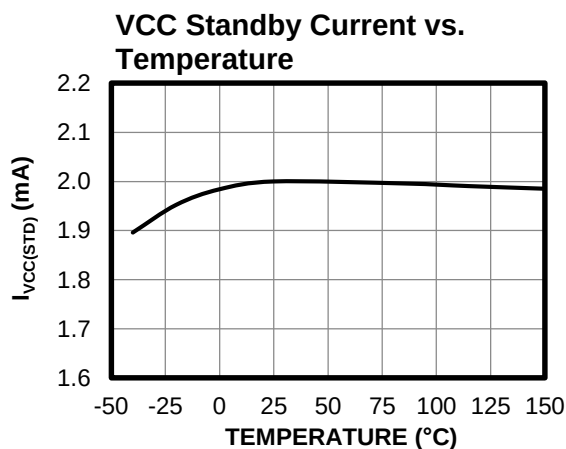
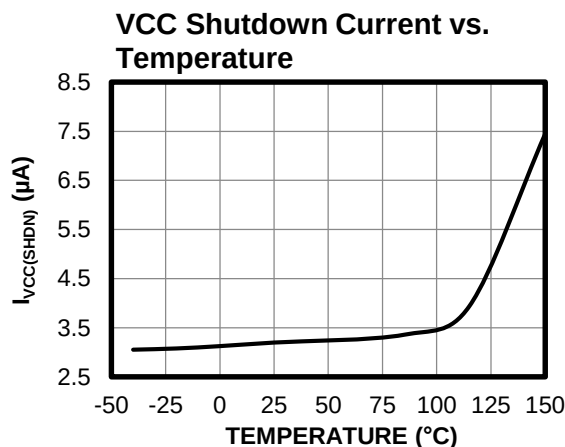
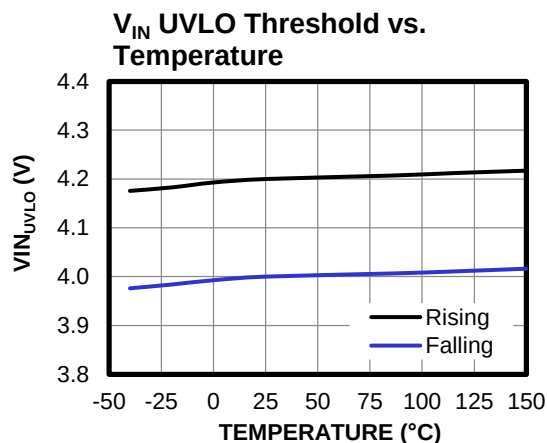
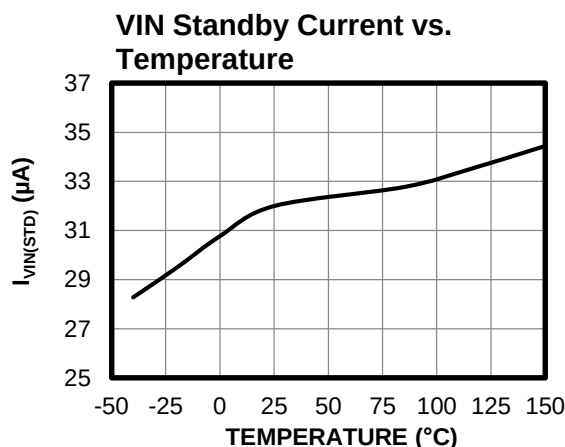
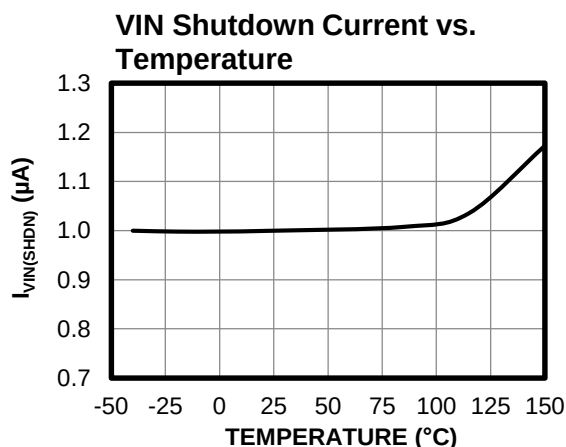


Figure 1: SPI Model 3

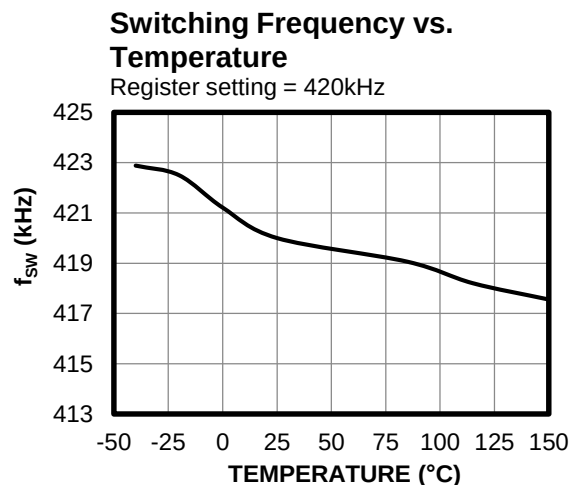
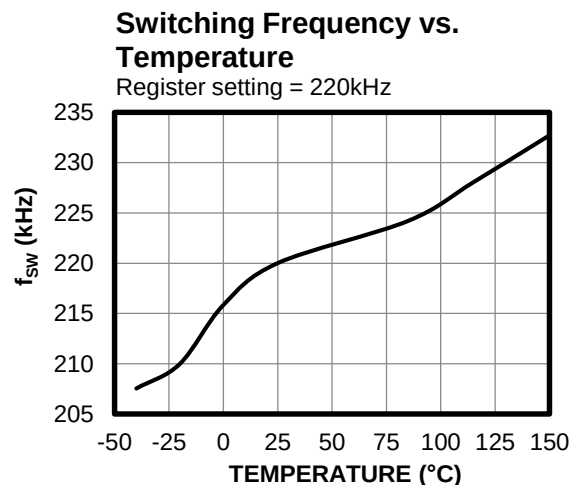
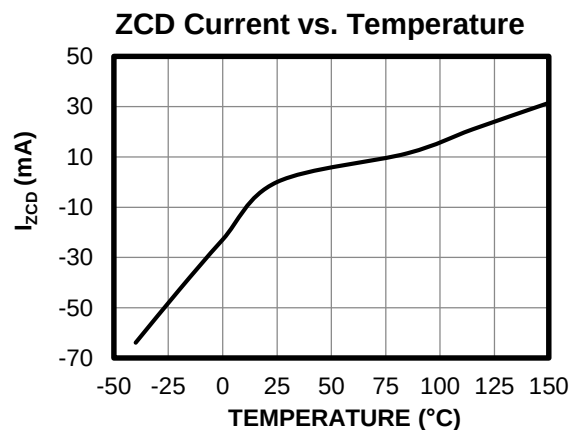
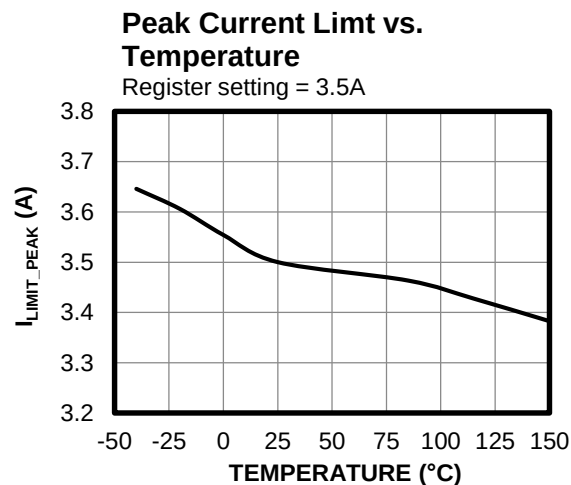
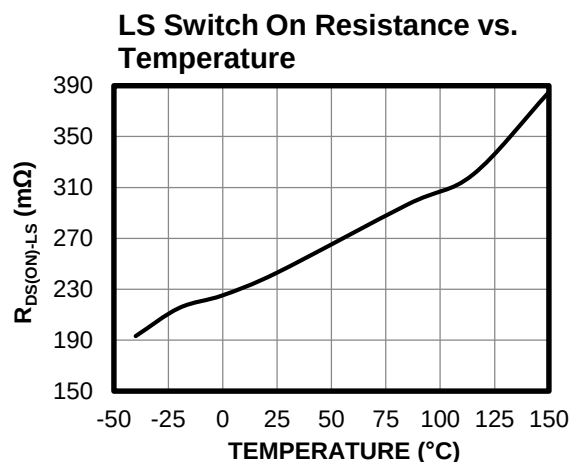
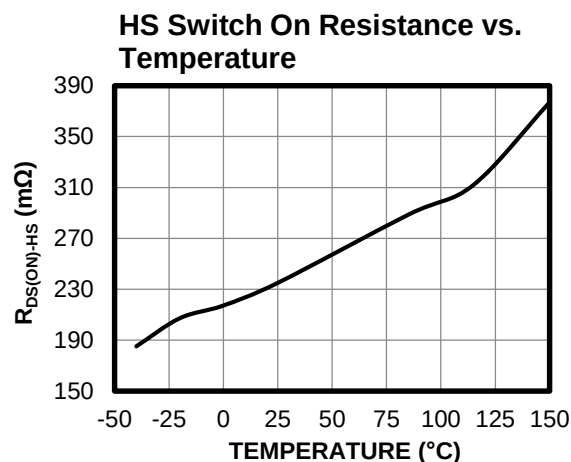
# TYPICAL CHARACTERISTICS

$V_{IN} = 12V$ ,  $T_J = -40^{\circ}C$  to  $+150^{\circ}C$ , unless otherwise noted.



# TYPICAL CHARACTERISTICS (continued)

$V_{IN} = 12V$ ,  $T_J = -40^{\circ}C$  to  $+150^{\circ}C$ , unless otherwise noted.

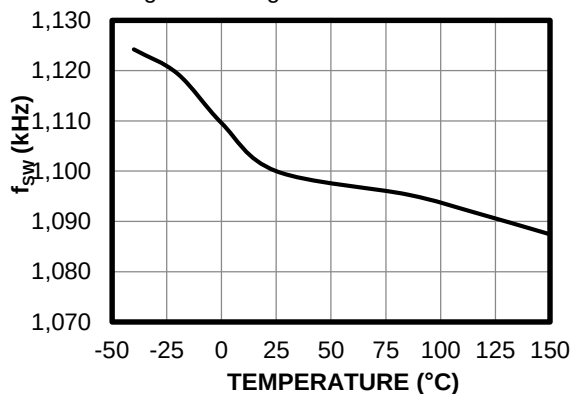


# TYPICAL CHARACTERISTICS (continued)

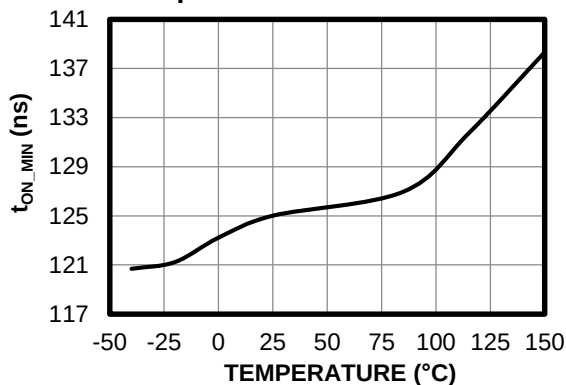
$V_{IN} = 12V$ ,  $T_J = -40^{\circ}C$  to  $+150^{\circ}C$ , unless otherwise noted.

**Switching Frequency vs. Temperature**

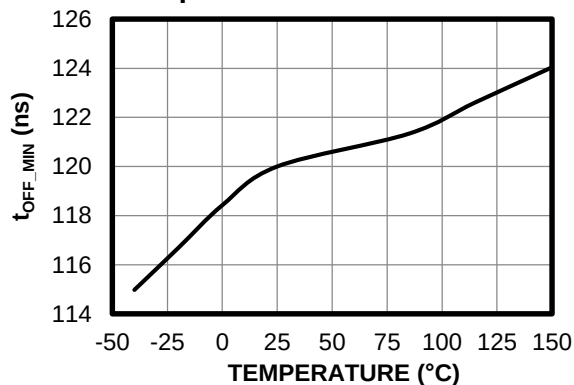
Register setting = 1100kHz



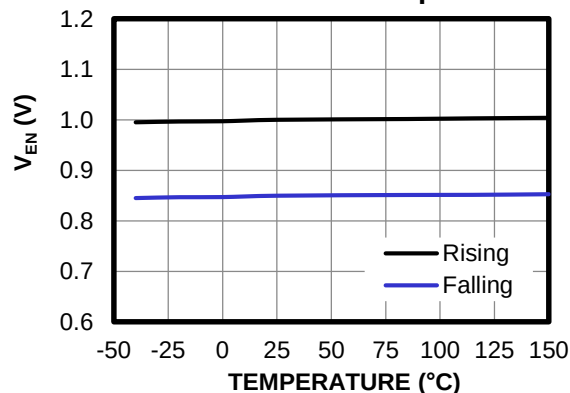
**Minimum On Time vs. Temperature**



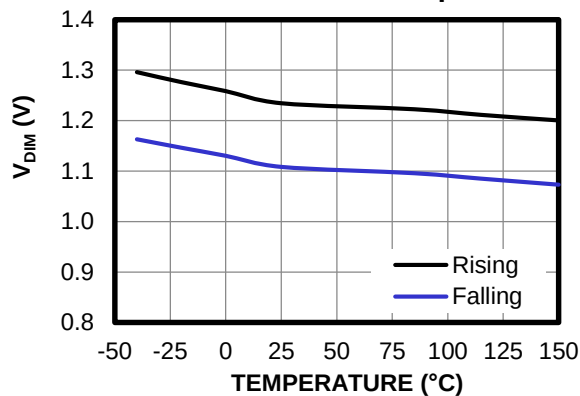
**Minimum Off Time vs. Temperature**



**EN Threshold vs. Temperature**

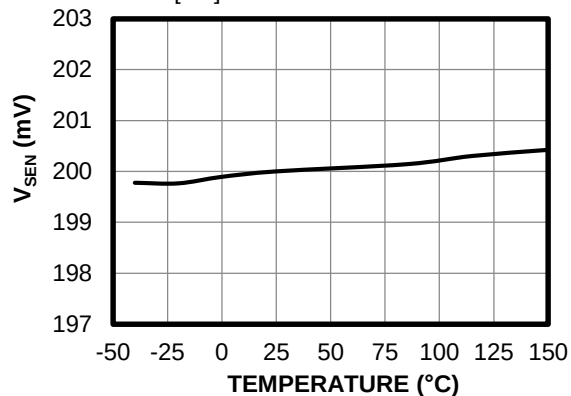


**DIM Threshold vs. Temperature**



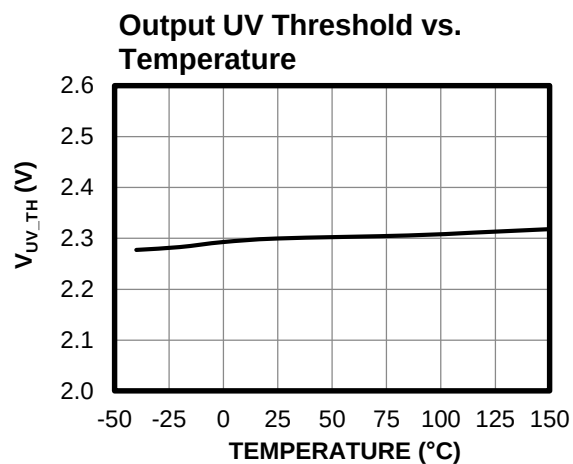
**Current-Sense Voltage vs. Temperature**

ADIM[7:0] = 0xC8



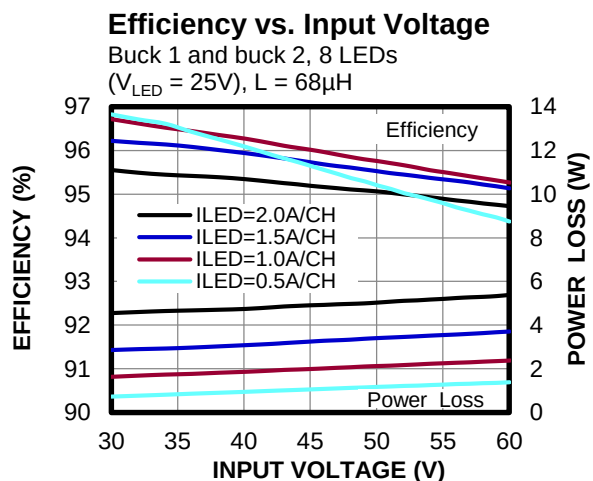
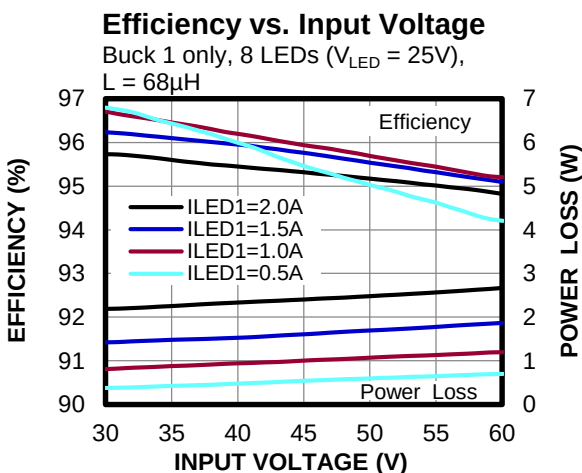
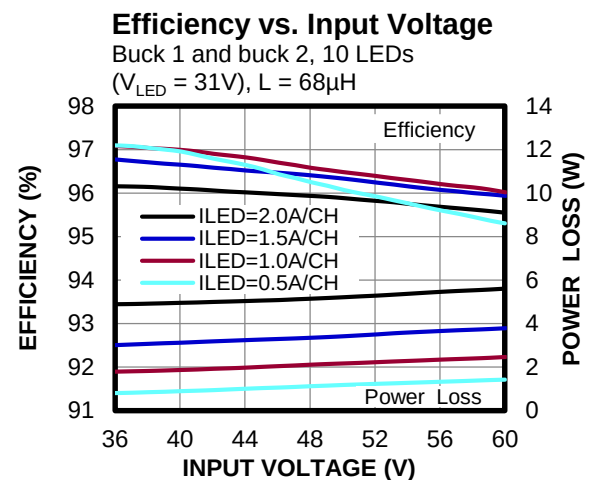
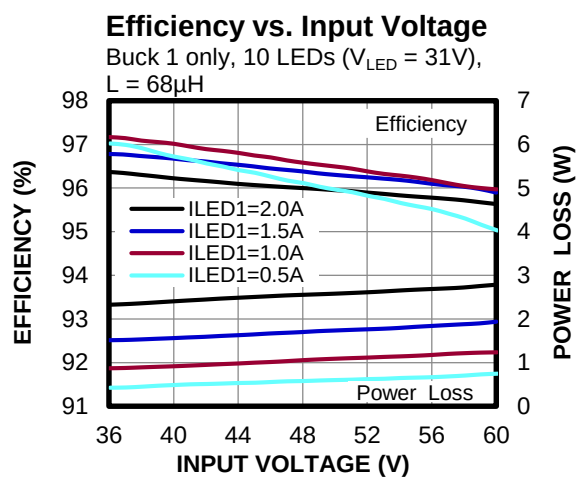
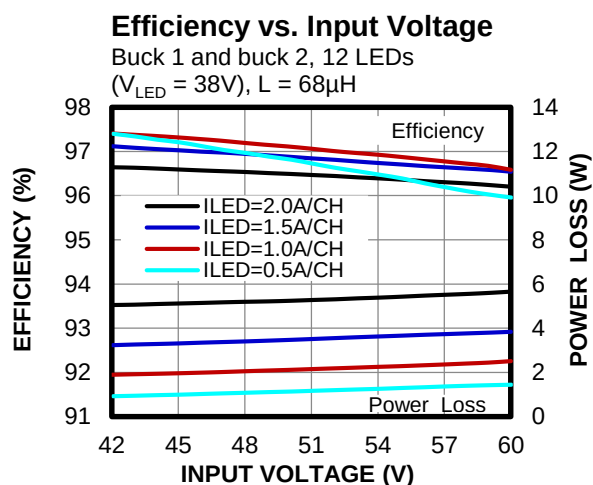
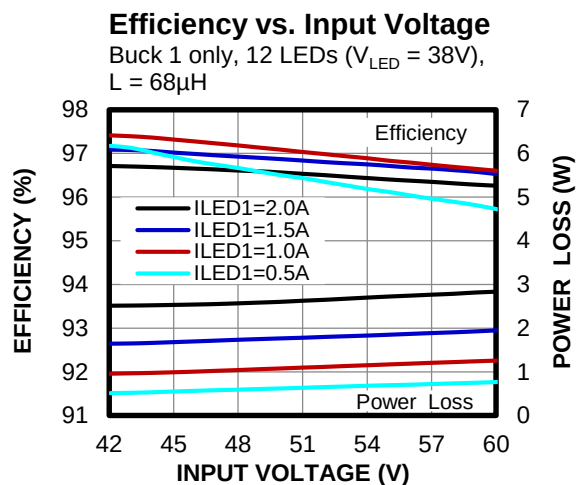
**TYPICAL CHARACTERISTICS** (*continued*)

$V_{IN} = 12V$ ,  $T_J = -40^{\circ}C$  to  $+150^{\circ}C$ , unless otherwise noted.



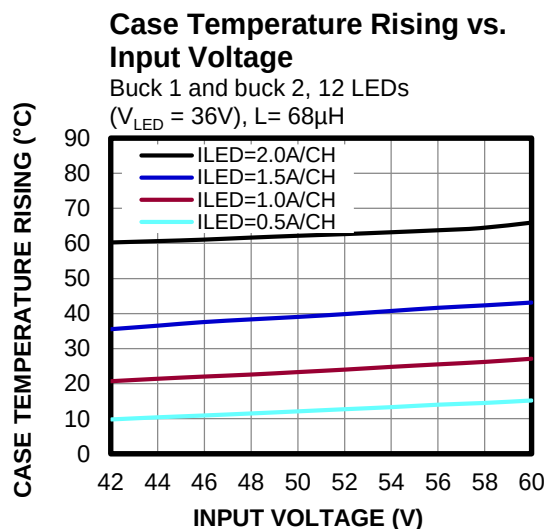
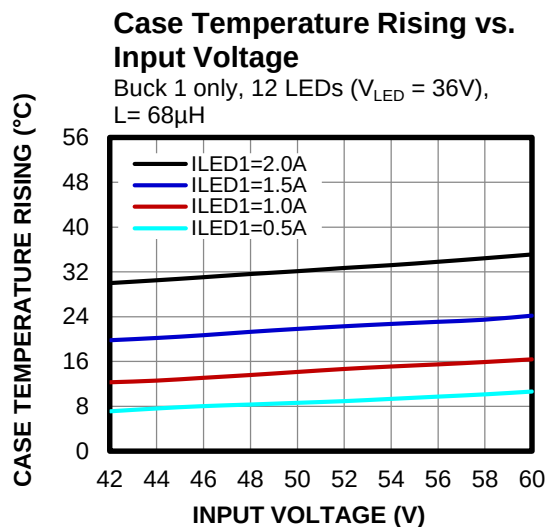
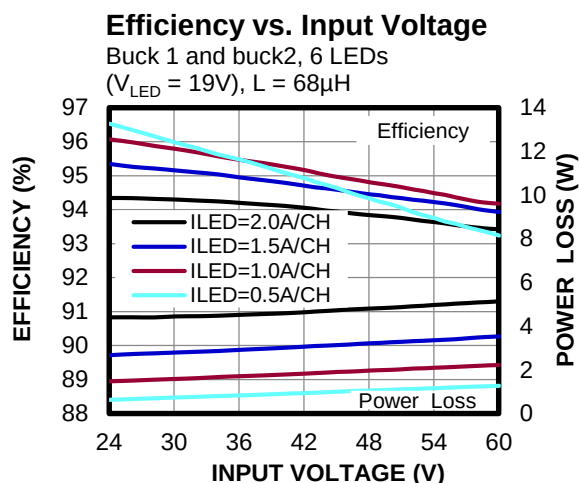
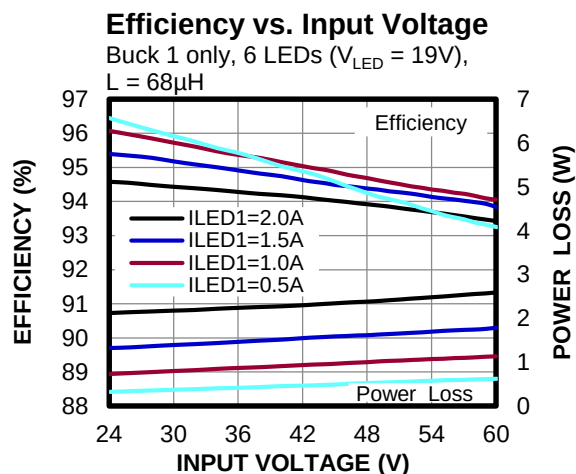
# TYPICAL PERFORMANCE CHARACTERISTICS

$V_{IN} = 48V$ , 12 LEDs in series ( $V_{LED} = 38V$ ),  $f_{SW} = 420kHz$ ,  $L = 68\mu H$ ,  $T_A = 25^\circ C$ , unless otherwise noted.



## TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

$V_{IN} = 48V$ , 12 LEDs in series ( $V_{LED} = 38V$ ),  $f_{SW} = 420kHz$ ,  $L = 68\mu H$ ,  $T_A = 25^\circ C$ , unless otherwise noted.

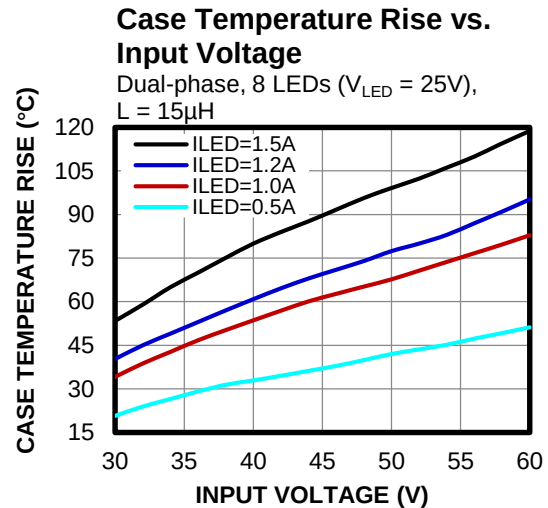
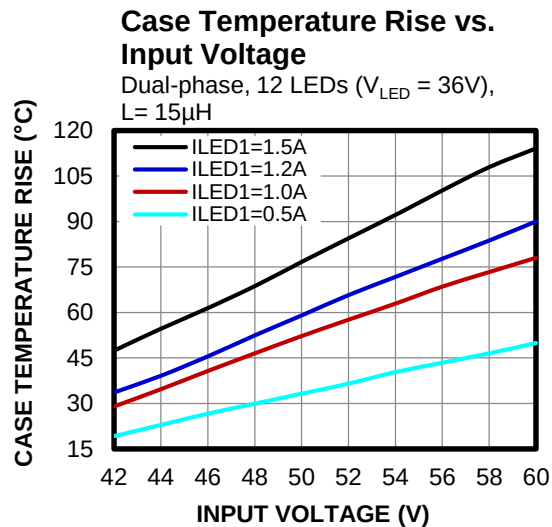
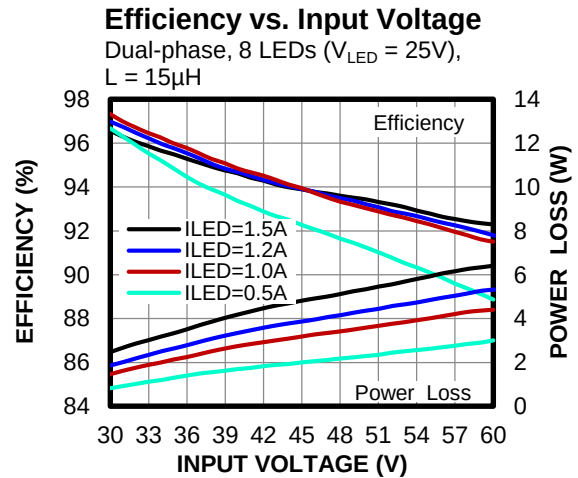
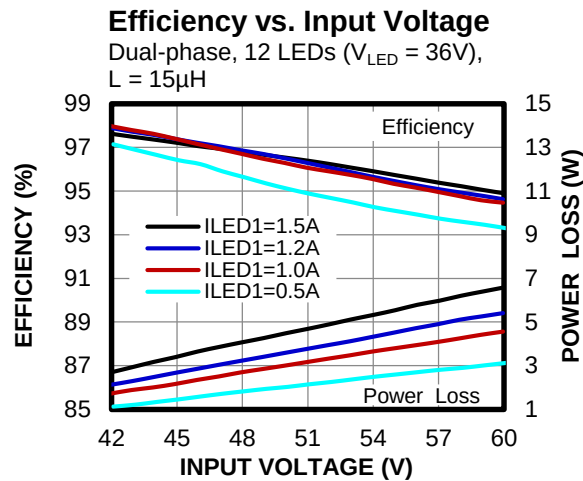


**Note:**

- 8) The efficiency and thermal curves are based on Figure 12 on page 48 when  $R_{BST} = 0\Omega$ , and the output and input filters have been removed.  
 $L = 68\mu H$  (e.g. Würth: 7447709680).

## TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

$V_{IN} = 48V$ , 12 LEDs in series ( $V_{LED} = 38V$ ),  $f_{SW} = 2.3MHz$ ,  $L = 68\mu H$ ,  $T_A = 25^\circ C$ , unless otherwise noted.



**Note:**

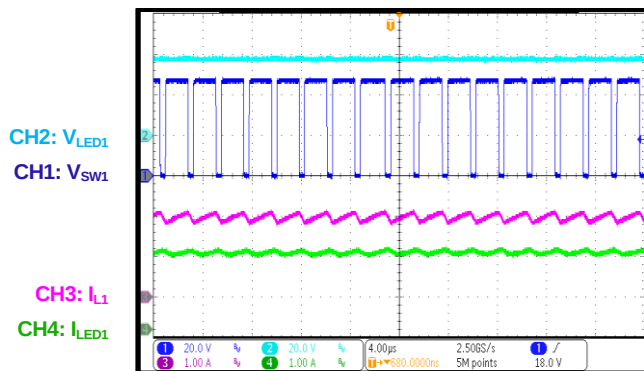
- 9) The efficiency and thermal curves are based on Figure 15 on page 49 when  $R_{BST} = 0\Omega$ , and the output and input filters have been removed.  
 $L = 15\mu H$  (e.g. XAL4040-153MEB).

# TYPICAL PERFORMANCE CHARACTERISTICS (continued)

$V_{IN} = 48V$ , 12 LEDs in series ( $V_{LED} = 38V$ ),  $f_{SW} = 420kHz$ ,  $L = 68\mu H$ ,  $T_A = 25^{\circ}C$ , unless otherwise noted.

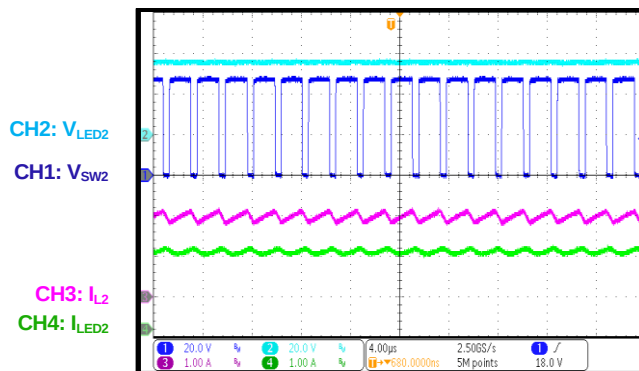
## Steady State (Buck 1)

$I_{LED1} = I_{LED2} = 2A$



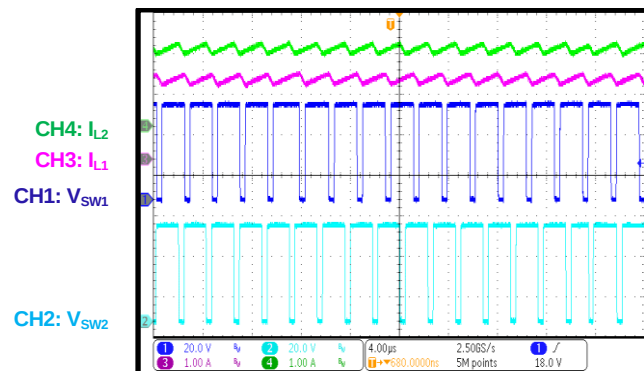
## Steady State (Buck 2)

$I_{LED1} = I_{LED2} = 2A$



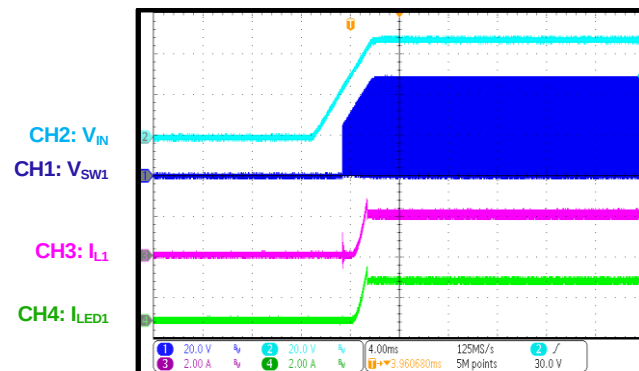
## Steady State

$I_{LED1} = I_{LED2} = 2A$



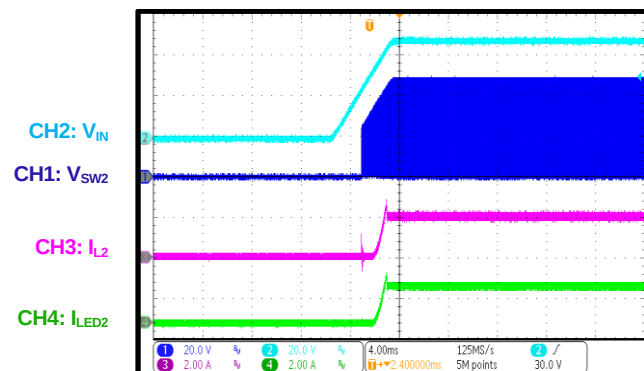
## Start-Up through VIN (Buck 1)

$I_{LED1} = I_{LED2} = 2A$



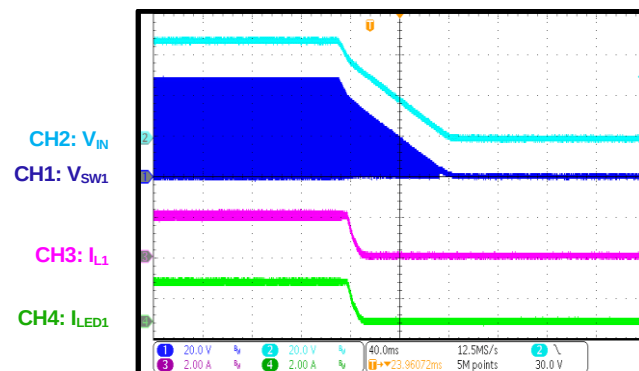
## Start-Up through VIN (Buck 2)

$I_{LED1} = I_{LED2} = 2A$



## Shutdown through VIN (Buck 1)

$I_{LED1} = I_{LED2} = 2A$

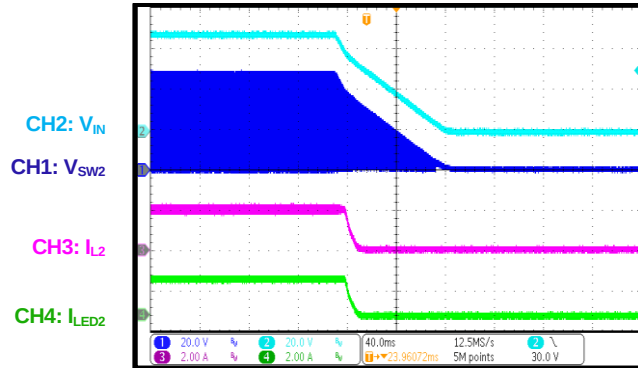


# TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

$V_{IN} = 48V$ , 12 LEDs in series ( $V_{LED} = 38V$ ),  $f_{SW} = 420kHz$ ,  $L = 68\mu H$ ,  $T_A = 25^{\circ}C$ , unless otherwise noted.

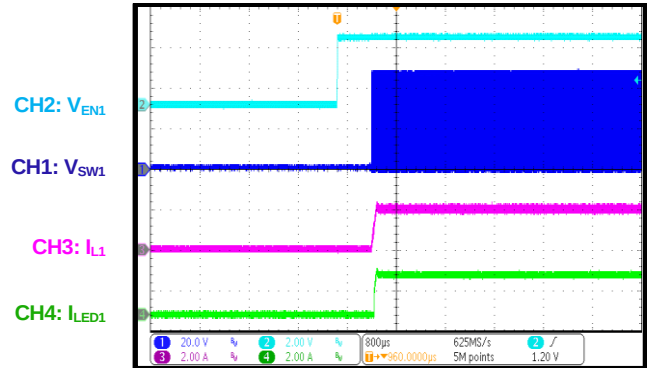
## Shutdown through VIN (Buck 2)

$I_{LED1} = I_{LED2} = 2A$



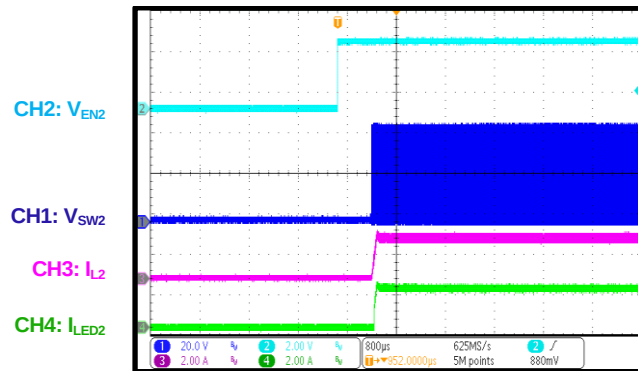
## Start-Up through EN1 (Buck 1)

$I_{LED1} = I_{LED2} = 2A$



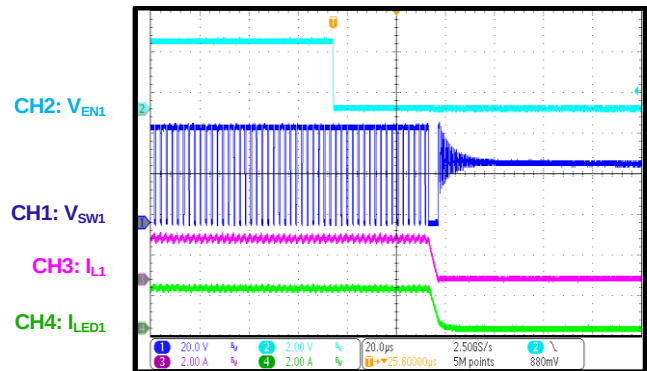
## Start-Up through EN2 (Buck 2)

$I_{LED1} = I_{LED2} = 2A$



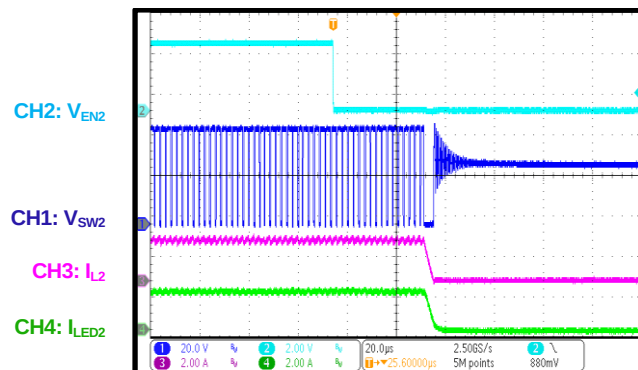
## Shutdown through EN1 (Buck 1)

$I_{LED1} = I_{LED2} = 2A$



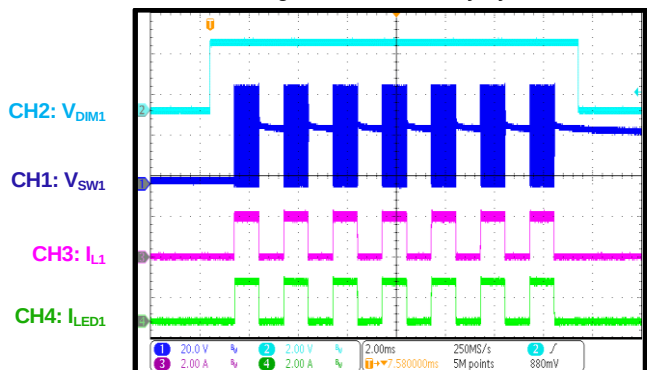
## Shutdown through EN2 (Buck 2)

$I_{LED1} = I_{LED2} = 2A$



## PWM Dimming Mode 1 Steady State (Buck 1)

PWM dimming: 500Hz/50% duty cycle

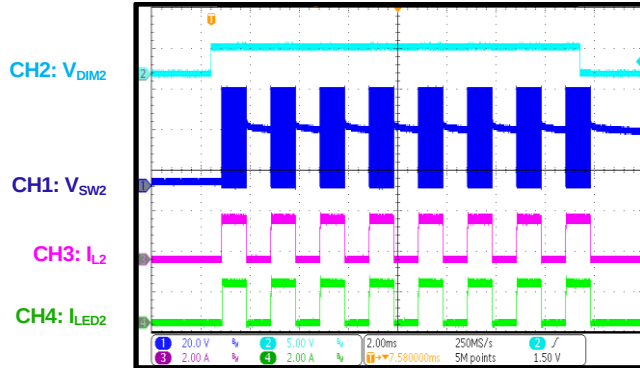


# TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

$V_{IN} = 48V$ , 12 LEDs in series ( $V_{LED} = 38V$ ),  $f_{SW} = 420kHz$ ,  $L = 68\mu H$ ,  $T_A = 25^{\circ}C$ , unless otherwise noted.

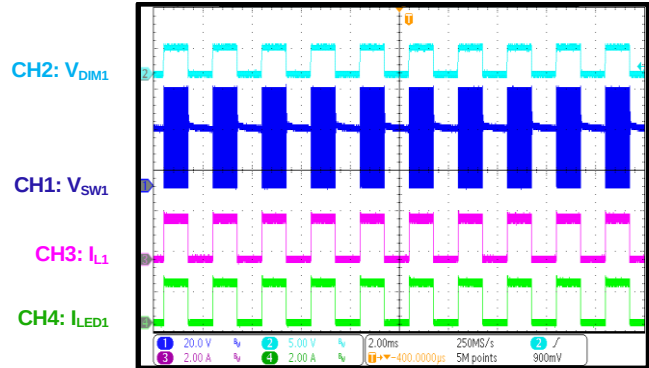
## PWM Dimming Mode 1 Steady State (Buck 2)

PWM dimming: 500Hz/50% duty cycle



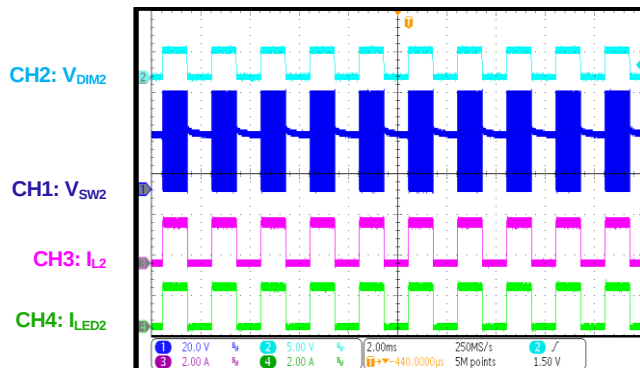
## PWM Dimming Mode 2 Steady State (Buck 1)

PWM dimming: 500Hz/50% duty cycle



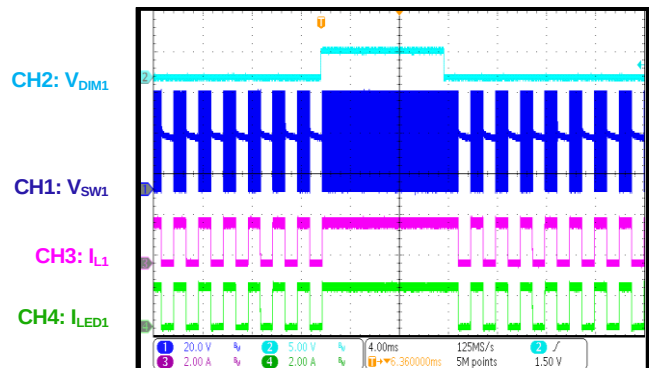
## PWM Dimming Mode 2 Steady State (Buck 2)

PWM dimming: 500Hz/50% duty cycle



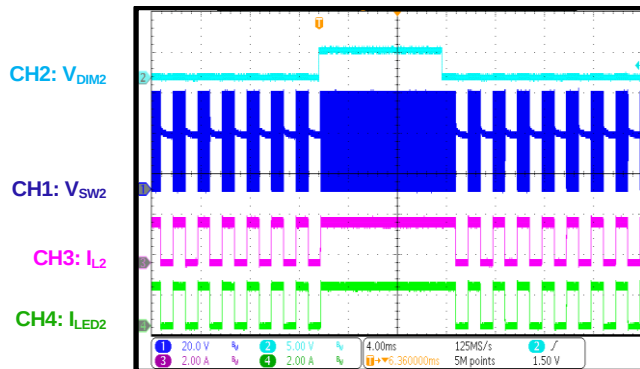
## PWM Dimming Mode 3 (Buck 1)

PWM dimming: 500Hz/50% duty cycle



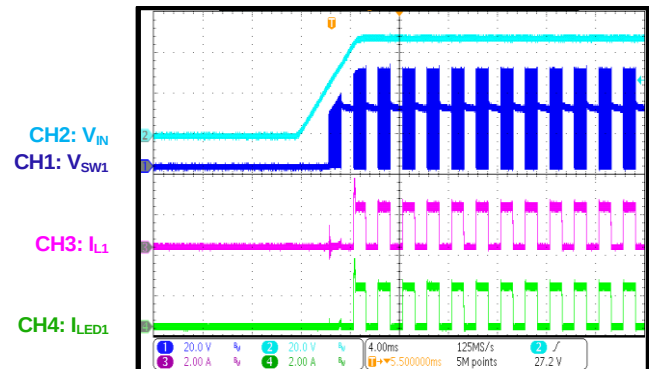
## PWM Dimming Mode 3 (Buck 2)

PWM dimming: 500Hz/50% duty cycle



## PWM Dimming Mode 2 (Buck 1)

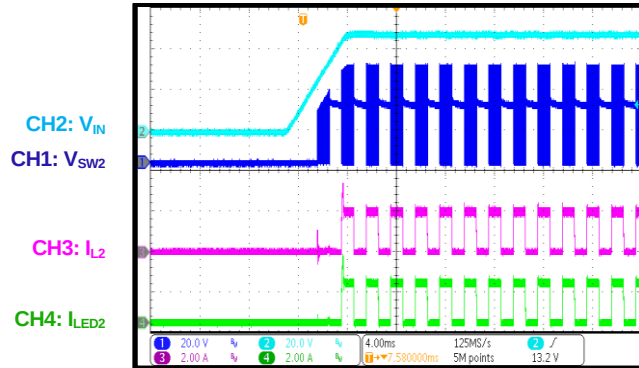
Start-up through  $V_{IN}$



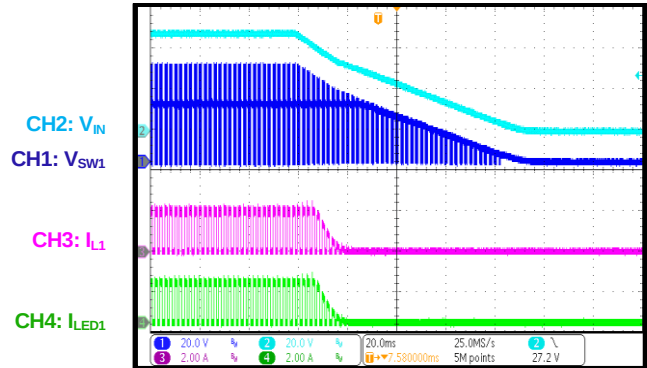
# TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

$V_{IN} = 48V$ , 12 LEDs in series ( $V_{LED} = 38V$ ),  $f_{SW} = 420kHz$ ,  $L = 68\mu H$ ,  $T_A = 25^{\circ}C$ , unless otherwise noted.

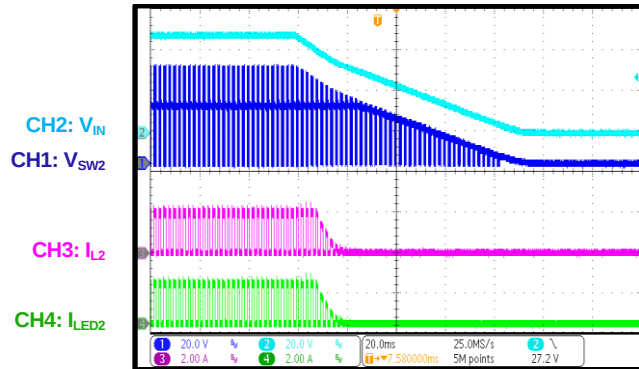
**PWM Dimming Mode 2 (Buck 2)**  
Start-up through VIN



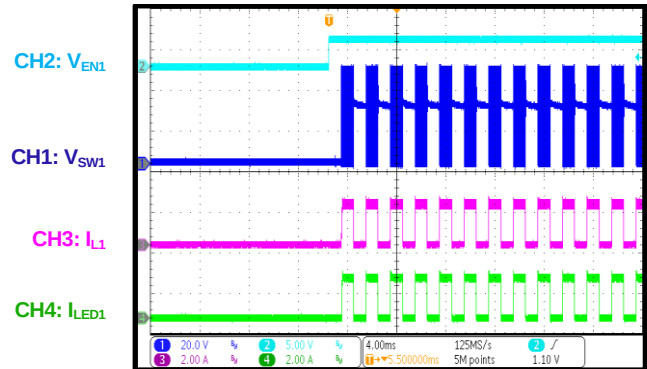
**PWM Dimming Mode 2 (Buck 1)**  
Shutdown through VIN



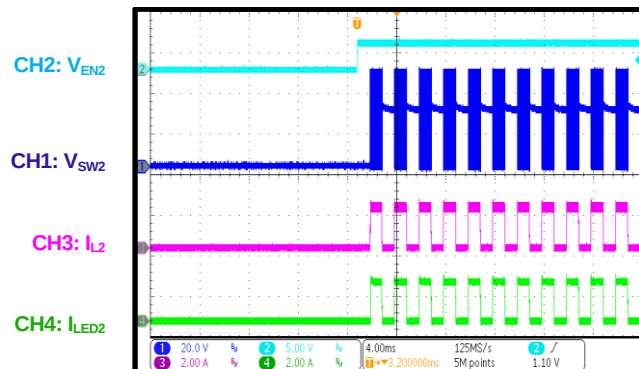
**PWM Dimming Mode 2 (Buck 2)**  
Shutdown through VIN



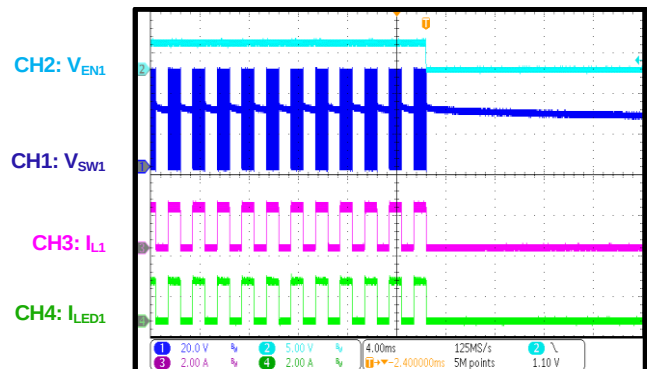
**PWM Dimming Mode 2 (Buck 1)**  
Start-up through EN1



**PWM Dimming Mode 2 (Buck 2)**  
Start-up through EN2



**PWM Dimming Mode 2 (Buck 1)**  
Shutdown through EN1

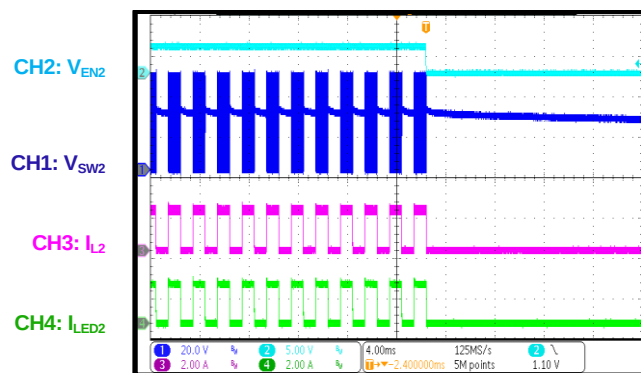


# TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

$V_{IN} = 48V$ , 12 LEDs in series ( $V_{LED} = 38V$ ),  $f_{SW} = 420kHz$ ,  $L = 68\mu H$ ,  $T_A = 25^{\circ}C$ , unless otherwise noted.

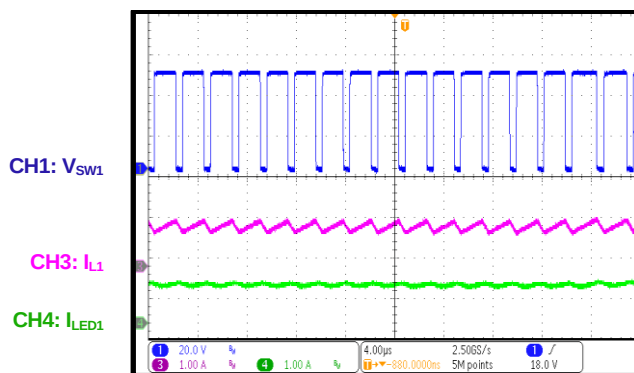
## PWM Dimming Mode 2 (Buck 2)

Shutdown through EN2



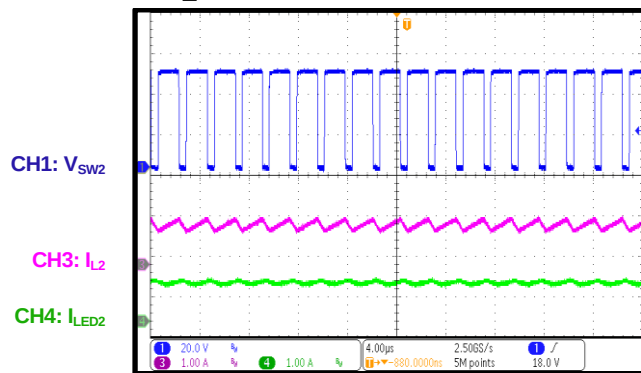
## Analog Dimming

ANA\_DIM1 = 0x64 ( $V_{REF} = 100mV$ )



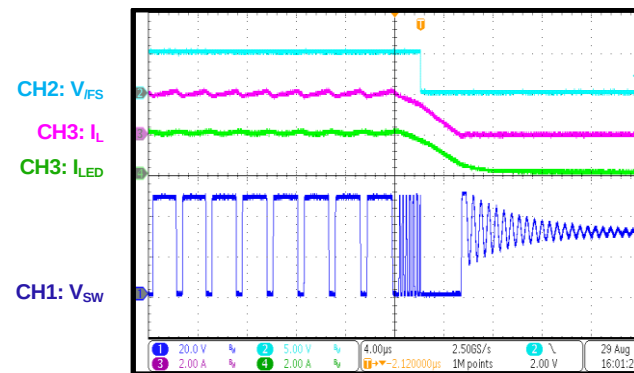
## Analog Dimming

ANA\_DIM2 = 0x64



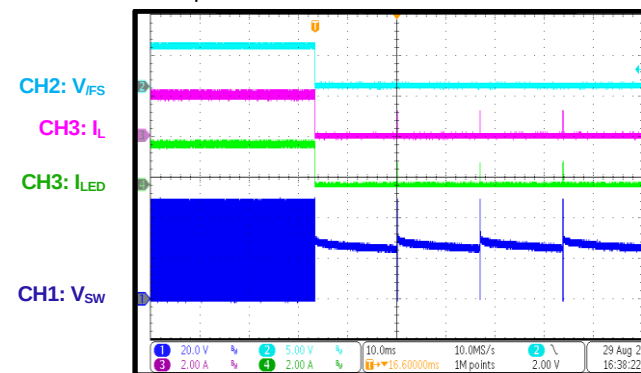
## OCP Entry

Latch-off mode, OCP mask disabled



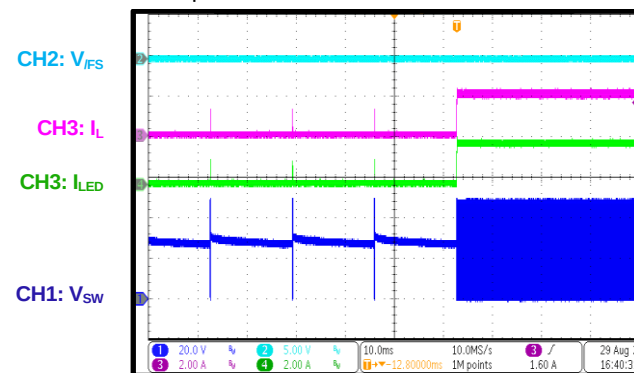
## OCP Entry

Hiccup mode, OCP mask disabled



## OCP Recovery

Hiccup mode, OCP mask disabled

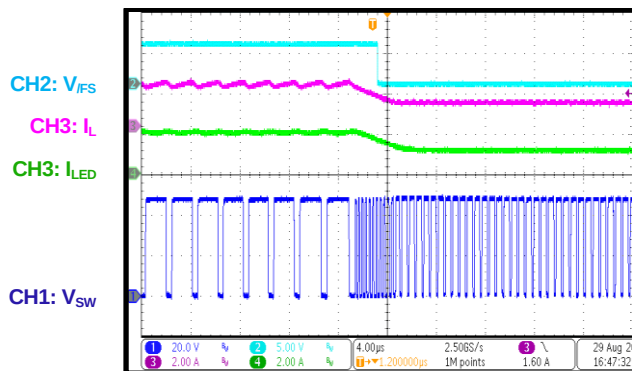


## TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

$V_{IN} = 48V$ , 12 LEDs in series ( $V_{LED} = 38V$ ),  $f_{SW} = 420kHz$ ,  $L = 68\mu H$ ,  $T_A = 25^\circ C$ , unless otherwise noted.

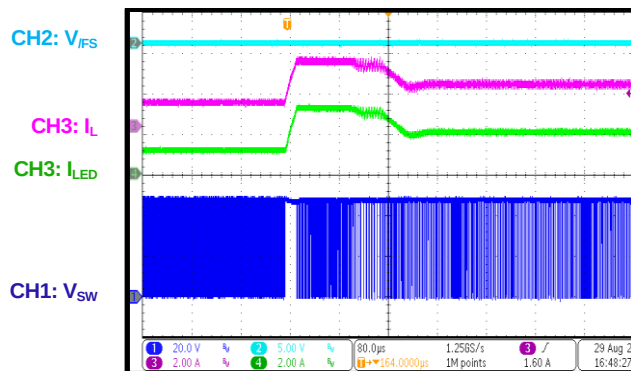
### OCP Entry

No action mode, OCP mask disabled



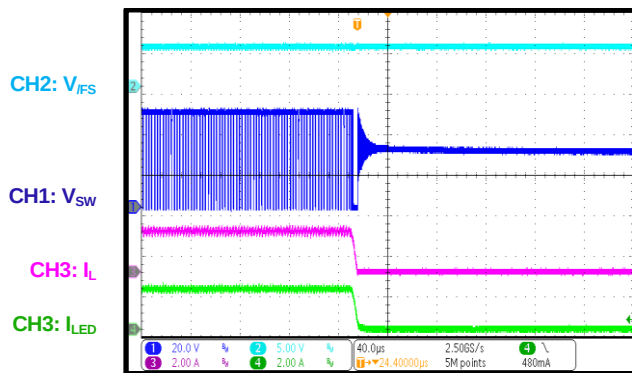
### OCP Recovery

No action mode, OCP mask disabled



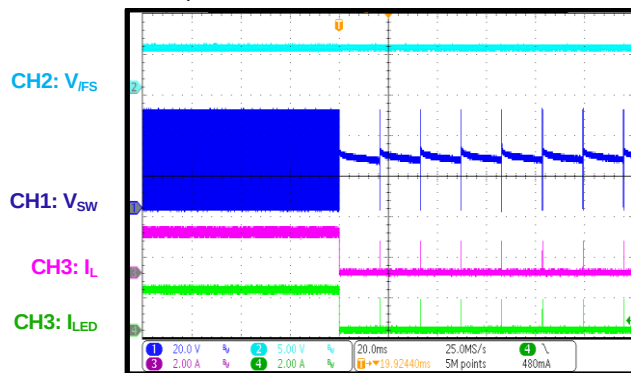
### OCP Entry

Latch-off mode, OCP mask enabled



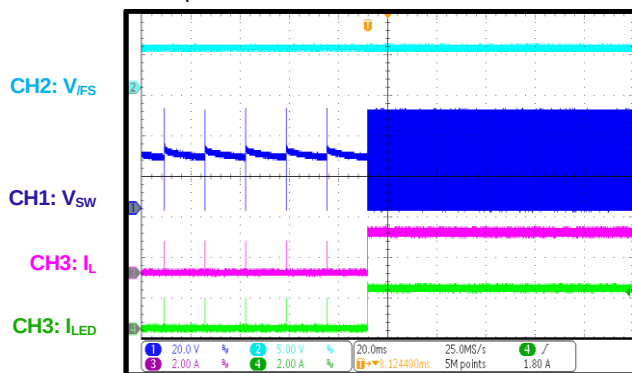
### OCP Entry

Hiccup mode, OCP mask enabled



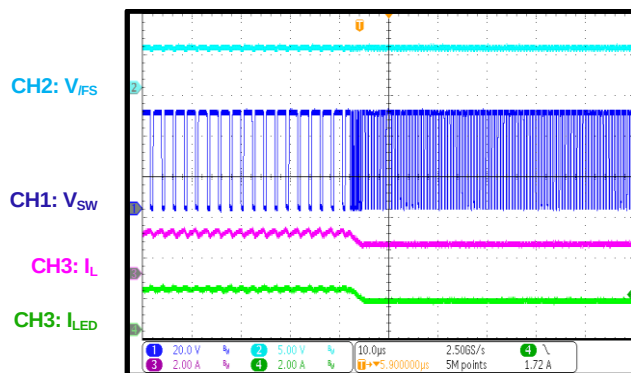
### OCP Recovery

Hiccup mode, OCP mask enabled



### OCP Entry

No action mode, OCP mask enabled

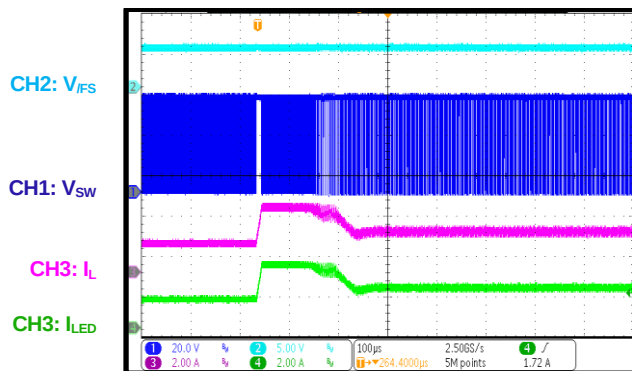


# TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

$V_{IN} = 48V$ , 12 LEDs in series ( $V_{LED} = 38V$ ),  $f_{SW} = 420kHz$ ,  $L = 68\mu H$ ,  $T_A = 25^{\circ}C$ , unless otherwise noted.

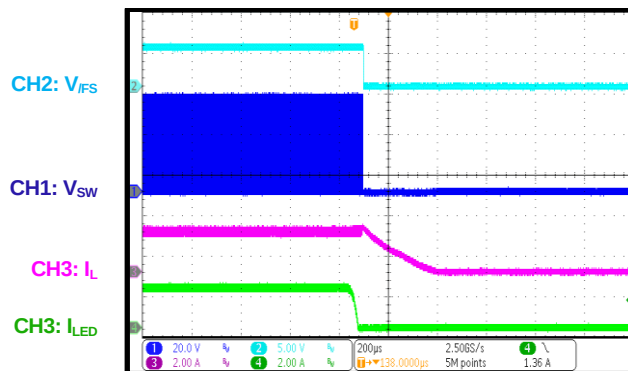
## OCP Recovery

No action mode, OCP mask enabled



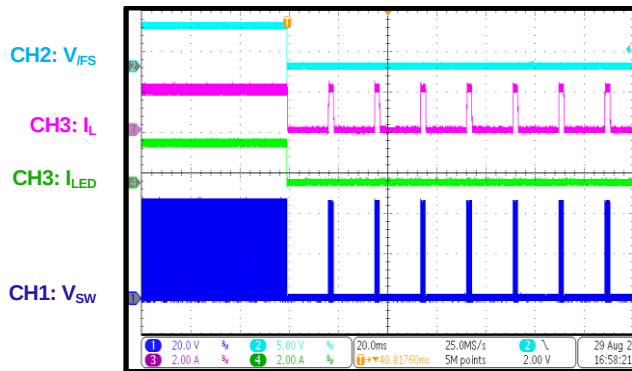
## UVP Entry

Latch-off mode, UVP mask disabled



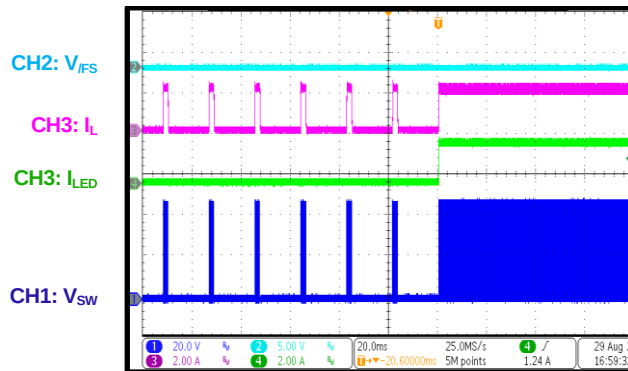
## UVP Entry

Hiccup mode, UVP mask disabled



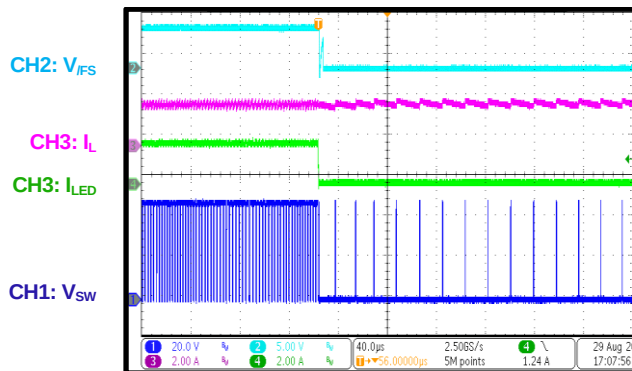
## UVP Recovery

Hiccup mode, UVP mask disabled



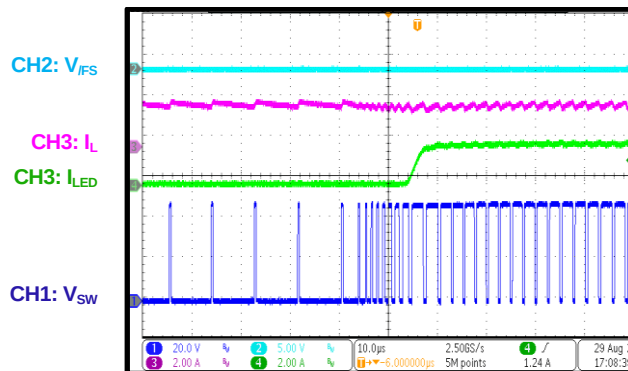
## UVP Entry

No action mode, UVP mask disabled



## UVP Recovery

No action mode, UVP mask disabled

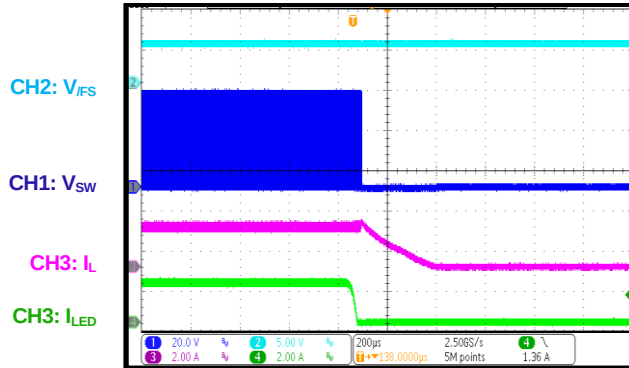


# TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

$V_{IN} = 48V$ , 12 LEDs in series ( $V_{LED} = 38V$ ),  $f_{SW} = 420kHz$ ,  $L = 68\mu H$ ,  $T_A = 25^{\circ}C$ , unless otherwise noted.

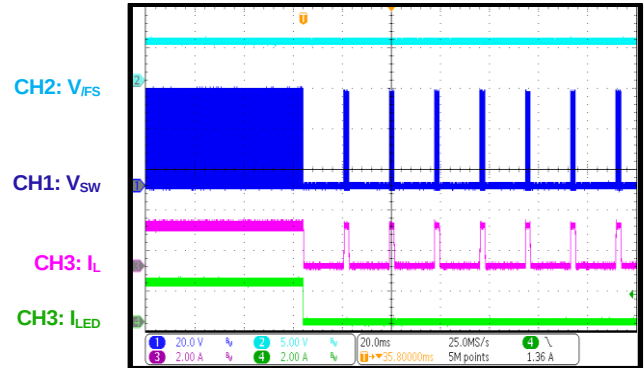
## UVP Entry

Latch-off mode, UVP mask enabled



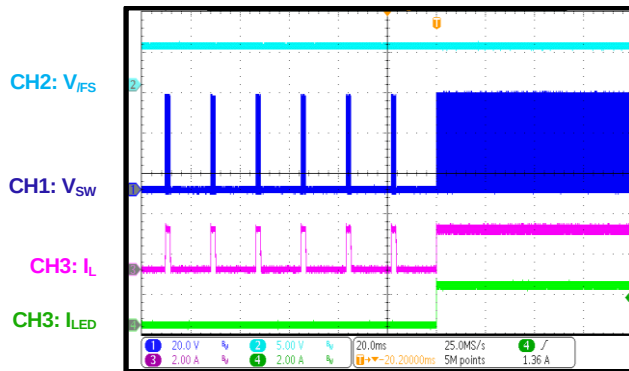
## UVP Entry

Hiccup mode, UVP mask enabled



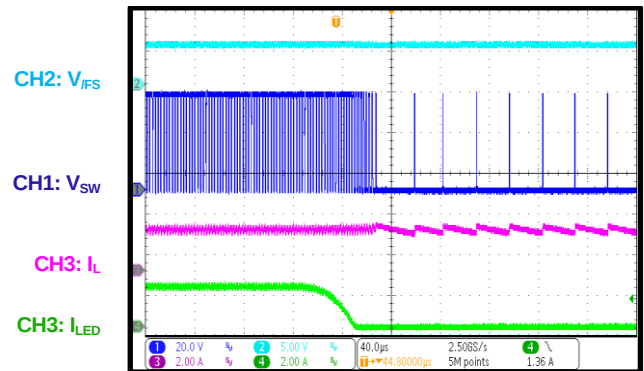
## UVP Recovery

Hiccup mode, UVP mask enabled



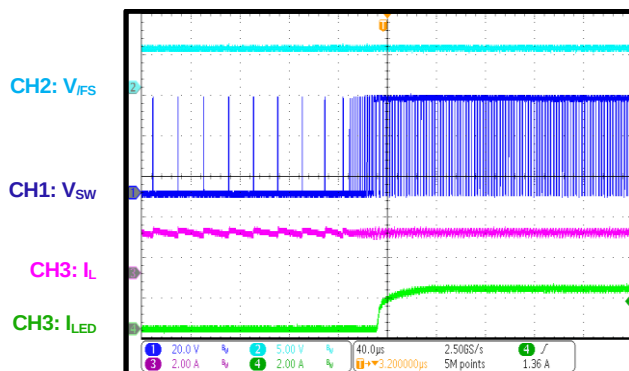
## UVP Entry

No action mode or UVP mask enabled

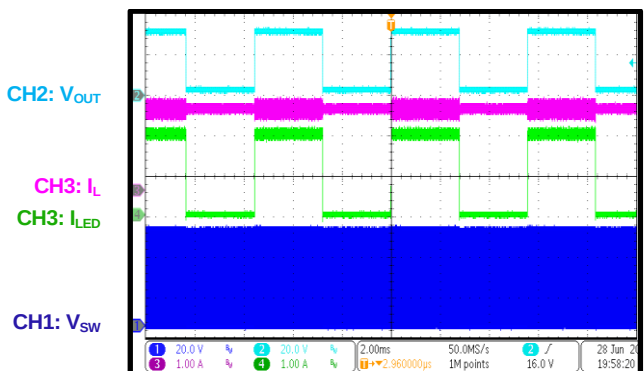


## UVP Recovery

No action mode or UVP mask enabled



## Shunt Dimming (UVP Disabled)

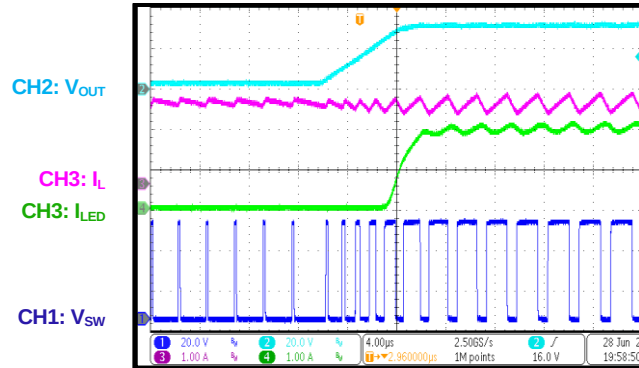


## TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

$V_{IN} = 48V$ , 12 LEDs in series ( $V_{LED} = 38V$ ),  $f_{SW} = 420kHz$ ,  $L = 68\mu H$ ,  $T_A = 25^\circ C$ , unless otherwise noted.

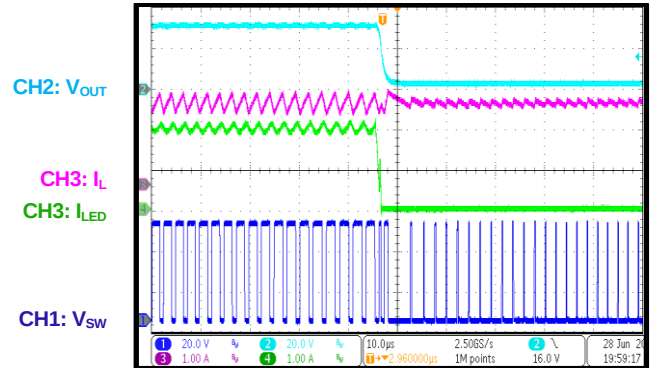
### Shunt Dimming On (UVP Disabled)

LED off to on: 0V to 36V



### Shunt Dimming Off (UVP Disabled)

LED on to off: 36V to 0V



## FUNCTIONAL BLOCK DIAGRAM

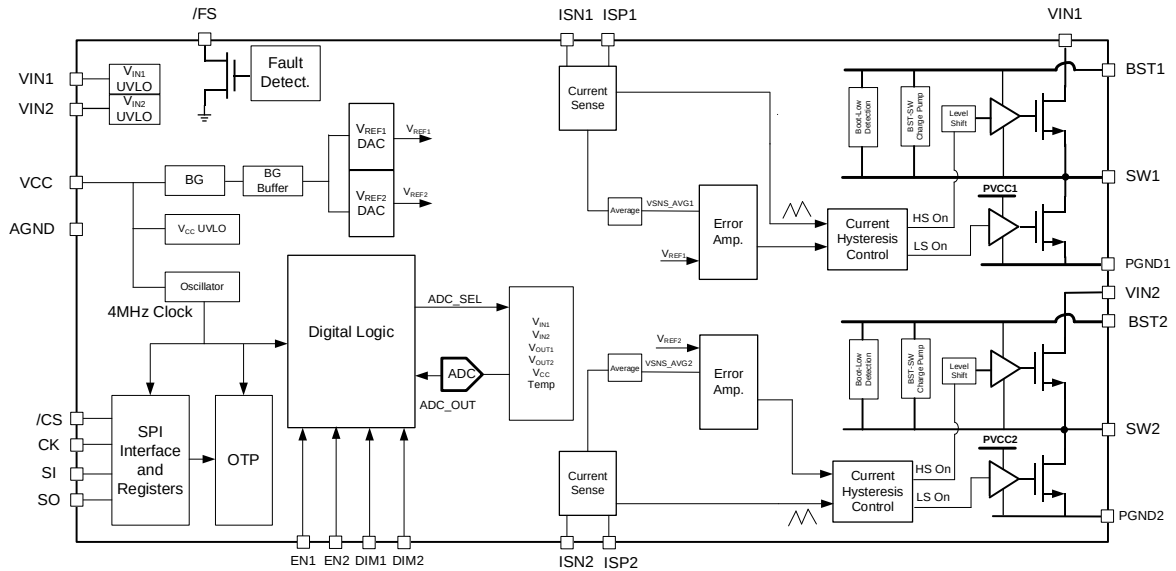


**Figure 2: Functional Block Diagram**

## OPERATION

The MPQ7210 is a high-frequency, synchronous, rectified, switch-mode buck LED driver with built-in power MOSFETs. It offers a very compact solution to achieve 2A of continuous output current ( $I_{OUT}$ ) with a dual-buck converter. The MPQ7210 provides excellent load and line regulation across a 4.5V to 60V input voltage ( $V_{IN}$ ) supply range.

The MPQ7210's two output channels can work alone. If a channel is not used, pull its ENx and DIMx pin low, and float the following pins: SWx, ISPx, ISNx, and BSTx.

The two output channels can operate in parallel as one phase to support high-current applications via the one-time programmable (OTP) memory. A single- or dual-inductor can be used for thermal consideration. In a single-phase configuration, float the EN2, DIM2, ISP2, and ISN2 pins; meanwhile, the internal buck 1 and buck 2 MOSFETs operate in parallel.

For higher power, two (or more) MPQ7210 devices can operate in parallel.

### Fixed-Frequency Band-to-Band Control

The MPQ7210 uses fixed-frequency band-to-band control. Compared to fixed-frequency pulse-width modulation (PWM) control, band-to-band control offers the advantages of a simpler control loop and faster transient response. Even without the output capacitor, the loop is stable.

Band-to-band control compares the inductor current ( $I_L$ ) to the internal thresholds: the peak ( $I_{BAND\_PEAK}$ ) and the valley ( $I_{BAND\_VALLEY}$ ). When  $I_L$  exceeds  $I_{BAND\_PEAK}$ , the high-side MOSFET (HS-FET) turns off. When  $I_L$  is below  $I_{BAND\_VALLEY}$ , the HS-FET turns on.  $(I_{BAND\_PEAK} + I_{BAND\_VALLEY}) / 2$  is controlled by a PID loop to regulate the LED current ( $I_{LED}$ ) to the set value.

$I_{BAND\_PEAK} - I_{BAND\_VALLEY}$  is controlled by a phase-locked loop (PLL) to regulate the switching frequency ( $f_{SW}$ ) to 420kHz or another frequency, as set by the relevant OTP register.

If the minimum on time ( $t_{ON\_MIN}$ ) or minimum off time ( $t_{OFF\_MIN}$ ) are triggered,  $f_{SW}$  is extended and the real  $f_{SW}$  is  $(D / t_{ON\_MIN})$  or  $((1 - D) / t_{OFF\_MIN})$ ,

where D is the required duty cycle. Typically,  $t_{ON\_MIN}$  is 125ns, and  $t_{OFF\_MIN}$  is 120ns.

The MPQ7210 is compatible with shunt MOSFET dimming and LED matrix manager devices. The fast dynamic response ensures near ideal current source behavior with minimal  $I_L$  overshoot or undershoot.

The device's behavior is impacted by the ISN1 and ISN2 node's falling slew rate. A faster falling slew rate and greater output capacitance pose risks to the shut MOSFET. In these scenarios, a larger inductance and lower output capacitance is strongly recommended. In theory, even without the output capacitor, the MPQ7210's loop should be stable, which makes it well-suited for applications with a faster falling slew rate.

### LED Current ( $I_{LED}$ ) Sense

The external resistor ( $R_{SEN}$ ) connected between the ISPx and ISNx pins sets the LED current ( $I_{LED}$ ).  $I_{LED}$  can be calculated with Equation (1):

$$I_{LED} (A) = \frac{0.2}{R_{SEN} (\Omega)} \quad (1)$$

If the MPQ7210 is configured for single-phase operation,  $I_{LED}$  can only set by the resistor between ISP1 and ISN1, and it can still be calculated with Equation (1).

### Analog-to-Digital Converter (ADC)

The MPQ7210 incorporates a 10-bit successive approximation register (SAR) analog-to-digital converter (ADC). The single ADC can be multiplexed to sample certain signals (see Table 1). The ADC can only sample one signal each time. The ADC\_INMUX bit value in Table 1 selects which signal is sampled.

**Table 1: ADC Sample Information (Register 0x12)**

| Selection | Description                     |
|-----------|---------------------------------|
| 000       | CH1: buck 1 input = $V_{IN1}$   |
| 001       | CH2: buck 1 output = $V_{OUT1}$ |
| 010       | CH3: buck 2 input = $V_{IN2}$   |
| 011       | CH4: buck 2 output = $V_{OUT2}$ |
| 100       | CH5: VCC voltage = $V_{CC}$     |
| 101       | Part temperature: $T_J$         |
| 110/111   | Not used                        |

Register 0x12, bit D[3] can control when the ADC starts sampling the data. To obtain the information regarding  $V_{IN}$ ,  $V_{OUT}$ ,  $V_{CC}$ , and  $T_J$ , follow the steps below:

1. Write to register 0x12, bits D[2:0] to select which signal to monitor.
2. Read 0x12. If bits D[7:5] = bits D[2:0] and bit D[4] = 1, then proceed to step 3; if not, return to step 1.
3. Write register 0x12, bit D[3] = 1.
4. Read register 0x13, bits D[9:0].

When the sensed signal is  $V_{IN1}$ ,  $V_{IN2}$ ,  $V_{OUT1}$ , or  $V_{OUT2}$ , the voltage is first divided by 32.125. (For example, if  $V_{IN}$  is 40V, it will become 1.245V.) The new value is sent to the ADC input. The ADC is 10 bits, and 1 LSB is 2mV (0b1001101111).

Register 0x13, bits D[7:0] (0b10011011 = 0h155) is updated based on the 8MSB of the ADC conversion. The final 2LSB are ignored. The relationship between the sensed voltage and the ADC\_DATA[7:0] can be estimated with Equation (2):

$$V_{IN}(V) = \text{ADC\_DATA}[7:0] \times 0.257 \quad (2)$$

When the sensed signal is  $V_{CC}$ , the voltage is divided by 4. (For example, if  $V_{CC}$  is 5V, then it becomes 1.25V.) The relationship between  $V_{CC}$  and ACC\_DATA can be calculated with Equation (3):

$$V_{CC}(V) = \text{ADC\_DATA}[7:0] \times 0.032 \quad (3)$$

When the sensed signal is  $T_J$ , the temperature information can be transferred to a voltage ( $V_T$ ), estimated with Equation (4):

$$V_T = 1.05 + 0.004 \times T_J \quad (4)$$

The relationship between  $T_J$  and ADC\_DATA can be calculated with Equation (5):

$$T_J = 2 \times (\text{ADC\_DATA}[7:0] - 131.25) \quad (5)$$

### Continuous Conduction Mode (CCM) and Discontinuous Conduction Mode (DCM)

The MPQ7210 uses continuous conduction mode (CCM) to ensure that the part works with a fixed frequency from a minimum load to a full-load range. The advantages of CCM are its controllable frequency and lower output voltage ripple under light loads.

When  $I_{\text{BAND\_VALLEY}} = 0A$ , the MPQ7210 enters discontinuous current mode (DCM). The low-side MOSFET (LS-FET) turns off once zero-current detection (ZCD) is triggered, then the LS-FET acts as an ideal diode. At light loads,  $f_{\text{SW}}$  decreases, and the SWx pin may skip a pulse if the device enters DCM. This may make the current ripple too high and make the current precision too low. Select a larger-value inductor so that the device can operate in CCM under any condition.

### Enable (EN) Control

EN is a control pin that turns the regulator on and off. Drive EN above 1V to turn the regulator on; drive EN below 0.85V to turn it off. EN can be connected to VCC through a resistor, but it cannot be connected directly to VIN through a resistor. In a dual-channel configuration, EN1 or EN2 going low can only reset buck 1 or buck 2, respectively. The analog circuit and register value cannot be reset. If both EN1 and EN2 pull low, the IC resets completely. In a single-channel configuration, only EN1 can reset the part.

The MPQ7210 can be enabled or disabled by setting the BUCK\_EN bit when ENx is high:

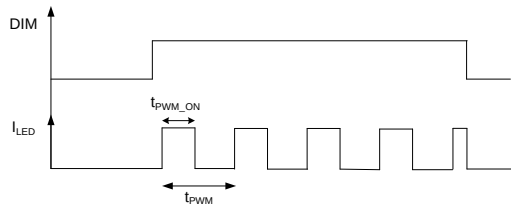
- If the BUCK1/2\_EN bit = 0, enable buck 1/2
- If the BUCK1/2\_EN bit = 1, disable buck 1/2

Only the EN pin can enable or disable the MPQ7210. It is not recommended to use the DIM pin to enable or disable the device, as the error amplifier's output voltage ( $V_{\text{COMP}}$ ) may be discharged by the leakage if the dimming off time is too long.

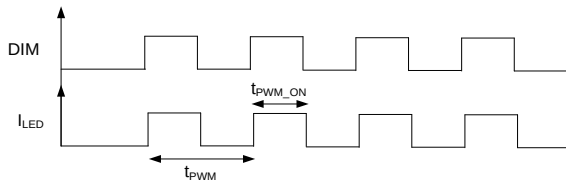
### Pulse-Width Modulation (PWM) Dimming

The MPQ7210 can be configured to PWM dimming mode with three different selections. The PWM dimming on time should be longer than 60μs, and the PWM dimming frequency should be between 100Hz and 2kHz. Ensure that the dimming off time is no longer than 10ms.

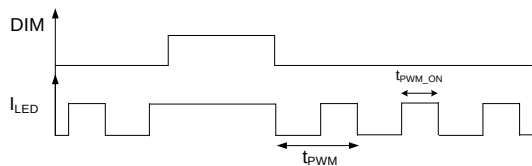
1. PWM dimming mode 1: When pulling the DIM pin high, the device dims with a certain PWM dimming frequency and duty cycle. The frequency and duty cycle can be configured via the SPI. When the DIM pin pulls low, the MPQ7210 stops switching. Figure 3 on page 28 shows PWM dimming mode 1.


**Figure 3: PWM Dimming Mode 1**

2. **PWM dimming mode 2:** When applying an external 100Hz to 2kHz PWM signal to the DIM pin, the MPQ7210 stops switching when the DIM voltage is below 1.15V and  $I_{LED}$  is zero. The device resumes normal operation with the nominal  $I_{LED}$  when the DIM pin's voltage exceeds 1.25V. The average  $I_{LED}$  is proportional to the PWM duty cycle. Figure 4 shows PWM dimming mode 2.


**Figure 4: PWM Dimming Mode 2**

3. **PWM dimming mode 3:** The DIM pin is used as the input pin to select the LED current with a full current or a certain dimming duty cycle. When the DIM pin's voltage is high, the device works at a 100% dimming duty cycle; when this voltage is low, the works at X% dimming duty cycle, where X is determined by the register setting. Figure 5 shows PWM dimming mode 3.


**Figure 5: PWM Dimming Mode 3**

For PWM dimming mode 1 and PWM dimming mode 3, the dimming frequency is determined by DEV\_CFG, bits D[3:0] (125Hz, 250Hz, 500Hz, and 1kHz) in register 0x03. The duty cycle is determined by the dimming duty cycle on register 0x04 and 0x05, bits D[11:0].

### Analog Dimming

$I_{LED}$  can also be set by the analog dimming register through the SPI. The reference voltage ( $V_{REF}$ ) can be adjusted to a maximum 127.5% of

200mV. The default analog dimming register value is 0x00C8, which corresponds to a 200mV  $V_{REF}$ .  $V_{REF}$  can be estimated with Equation (6):

$$V_{REF} = 0x06, \text{ bits D}[7:0] / 200 \times 200\text{mV} \quad (6)$$

The minimum  $V_{REF}$  is 10mV, and the maximum  $V_{REF}$  is 255mV.

### Under-Voltage Lockout (UVLO)

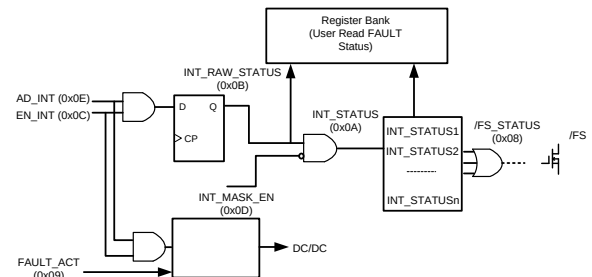
Under-voltage lockout (UVLO) protects the chip from operating at an insufficient supply voltage. Both  $V_{IN}$  and  $V_{CC}$  have UVLO.  $V_{IN}$  and  $V_{CC}$  both have a rising UVLO threshold of 4.2V with a 0.2V hysteresis.  $V_{IN}$  and  $V_{CC}$  UVLO do not trigger the /FS pin. There is no internal VCC regulator for the MPQ7210, so it requires an additional 5V DC source to power VCC. Add a 1μF to 10μF decoupling ceramic capacitor at the VCC pin.

When the device starts up, VCC should turn on first. Once  $V_{CC}$  exceeds its UVLO threshold, the internal logic builds up. Then power on  $V_{IN}$ . When shutting down, turn  $V_{IN}$  off first, then disable VCC to shut down the internal circuit.

### Faults Detection and Diagnostics

The MPQ7210 has a fault indicator pin (/FS). /FS is high at normal operation, but interruptions pull this pin low to indicate a fault status for the following: output under-voltage protection (UVP), over-current protection (OCP), BST UV condition,  $T_J$  thermal warning (TW), and thermal shutdown (TSD).

When the false interruption register mask is enabled, the /FS pin does not pull low, even if an interruption occurs. The MPQ7210 has multiple registers to indicate if an interruption occurs (see Figure 6).


**Figure 6: Interruption Diagram**

AD\_INT (UVP, OCP, TSD) indicates whether an interrupt has actually occurred (see Figure 6).

Only when EN\_INT (interruption enable) is enabled, the INT\_RAW\_STATUS and analog circuit (DC/DC) react to the interruption. INT\_RAW\_STATUS can be also masked by the INT\_MASK\_EN register (mask is enable); then INT\_STATUS does not flag 1, and the /FS does not pull low (see Figure 6 on page 28).

The /FS pin can be cleared by writing 0xFFFF to register 0x0A when the interruption is removed. The user can read the INT\_STATUS (0x0A) register to check whether an interruption has occurred. Table 2 shows the device's behavior under different fault conditions.

**Table 2: Device Behavior under Fault Conditions**

| Protection Feature                                                                              | Protection Behavior                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                         |
|-------------------------------------------------------------------------------------------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| <b>Once the below interruption is triggered, the related fault is flagged in register 0x0A.</b> |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                             |
| Inductor current over-current protection (OCP)                                                  | <u>Trigger condition:</u> $I_L$ triggers the OC value in registers 0x10 and 0x11. OCP prevents $I_L$ runaway, and it can also be used to limit $I_{LED}$ . Typically, the wrong $I_{LED}$ setting, or the sensing resistor shifting low, can trigger OCP. When the OC condition is triggered, the related fault is flagged. If set to hiccup mode, the device tries to recover every 16ms. If the OC condition remains, the inductor's peak value is limited to an OC value. If the OC condition is removed, the device recovers. OCP can be set to latch-off or no action mode. See the Over-Current Protection (OCP) section on page 30 for more details. |
| Output under-voltage protection (UVP)                                                           | <u>Trigger condition:</u> $V_{OUT}$ drops below the UV threshold (typically 2.3V). Output UVP monitors if there is an LED+ short to GND. The UV threshold is typically 2.3V. If the output is connected to a dimming switch, this feature should be disabled. If set to hiccup mode, the device tries to recover every 16ms. If the UV condition remains, the part works for 1ms to check if the UV condition is removed. If the UV condition is removed, the part recovers. The protection can be set to latch-off or no action mode. For more details, see the Under-Voltage Protection (UVP) section on page 30.                                         |
| Thermal warning (TW)                                                                            | <u>Trigger condition:</u> $T_J$ exceeds the TW threshold (typically 125°C). When the IC's $T_J$ exceeds 125°C. The related fault is flagged, and the device takes no action. After $T_J$ drops below 105°C, the fault flag can be cleared.                                                                                                                                                                                                                                                                                                                                                                                                                  |
| Thermal shutdown (TSD)                                                                          | <u>Trigger condition:</u> $T_J$ exceeds the TSD threshold (typically 170°C). If $T_J$ exceeds 170°C, TSD is triggered. All output channels turn off for this protection. When $T_J$ drops to 150°C, the device recovers in hiccup mode. In latch-off mode, the device must be reset by EN, $V_{CC}$ , or $V_{IN}$ UVLO.                                                                                                                                                                                                                                                                                                                                     |
| BST voltage under-voltage lockout (UVLO)                                                        | <u>Trigger condition:</u> The BST-to-SW voltage drops below the UV threshold (typically 2.5V). This protection monitors the BST-to-SW voltage. If the BST voltage is below the UVLO threshold (2.2V), UVLO is triggered. The device shuts down (no switching, $V_{OUT}$ drops to 0V). The device recovers switching when the BST voltage exceeds the 2.5V rising threshold.                                                                                                                                                                                                                                                                                 |
| One-time programmable (OTP) memory indicator failure protection                                 | Each time the device starts up, the part will self-check if there is an OTP error. If there is an OTP error, the part stays in an idle status.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                              |
| OTP program failure protection                                                                  | Checks if the OTP program is successful when the device undergoes OTP in the factory. This bit can be covered by OTP indicator protection.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                  |
| OTP cyclic redundancy check (CRC) failure protection                                            | After the OTP indicator check finishes, the device checks the OTP data's CRC. If there is any wrong data, the CRC value is different, the CRC error is flagged, and the device maintains an idle status. Both OTP indicator and OTP CRC failures force the device to an idle state with no switching.                                                                                                                                                                                                                                                                                                                                                       |
| <b>Once the below interruption is triggered, no fault register is flagged.</b>                  |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                             |
| $V_{IN}$ UVLO                                                                                   | The device shuts down and stops switching.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                  |
| $V_{CC}$ UVLO                                                                                   | The device shuts down and stops switching.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                  |
| Minimum off time is triggered                                                                   | The device enters dropout mode, and the frequency folds back to low gradually while $V_{IN}$ drops. $I_{LED}$ cannot stay at the set value in deep dropout mode.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                            |

### Over-Current Protection (OCP)

The MPQ7210 has cycle-by-cycle peak current-limit protection.  $I_L$  is monitored while the HS-FET is on. If  $I_L$  exceeds the current-limit value, the HS-FET turns off immediately. Then the LS-FET turns on to discharge the energy, and  $I_L$  decreases. The HS-FET remains off unless  $I_L$  drops to zero, and then another HS-FET on cycle starts. OCP can be disabled or enabled with three choices when an OC condition is triggered. If OCP is enabled and an OC condition is triggered, the device can be set to no action, latch-off, or hiccup mode:

- **No action:** The device continues switching, but the current is limited to the set OC value.
- **Hiccup mode:** The device tries to recover every 16ms; if the OC condition remains, the inductor's peak value is limited to the set OC value. If the OC condition is removed, the device recovers.
- **Latch-off mode:** The device latches off and stops switching, even the OC condition is removed. The device does not recover even if the OC condition is removed.

The OC value can be set via the OTP or adjusted through the SPI via register 0x11, bits[5:4] (for buck 1) and 0x11, bits[2:0] (for buck 2). Select the OC behavior and OC limit based on the specifications. The OC limit should be 50% greater than the maximum  $I_{LED}$ .

**Table 3: OC Value Selection**

| Register Selection | OC Limit | Register Selection | OC Limit |
|--------------------|----------|--------------------|----------|
| 000                | 500mA    | 100                | 2.5A     |
| 001                | 1A       | 101                | 3A       |
| 010                | 1.5A     | 110                | 3.5A     |
| 011                | 2A       | 111                | 4A       |

Set the OC response based on the application requirements. If OCP is disabled or the device is set to no action, conduct a thorough validation at the system level.

### Under-Voltage Protection (UVP)

The MPQ7210 provides output UVP by monitoring the ISNx pin's voltage. If the ISNx pin's voltage drops below the UVP threshold (typically 2.3V), UVP is detected. UVP can be enabled or disabled with three potential responses. If UVP is enabled and a UV condition

is triggered, the device can be set to no action, hiccup, or latch-off mode:

- **No action:** The device continues switching and the inductor's average current stays at the set current. If the minimum on time is triggered, the frequency drops.
- **Hiccup mode:** The device tries to recover every 16ms; if the UV condition is removed, the device recovers.
- **Latch-off mode:** The device latches off and stops switching the UV condition is triggered; the device does not recover even if the UV interruption is removed and the /FS register is cleared.

UVP protects from LED+ short to LED-, but if the MPQ7210 is used to power shunt FET dimming and LED matrix manager devices, all the dimming switches may turn on at the same time. In this scenario,  $V_{OUT}$  may be discharged to 0V, which triggers UVP. UVP should be disabled for these applications.

If the dimming duty cycle is set to 0% for a long time during normal PWM dimming conditions,  $V_{OUT}$  is discharged to 0V. This may also trigger UVP. Disable UVP before setting the PWM dimming duty cycle to 0%. For these applications, the LED+ short to LED- condition can be monitored by reading  $V_{OUT}$  through the ADC.

### Thermal Warning (TW)

If  $T_J$  exceeds 125°C, the STATUS\_TWN bit asserts and the /FS pin pulls low, while the IC continues working. When the thermal warning condition is removed (20°C hysteresis), /FS stays low and the /FS bit remains flagged at 1 until it has been cleared by the MCU.

The thermal warning interrupt can be individually masked via TWN\_INT\_MASK\_EN to prevent the /FS open-drain output from pulling low. Even if the thermal warning condition is masked, the thermal warning status can still be read via the /FS\_REAL\_TIME\_STATUS register.

### Thermal Shutdown (TSD)

If  $T_J$  continues to rise, thermal shutdown prevents the chip from operating at exceedingly high temperatures.

When the die temperature exceeds 170°C, all output channels turn off for protection, the STATUS\_TSD bit is set, and the /FS pin asserts. When the IC recovers from thermal shutdown, the /FS pin stays low and the /FS bit is flagged to 1 until it is cleared by the MCU.

Thermal protection can be configured to latch-off or hiccup mode. If set to hiccup mode, the device recovers and turns on the channels when the temperature drops by at least 20°C. The channels return to their previous settings without needing to be reinitialized. If set to latch-off mode, the device latches off when the die temperature exceeds 170°C. Only V<sub>CC</sub>, EN, or V<sub>IN</sub> UVLO can reset the latch.

### Floating Driver and Bootstrap Charging

An external bootstrap capacitor powers the floating power MOSFET driver. The bootstrap capacitor voltage is charged to 5V from V<sub>CC</sub> through a pass transistor when the LS-FET is on. This floating driver has its own UVLO protection, with a rising threshold of 2.5V and a hysteresis of 700mV.

When the BST-to-SW voltage drops to 2.2V, the LS-FET is forced on to refresh the BST voltage. The recommended bootstrap capacitor is a ceramic capacitor between 47nF and 220nF. The actual capacitor's capacitance has a derating that changes at different DC voltages and temperatures. Take this derating into account when choosing the capacitor to ensure that the actual capacitance is between 47nF and 200nF. A maximum 22Ω resistor can be placed in series with the bootstrap capacitor to reduce the SW pin's spike voltage.

If BST\_UVP is triggered, the BSTOK\_INT\_STATUS bit asserts and the /FS pin pulls low if BST protection is enabled.

### Serial Peripheral Interface (SPI)

The MPQ7210 features a four-wire SPI with a clock speed up to 4MHz. Ensure that the MCU and the MPQ7210 are on the same board, with a line that is as short as possible.

The interface is a four-wire SPI with SPI mode 3 (CPOL = CPHA = 1, the clock is idle high, sample data at the clock's first rising edge).

For standard SPI configurations, the /CS (chip select, active low), CK (sync clock), SI (MOSI, serial data input), and SO (MISO, serial data output) pins are used. The communication starts when /CS is pulled low by the SPI master and stops when the /CS pin pulls high. CK is also controlled by the SPI master. SI and SO are driven at the falling edge of CK and should be captured at the rising edge of CK. The /CS pin stays low while sending data.

The clock must be within the specified frequency range (≤4MHz).

Command and data are shifted with the least significant bit (LSB) first, and the most significant bit (MSB) last.

The SPI does not support back-to-back frame operation. After each SPI transfer, the /CS pin must go from low to high to low before the next SPI frame transfer starts. The minimum time between two SPI commands is one SPI clock cycle during which the /CS pin must remain high.

### Bit Encoding of the Command Byte

The first byte (command byte) transmitted at SI after /CS goes low contains address and command information. Table 2 shows the command byte arrangement. Bits[7:0] are the target register address, while bit[0] is command mode (two supported modes, where 0 is a single write and 1 is a single read).

Figure 7 on page 32 shows the SPI signal frame write/read.

**Table 2: Command Byte**

| D7   | D6 | D5 | D4 | D3 | D2 | D1 | D0  |
|------|----|----|----|----|----|----|-----|
| ADDR |    |    |    |    |    |    | CMD |

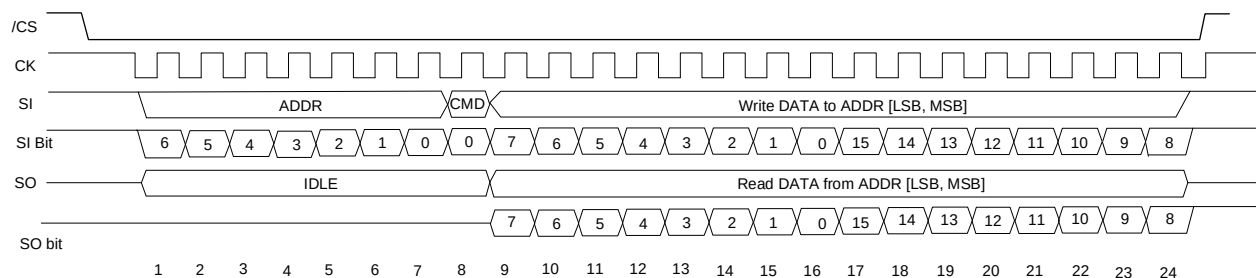


**Figure 7: SPI Signal Frame Write/Read**

Figure 8 shows the SPI frame signal write/read.

The read frame description is below:

The write frame description is below:

- SI: Received master {CMD (ADDR+CMD), W\_data [L], W\_data [H]}.
- SO: Stay idle.
- SI: Received master [CMD (ADDR+CMD)].
- SO: Transmit slave {R\_data [L], R\_data [H]}.

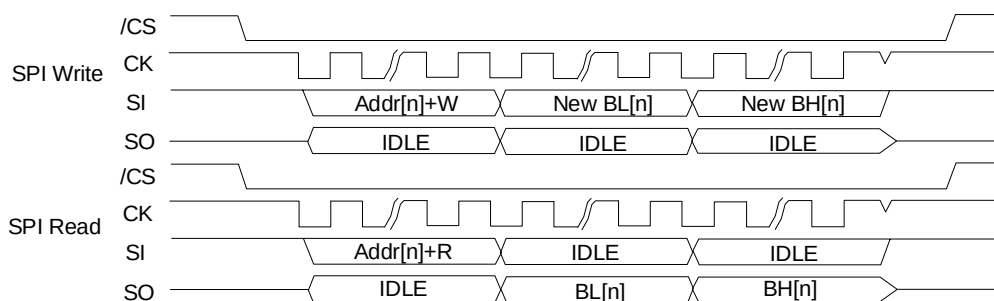


**Figure 8: SPI Frame Signal Write/Read**

## REGISTER MAP

| Register Name                        | R/W       | Addr. | Def  | D15                                               | D14            | D13                                              | D12                                               | D11                                                 | D10                                              | D9                                       | D8                                      | D7                                  | D6                                          | D5                                          | D4                                                      | D3                                                           | D2                                                      | D1        | D0 |  |                    |  |
|--------------------------------------|-----------|-------|------|---------------------------------------------------|----------------|--------------------------------------------------|---------------------------------------------------|-----------------------------------------------------|--------------------------------------------------|------------------------------------------|-----------------------------------------|-------------------------------------|---------------------------------------------|---------------------------------------------|---------------------------------------------------------|--------------------------------------------------------------|---------------------------------------------------------|-----------|----|--|--------------------|--|
| SIL_INF                              | R/W       | 0x01  | 0000 | OTP                                               | RSV            |                                                  |                                                   |                                                     |                                                  |                                          |                                         | SIL_INF                             |                                             |                                             |                                                         |                                                              |                                                         |           |    |  |                    |  |
| DEV_CFG                              | R/W       | 0x03  | 005A | RSV                                               |                |                                                  |                                                   |                                                     | PHASE                                            |                                          |                                         | DIM1_MODE                           |                                             | DIM2_MODE                                   |                                                         | DIM1_FREQ                                                    |                                                         | DIM2_FREQ |    |  |                    |  |
| PWM_DIM1                             | R/W       | 0x04  | 0000 | RSV                                               |                |                                                  |                                                   | PWM_DIM1_DUTY                                       |                                                  |                                          |                                         |                                     |                                             |                                             |                                                         |                                                              |                                                         |           |    |  |                    |  |
| PWM_DIM2                             | R/W       | 0x05  | 0000 | RSV                                               |                |                                                  |                                                   | PWM_DIM2_DUTY                                       |                                                  |                                          |                                         |                                     |                                             |                                             |                                                         |                                                              |                                                         |           |    |  |                    |  |
| ANA_DIM1                             | R/W       | 0x06  | 00C8 | RSV                                               |                |                                                  |                                                   |                                                     |                                                  |                                          |                                         | ANA_DIM1                            |                                             |                                             |                                                         |                                                              |                                                         |           |    |  |                    |  |
| ANA_DIM2                             | R/W       | 0x07  | 00C8 | RSV                                               |                |                                                  |                                                   |                                                     |                                                  |                                          |                                         | ANA_DIM2                            |                                             |                                             |                                                         |                                                              |                                                         |           |    |  |                    |  |
| INT_ALL                              | R         | 0x08  | 0000 | RSV                                               |                |                                                  |                                                   |                                                     |                                                  |                                          |                                         |                                     |                                             |                                             |                                                         |                                                              |                                                         |           |    |  | INT_ST<br>ATU<br>S |  |
| /FS_CFG                              | R/W       | 0x09  | 5551 | BUCK1_OCP_ACT                                     |                | BUCK2_OCP_ACT                                    |                                                   | BUCK1_UVP_ACT                                       |                                                  | BUCK2_UVP_ACT                            |                                         | RSV                                 |                                             | RSV                                         |                                                         | RSV                                                          |                                                         | TSD_ACT   |    |  |                    |  |
| /FS_INT_S<br>TATUS                   | R/W<br>1C | 0x0A  | 0000 | BUC<br>K1<br>OCP<br>_INT<br>_STA<br>TUS           | RSV            | BUC<br>K1_U<br>VP_I<br>NT_<br>STA<br>TUS         | BUC<br>K2_OCP<br>_INT<br>_STA<br>TUS              | RSV                                                 | BUC<br>K2_U<br>VP_I<br>NT_<br>STA<br>TUS         | PHA<br>SE_I<br>NT_<br>STA<br>TUS         | TWN<br>_INT<br>_STA<br>TUS              | TSD_<br>INT_<br>STAT<br>US          | BST1<br>_UV_<br>INT_<br>_STA<br>TUS         | BST2<br>_UV_<br>INT_<br>_STA<br>TUS         | OTP<br>_IND<br>_FAI<br>L_IN<br>T_ST<br>ATU<br>S         | OTP<br>_PR<br>OG_<br>FAI<br>L_IN<br>T_ST<br>ATU<br>S         | OTP<br>_CRC_<br>FAI<br>L_IN<br>T_ST<br>ATU<br>S         | RSV       |    |  |                    |  |
| /FS_INT_R<br>AW_STAT<br>US           | R         | 0x0B  | 0000 | BUC<br>K1_OCP<br>_INT_<br>_RA<br>W_S<br>TAT<br>US | RSV            | BUC<br>K1_U<br>VP_I<br>NT_<br>RAW<br>_STA<br>TUS | BUC<br>K2_OCP<br>_INT_<br>_RA<br>W_S<br>TAT<br>US | RSV                                                 | BUC<br>K2_U<br>VP_I<br>NT_<br>RAW<br>_STA<br>TUS | PHA<br>SE_I<br>NT_<br>RAW<br>_STA<br>TUS | TWN<br>_INT_<br>_RA<br>W_S<br>TAT<br>US | TSD_<br>INT_<br>_RAW<br>_STA<br>TUS | BST1<br>_UV_<br>INT_<br>_RAW<br>_STA<br>TUS | BST2<br>_UV_<br>INT_<br>_RAW<br>_STA<br>TUS | OTP<br>_IND<br>_FAI<br>L_IN<br>T_RA<br>W_S<br>TAT<br>US | OTP<br>_PR<br>OG_<br>FAI<br>L_IN<br>T_RA<br>W_S<br>TAT<br>US | OTP<br>_CRC_<br>FAI<br>L_IN<br>T_RA<br>W_S<br>TAT<br>US | RSV       |    |  |                    |  |
| /FS_INT_E<br>N                       | R/W       | 0x0C  | 93FC | BUC<br>K1_OCP<br>_EN                              | RSV            | BUC<br>K1_U<br>VP_<br>EN                         | BUC<br>K2_OCP<br>_EN                              | RSV                                                 | BUC<br>K2_U<br>VP_<br>EN                         | PHA<br>SE_I<br>NT_<br>EN                 | TWN<br>_INT<br>_EN                      | TSD_<br>_EN                         | BST1<br>_UV_<br>INT_<br>_EN                 | BST2<br>_UV_<br>INT_<br>_EN                 | OTP<br>_IND<br>_FAI<br>L_EN                             | OTP<br>_PR<br>OG_<br>FAI<br>L_EN                             | OTP<br>_CRC_<br>FAI<br>L_EN                             | RSV       |    |  |                    |  |
| /FS_INT_<br>MASK_EN                  | R/W       | 0x0D  | 0000 | BUC<br>K1_OCP<br>_INT_<br>_MA<br>SK_<br>EN        | RSV            | BUC<br>K1_U<br>VP_I<br>NT_<br>MAS<br>K_E<br>N    | BUC<br>K2_OCP<br>_INT_<br>_MA<br>SK_<br>EN        | RSV                                                 | BUC<br>K2_U<br>VP_I<br>NT_<br>MAS<br>K_E<br>N    | PHA<br>SE_I<br>NT_<br>MAS<br>K_E<br>N    | TWN<br>_INT_<br>_MA<br>SK_<br>EN        | TSD_<br>INT_<br>_MAS<br>K_E<br>N    | BST1<br>_UV_<br>INT_<br>_MAS<br>K_E<br>N    | BST2<br>_UV_<br>INT_<br>_MAS<br>K_E<br>N    | OTP<br>_JND<br>_FAI<br>L_IN<br>T_M<br>ASK_<br>EN        | OTP<br>_PR<br>OG_<br>FAI<br>L_IN<br>T_MA<br>SK_<br>EN        | OTP<br>_CRC_<br>FAI<br>L_IN<br>T_MA<br>SK_<br>EN        | RSV       |    |  |                    |  |
| /FS_INT_<br>REAL_TIM<br>E_STATU<br>S | R         | 0x0E  | 0000 | STA<br>TUS_<br>OC_P1                              | RSV            | STA<br>TUS_<br>UV_P1                             | STA<br>TUS_<br>OC_P2                              | RSV                                                 | STA<br>TUS_<br>UV_P2                             | STA<br>TUS_<br>TW_N                      | STA<br>TUS_<br>TS_D                     | RSV                                 |                                             |                                             |                                                         |                                                              |                                                         |           |    |  |                    |  |
| BUCK1_C<br>FG                        | R         | 0x10  | 001E | RSV                                               |                |                                                  |                                                   |                                                     |                                                  |                                          |                                         |                                     |                                             | BUCK1_FREQ_SEL                              |                                                         | BUC<br>K1_F<br>SS_<br>EN                                     | BUCK1_OCP_SEL                                           |           |    |  |                    |  |
| BUCK2_C<br>FG                        | R         | 0x11  | 001E | RSV                                               |                |                                                  |                                                   |                                                     |                                                  |                                          |                                         |                                     |                                             | BUCK2_FREQ_SEL                              |                                                         | BUC<br>K2_F<br>SS_<br>EN                                     | BUCK2_OCP_SEL                                           |           |    |  |                    |  |
| ADC_CTR<br>L                         | R/W       | 0x12  | 0500 | RSV                                               |                |                                                  |                                                   |                                                     |                                                  |                                          |                                         | CUR_STORED_CH                       |                                             |                                             | ADC<br>_RE<br>ADY                                       | TRIG<br>GER<br>_AD<br>C_R<br>EAD                             | ADC_INMUX                                               |           |    |  |                    |  |
| ADC_OUT                              | R         | 0x13  | 0000 | RSV                                               |                |                                                  |                                                   |                                                     |                                                  |                                          | ADC_DATA                                |                                     |                                             |                                             |                                                         |                                                              |                                                         |           |    |  |                    |  |
| BUCK_ST<br>ATUS                      | R         | 0x15  | 0000 | RSV                                               | DA_OTP<br>_RDY | OTP<br>_CR<br>C_E<br>RR_<br>FLA<br>G             | TRIM<br>_PA<br>GE_<br>CRC<br>_ER<br>R_FL<br>AG    | USE<br>R_P<br>AGE_<br>_CR<br>C_E<br>RR_<br>FLA<br>G | RSV                                              |                                          |                                         |                                     |                                             |                                             |                                                         |                                                              |                                                         |           |    |  |                    |  |
| BUCK_EN                              | R/W       | 0x20  | 0x00 | RSV                                               |                |                                                  |                                                   |                                                     |                                                  |                                          |                                         | BUC<br>K1_E<br>N                    |                                             |                                             |                                                         | BUC<br>K2_E<br>N                                             |                                                         |           |    |  |                    |  |

## REGISTER DESCRIPTION

### SIL\_REV (0x01)

**Default:** 0x0000

**POR:** N/A

The SIL\_REV command indicates whether OTP is complete, provides readout data, and returns the silicon information.

| Bits    | Access | Bit Name | Default | Description                                         |
|---------|--------|----------|---------|-----------------------------------------------------|
| D15     | R      | OTP      | 0       | When the device finishes OTP, this bit is set to 1. |
| D[14:8] | R      | RESERVED | 0       | Reserved. Always read as 0.                         |
| D[7:0]  | R      | SIL_INF  | 0       | Returns the silicon revision information.           |

### DEV\_CFG (0x03)

**Default:** 0x005A

**POR:** Load from the OTP

The DEV\_CFG command configures the part phase, PWM dimming mode, PWM dimming frequency.

| Bits     | Access | Bit Name  | Default | Description                                                                                                                                                                                                               |
|----------|--------|-----------|---------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| D[15:10] | R      | RESERVED  | 0       | Reserved. Always read as 0.                                                                                                                                                                                               |
| D[9:8]   | R      | PHASE     | 0       | Selects the phase (dual-phase or single-phase). Read-only after loading the OTP. If the part is set to 01 or 10 via the OTP, the part does not operate.<br>00: Dual-phase<br>01, 10: Error<br>11: Single-phase            |
| D[7:6]   | R/W    | DIM1_MODE | 01      | Configures buck 1's dimming mode. See the Pulse-Width Modulation (PWM) Dimming section on page 27 for more details.<br>00: PWM dimming mode 1<br>01: PWM dimming mode 3<br>10, 11: PWM dimming mode 2, follow the DIM pin |
| D[5:4]   | R/W    | DIM2_MODE | 01      | Configures buck 2's dimming mode. See the Pulse-Width Modulation (PWM) Dimming section on page 27 for more details.<br>00: PWM dimming mode 1<br>01: PWM dimming mode 3<br>10, 11: PWM dimming mode 2, follow the DIM pin |
| D[3:2]   | R/W    | DIM1_FREQ | 10      | Configures buck 1's dimming frequency.<br>00: 125Hz<br>01: 250Hz<br>10: 500Hz<br>11: 1kHz                                                                                                                                 |
| D[1:0]   | R/W    | DIM2_FREQ | 10      | Configures buck 2's dimming frequency.<br>00: 125Hz<br>01: 250Hz<br>10: 500Hz<br>11: 1kHz                                                                                                                                 |

### PWM\_DIM1 (0x04)

**Default:** 0x0000

**POR:** Load from the OTP

The PWM\_DIM1 command configures buck 1's PWM dimming duty cycle.

| Bits     | Access | Bit Name  | Default | Description                                                                                                                                                                                                                 |
|----------|--------|-----------|---------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| D[15:12] | R      | RESERVED  | 0       | Reserved. Always read as 0.                                                                                                                                                                                                 |
| D[11:0]  | R/W    | DIM1_DUTY | 0       | Configures buck 1's PWM dimming duty cycle. The duty cycle is $(x / 4095)$ , where $x$ is the register value, which can be set between 0 and 0xFFF via the OTP in the factory, or it can be changed on the fly via the SPI. |

### PWM\_DIM2 (0x05)

**Default:** 0x0000

**POR:** Load from the OTP

The PWM\_DIM2 command configures buck 2's PWM dimming duty cycle.

| Bits     | Access | Bit Name  | Default | Description                                                                                                                                                                                                                 |
|----------|--------|-----------|---------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| D[15:12] | R      | RESERVED  | 0       | Reserved. Always read as 0.                                                                                                                                                                                                 |
| D[11:0]  | R/W    | DIM2_DUTY | 0       | Configures buck 2's PWM dimming duty cycle. The duty cycle is $(x / 4095)$ , where $x$ is the register value, which can be set between 0 and 0xFFF via the OTP in the factory, or it can be changed on the fly via the SPI. |

### ANA\_DIM1 (0x06)

**Default:** 0x00C8

**POR:** Load from the OTP

The ANA\_DIM1 command configures buck 1's analog dimming reference voltage.

| Bits    | Access | Bit Name | Default | Description                                                                                                                                                                                                                                                                                                                                                |
|---------|--------|----------|---------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| D[15:8] | R      | RESERVED | 0       | Reserved. Always read as 0.                                                                                                                                                                                                                                                                                                                                |
| D[7:0]  | R/W    | ANA_DIM1 | 0xC8    | Configures buck 1's analog dimming setting. When the 0x06 register is set to 0xC8, the reference voltage is 0.2V. The voltage on the sensing resistor is $(N / 200 \times 200\text{mV})$ , where $N$ is the register value, which can be set between 0 and 255 via the OTP in the factory, or changed on the fly via the SPI. The minimum voltage is 10mV. |

### ANA\_DIM2 (0x07)

**Default:** 0x00C8

**POR:** Load from the OTP

The ANA\_DIM2 command configures the part buck 2 analog dimming reference voltage.

| Bits    | Access | Bit Name | Default | Description                                                                                                                                                                                                                                                                                                                                                |
|---------|--------|----------|---------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| D[15:8] | R      | RESERVED | 0       | Reserved. Always read as 0.                                                                                                                                                                                                                                                                                                                                |
| D[7:0]  | R/W    | ANA_DIM2 | 0xC8    | Configures buck 2's analog dimming setting. When the 0x07 register is set to 0xC8, the reference voltage is 0.2V. The voltage on the sensing resistor is $(N / 200 \times 200\text{mV})$ , where $N$ is the register value, which can be set between 0 and 255 via the OTP in the factory, or changed on the fly via the SPI. The minimum voltage is 10mV. |

### INT\_ALL (0x08)

**Default:** 0x0000

**POR:** N/A

The INT\_ALL command indicates the device's interruption status. If any interruption is triggered, bit[0] flags 1.

| Bits    | Access | Bit Name   | Default | Description                                                                                                                      |
|---------|--------|------------|---------|----------------------------------------------------------------------------------------------------------------------------------|
| D[15:1] | R      | RESERVED   | 0       | Reserved. Always read as 0.                                                                                                      |
| D0      | R      | INT_STATUS | 0       | Indicates the /FS interruption status.<br>0: No interruption events; /FS is high<br>1: There are interruption events; /FS is low |

### INT\_CFG (0x09)

**Default:** 0x5551

**POR:** N/A

The INT\_CFG command configures the device's action for I<sub>L</sub> over-current protection (OCP), V<sub>OUT</sub> under-voltage protection (UVP), and thermal shutdown (TSD). Typically, the device can be configured for no action, hiccup, and latch-off mode.

| Bits     | Access | Bit Name      | Default | Description                                                                                                |
|----------|--------|---------------|---------|------------------------------------------------------------------------------------------------------------|
| D[15:14] | R/W    | BUCK1_OCP_ACT | 01      | Sets buck 1's OCP response.<br>00: Latch-off mode<br>01: Hiccup mode<br>10, 11: No action                  |
| D[13:12] | R/W    | BUCK2_OCP_ACT | 01      | Sets buck 2's OCP response.<br>00: Latch-off mode<br>01: Hiccup mode<br>10, 11: No action                  |
| D[11:10] | R/W    | BUCK1_UVP_ACT | 01      | Sets buck 1's V <sub>OUT</sub> UVP response.<br>00: Latch-off mode<br>01: Hiccup mode<br>10, 11: No action |
| D[9:8]   | R/W    | BUCK2_UVP_ACT | 01      | Sets buck 2's V <sub>OUT</sub> UVP response.<br>00: Latch-off mode<br>01: Hiccup mode<br>10, 11: No action |
| D[7:6]   | R/W    | RESERVED      | 01      | Reserved. Always read as 01.                                                                               |
| D[5:4]   | R/W    | RESERVED      | 01      | Reserved. Always read as 01.                                                                               |
| D[3:2]   | R      | RESERVED      | 0       | Reserved. Always read as 0.                                                                                |
| D[1:0]   | R/W    | TSD           | 01      | Sets the thermal shutdown response.<br>00: Latch-off mode<br>01: Hiccup mode<br>10, 11: No action          |

## /FS\_INT\_STATUS (0x0A)

**Default:** 0x0000

**POR:** N/A

The /FS\_INT\_STATUS command indicates if the following occur: over-current protection (OCP), under-voltage protection (UVP), thermal warning (TW), thermal shutdown (TSD), BST UV, and one-time programmable (OTP) error interruption. If any interruption occurs, an /FS interruption status register flag is set to 1 and the /FS pin pulls low if the interruption mask is disabled. When writing 1 to this register, the interruption flag is cleared after the interruption condition is removed. The user can read this register to obtain the information if there is an interruption.

| Bits   | Access | Bit Name                 | Default | Description                                                               |
|--------|--------|--------------------------|---------|---------------------------------------------------------------------------|
| D[15]  | R/W1C  | BUCK1_OCP_INT_STATUS     | 0       | Indicates buck 1's OCP interruption status.                               |
| D[14]  | R      | RESERVED                 | 0       | Reserved. Always read as 0.                                               |
| D[13]  | R/W1C  | BUCK1_UVP_INT_STATUS     | 0       | Indicates buck 1's output UVP interruption status.                        |
| D[12]  | R/W1C  | BUCK2_OCP_INT_STATUS     | 0       | Indicates buck 2's OCP interruption status.                               |
| D[11]  | R      | RESERVED                 | 0       | Reserved. Always read as 0.                                               |
| D[10]  | R/W1C  | BUCK2_UVP_INT_STATUS     | 0       | Indicates buck 2's output UVP interruption status.                        |
| D[9]   | R/W1C  | PHASE_INT_STATUS         | 0       | Indicates the phase control's safety error interruption status.           |
| D[8]   | R/W1C  | TWN_INT_STATUS           | 0       | Indicates the TW interruption status.                                     |
| D[7]   | R/W1C  | TSD_INT_STATUS           | 0       | Indicates the TSD interruption status.                                    |
| D[6]   | R/W1C  | BST1_UV_INT_STATUS       | 0       | Indicates the interrupt status for whether buck 1's boot voltage is okay. |
| D[5]   | R/W1C  | BST2_UV_INT_STATUS       | 0       | Indicates the interrupt status for whether buck 2's boot voltage is okay. |
| D[4]   | R/W1C  | OTP_IND_FAIL_INT_STATUS  | 0       | Indicates an OTP failure interruption status.                             |
| D[3]   | R/W1C  | OTP_PROG_FAIL_INT_STATUS | 0       | Indicates an OTP failure after the OTP is programmed.                     |
| D[2]   | R/W1C  | OTP_CRC_FAIL_INT_STATUS  | 0       | Indicates the OTP CRC failure interruption status.                        |
| D[1:0] | RSV    | RESERVED                 | 0       | Reserved. Always read as 0.                                               |

## /FS\_INT\_RAW\_STATUS (0x0B)

**Default:** 0x0000

**POR:** N/A

The /FS\_INT\_RAW\_STATUS command indicates if an error interruption occurs if any of the following interrupts are enabled: over-current protection (OCP), under-voltage protection (UVP), thermal warning (TW), thermal shutdown (TSD), BST UV, and one-time programmable (OTP) error. If any interruption occurs, the related register bit is flagged as 1. The related interruption bit is flagged only if the related interruption is enabled.

| Bits  | Access | Bit Name                 | Default | Description                                            |
|-------|--------|--------------------------|---------|--------------------------------------------------------|
| D[15] | R      | BUCK1_OCP_INT_RAW_STATUS | 0       | Indicates buck 1's OCP interruption raw status.        |
| D[14] | R      | RESERVED                 | 0       | Reserved. Always read as 0.                            |
| D[13] | R      | BUCK1_UVP_INT_RAW_STATUS | 0       | Indicates buck 1's output UVP interruption raw status. |

|        |     |                              |   |                                                                     |
|--------|-----|------------------------------|---|---------------------------------------------------------------------|
| D[12]  | R   | BUCK2_OCP_INT_RAW_STATUS     | 0 | Indicates buck 2's OCP interruption raw status.                     |
| D[11]  | R   | RESERVED                     | 0 | Reserved. Always read as 0.                                         |
| D[10]  | R   | BUCK2_UVP_INT_RAW_STATUS     | 0 | Indicates buck 2's output UVP interruption raw status.              |
| D[9]   | R   | PHASE_INT_RAW_STATUS         | 0 | Indicates the phase control's safety error interruption raw status. |
| D[8]   | R   | TWN_INT_RAW_STATUS           | 0 | Indicates the TW interruption raw status.                           |
| D[7]   | R   | TSD_INT_RAW_STATUS           | 0 | Indicates the TSD interruption raw status.                          |
| D[6]   | R   | BST1_UV_INT_RAW_STATUS       | 0 | Indicates buck 1's BST UV interruption raw status.                  |
| D[5]   | R   | BST2_UV_INT_RAW_STATUS       | 0 | Indicates buck 2's BST UV interruption raw status.                  |
| D[4]   | R   | OTP_IND_FAIL_INT_RAW_STATUS  | 0 | Indicates an OTP failure interruption raw status.                   |
| D[3]   | R   | OTP_PROG_FAIL_INT_RAW_STATUS | 0 | Indicates an OTP failure after the OTP is programmed.               |
| D[2]   | R   | OTP_CRC_FAIL_INT_RAW_STATUS  | 0 | Indicates the OTP CRC failure interruption raw status.              |
| D[1:0] | RSV | RESERVED                     | 0 | Reserved. Always read as 0.                                         |

### **/FS\_INT\_EN (0x0C)**

**Default:** 0x93FC

**POR:** Load from the OTP

The /FS\_INT\_EN command enables the following interruptions: over-current protection (OCP), under-voltage protection (UVP), thermal warning (TW), thermal shutdown (TSD), BST UV, and one-time programmable (OTP) error. If the related protection is enable, the part will act as the INT\_CFG configuration.

| Bits  | Access | Bit Name     | Default | Description                                                                           |
|-------|--------|--------------|---------|---------------------------------------------------------------------------------------|
| D[15] | R/W    | BUCK1_OCP_EN | 1       | 0: Disable buck 1 OCP<br>1: Enable buck 1 OCP                                         |
| D[14] | R      | RESERVED     | 0       | Reserved. Always read as 0.                                                           |
| D[13] | R/W    | BUCK1_UVP_EN | 0       | 0: Disable buck 1 output UVP<br>1: Enable buck 1 output UVP                           |
| D[12] | R/W    | BUCK2_OCP_EN | 1       | 0: Disable buck 2 OCP<br>1: Enable buck 2 OCP                                         |
| D[11] | R/W    | RESERVED     | 0       | Reserved. Always read as 0.                                                           |
| D[10] | R/W    | BUCK2_UVP_EN | 0       | 0: Disable buck 2 output UVP<br>1: Enable buck 2 output UVP                           |
| D[9]  | R/W    | PHASE_EN     | 1       | 0: Disable the phase control safety error<br>1: Enable the phase control safety error |
| D[8]  | R/W    | TWN_EN       | 1       | 0: Disable the TW interruption<br>1: Enable the TW interruption                       |
| D[7]  | R/W    | TSD_EN       | 1       | 0: Disable TSD interruption<br>1: Enable TSD interruption                             |
| D[6]  | R/W    | BST1_UV_EN   | 1       | 0: Disable buck 1's BST UV interruption<br>1: Enable buck 1's BST UV interruption     |
| D[5]  | R/W    | BST2_UV_EN   | 1       | 0: Disable buck 2's BST UV interruption<br>1: Enable buck 2's BST UV interruption     |

|        |     |                  |   |                                                                                                                    |
|--------|-----|------------------|---|--------------------------------------------------------------------------------------------------------------------|
| D[4]   | R/W | OTP_IND_FAIL_EN  | 1 | 0: Turn off the OTP indicator interruption status<br>1: Turn on the OTP indicator interruption status              |
| D[3]   | R/W | OTP_PROG_FAIL_EN | 1 | 0: Turn off the OTP program failure interruption status<br>1: Turn off the OTP program failure interruption status |
| D[2]   | R/W | OTP_CRC_FAIL_EN  | 1 | 0: Turn off the OTP CRC failure interruption status<br>1: Turn on the OTP CRC failure interruption status          |
| D[1:0] | RSV | RESERVED         | 0 | Reserved. Always read as 0.                                                                                        |

**/FS\_INT\_MASK\_EN (0x0D)**

**Default:** 0x0000

**POR:** Load from the OTP

The /FS\_INT\_MASK\_EN command masks the following interruptions: over-current protection (OCP), under-voltage protection (UVP), thermal warning (TW), thermal shutdown (TSD), BST UV, and one-time programmable (OTP) error. If the related interruption fault flag mask is enabled, the fault register flag is not set to 1, even if the interruption is triggered. This register can only be configured via the SPI on the fly; it cannot be configured via the OTP.

| Bits   | Access | Bit Name                  | Default | Description                                                                                                               |
|--------|--------|---------------------------|---------|---------------------------------------------------------------------------------------------------------------------------|
| D[15]  | R/W    | BUCK1_OCP_INT_MASK_EN     | 0       | 0: Disable buck 1's OCP interruption mask<br>1: Enable buck 1's OCP interruption mask                                     |
| D[14]  | R      | RESERVED                  | 0       | Reserved. Always read as 0.                                                                                               |
| D[13]  | R/W    | BUCK1_UVP_INT_MASK_EN     | 0       | 0: Disable buck 1's UV interruption mask<br>1: Enable buck 1's UV interruption mask                                       |
| D[12]  | R/W    | BUCK2_OCP_INT_MASK_EN     | 0       | 0: Disable buck 2's OCP interruption mask<br>1: Enable buck 2's OCP interruption mask                                     |
| D[11]  | R/W    | RESERVED                  | 0       | Reserved. Always read as 0.                                                                                               |
| D[10]  | R/W    | BUCK2_UVP_INT_MASK_EN     | 0       | 0: Disable buck 2's UV interruption mask<br>1: Enable buck 2's UV interruption mask                                       |
| D[9]   | R/W    | PHASE_INT_MASK_EN         | 0       | 0: Disable the phase control safety error interruption mask<br>1: Enable the phase control safety error interruption mask |
| D[8]   | R/W    | TW_INT_MASK_EN            | 0       | 0: Disable the TW interruption mask<br>1: Enable the TW interruption mask                                                 |
| D[7]   | R/W    | TSD_INT_MASK_EN           | 0       | 0: Disable the TSD interruption mask<br>1: Enable the TSD interruption mask                                               |
| D[6]   | R/W    | BST1_UV_INT_MASK_EN       | 0       | 0: Disable buck 1's BST UV interruption mask<br>1: Enable buck 1's BST UV interruption mask                               |
| D[5]   | R/W    | BST2_UV_INT_MASK_EN       | 0       | 0: Disable buck 2's BST UV interruption mask<br>1: Enable buck 2's BST UV interruption mask                               |
| D[4]   | R/W    | OTP_IND_FAIL_EN           | 0       | 0: Disable the OTP indicator interruption mask<br>1: Enable the OTP indicator interruption mask                           |
| D[3]   | R/W    | OTP_PROG_FAIL_INT_MASK_EN | 0       | 0: Disable the OTP program failure interruption mask<br>1: Enable the OTP program failure interruption mask               |
| D[2]   | R/W    | OTP_CRC_FAIL_INT_MASK_EN  | 0       | 0: Disable the OTP CRC failure interruption mask<br>1: Enable the OTP CRC failure interruption mask                       |
| D[1:0] | RSV    | RESERVED                  | 0       | Reserved. Always read as 0.                                                                                               |

## /FS\_INT\_REAL\_TIME\_STATUS (0x0E)

**Default:** 0x0000

**POR:** N/A

The /FS\_REAL\_TIME\_STATUS command indicates the real-time status of the following interrupts: over-current protection (OCP), under-voltage protection (UVP), thermal warning (TW), and thermal shutdown (TSD). If the interrupt condition is removed, the related bit returns to 0.

| Bits   | Access | Bit Name         | Default | Description                               |
|--------|--------|------------------|---------|-------------------------------------------|
| D[15]  | R      | BUCK1_OCP_STATUS | 0       | Indicates buck 1's live OCP status.       |
| D[14]  | R      | RESERVED         | 0       | Reserved. Always read as 0.               |
| D[13]  | R      | BUCK1_UVP_STATUS | 0       | Indicates buck 1's live output UV status. |
| D[12]  | R      | BUCK2_OCP_STATUS | 0       | Indicates buck 2's live OCP status.       |
| D[11]  | R      | RESERVED         | 0       | Reserved. Always read as 0.               |
| D[10]  | R      | BUCK2_UVP_STATUS | 0       | Indicates buck 2's live output UV status. |
| D[9]   | R      | TW_STATUS        | 0       | Indicates the real-time TW status.        |
| D[8]   | R      | TSD_STATUS       | 0       | Indicates the real-time TSD status.       |
| D[7:0] | RSV    | RESERVED         | 0       | Reserved. Always read as 0.               |

## BUCK1\_CFG (0x10)

**Default:** 0x001E

**POR:** Load from the OTP

The BUCK1\_CFG command configures buck 1's switching frequency, frequency spread spectrum (FSS), and high-side (HS) current limit. The switching frequency and FSS can only be configured via the OTP. The current limit can be configured via the OTP in the factory or via the SPI on the fly. The current limit prevents current runaway, and it can limit the current through the LED.

| Bits    | Access | Bit Name       | Default | Description                                                                                                                                    |
|---------|--------|----------------|---------|------------------------------------------------------------------------------------------------------------------------------------------------|
| D[15:6] | RSV    | RESERVED       | 0       | Reserved. Always read as 0.                                                                                                                    |
| D[5:4]  | R      | BUCK1_FREQ_SEL | 01      | Sets buck 1's switching frequency selection. Read-only after the OTP finishes loading.<br>00: 220kHz<br>01: 420kHz<br>10: 1.1MHz<br>11: 2.3MHz |
| D[3]    | R      | BUCK1_FSS_EN   | 1       | Enables FSS. Read-only after the OTP finishes loading.<br>0: Disabled<br>1: Enabled                                                            |
| D[2:0]  | R      | BUCK1_OCP_SEL  | 110     | Sets the HS current limit.<br>000: 500mA<br>001: 1A<br>010: 1.5A<br>011: 2A<br>100: 2.5A<br>101: 3A<br>110: 3.5A<br>111: 4A                    |

**BUCK2\_CFG (0x11)**
**Default:** 0x001E

**POR:** Load from the OTP

The BUCK2\_CFG command configures the buck 2 switching frequency, frequency spread spectrum (FSS), and high-side (HS) current limit. The switching frequency and FSS can only be configured via the OTP. The current limit can be configured via the OTP in the factory or via the SPI on the fly. The current limit prevents current runaway, and it can limit the current through the LED.

| Bits    | Access | Bit Name       | Default | Description                                                                                                                                    |
|---------|--------|----------------|---------|------------------------------------------------------------------------------------------------------------------------------------------------|
| D[15:6] | RSV    | RESERVED       | 0       | Reserved. Always read as 0.                                                                                                                    |
| D[5:4]  | R      | BUCK2_FREQ_SEL | 01      | Sets buck 2's switching frequency selection. Read-only after the OTP finishes loading.<br>00: 220kHz<br>01: 420kHz<br>10: 1.1MHz<br>11: 2.3MHz |
| D[3]    | R      | BUCK2_FSS_EN   | 1       | Enables FSS. Read-only after the OTP finishes loading.<br>0: Disabled<br>1: Enabled                                                            |
| D[2:0]  | R      | BUCK2_OCP_SEL  | 110     | Sets the HS current limit.<br>000: 500mA<br>001: 1A<br>010: 1.5A<br>011: 2A<br>100: 2.5A<br>101: 3A<br>110: 3.5A<br>111: 4A                    |

**ADC\_CTRL (0x12)**
**Default:** 0x0000

**POR:** Load from the OTP

The ADC\_CTRL command configures the ADC-related information. CUR\_STORED\_CH records the current-sensing channel information and ADC\_READY indicates whether the ADC is idle. TRIG\_ADC\_READ triggers the ADC reading signal. ADC\_INMUX selects which signal the ADC will read. The ADC can read one channel at a time and the reading process is triggered by writing 1 to TRIG\_ADC\_READ.

| Bit     | Access | Bit Name      | Default | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                 |
|---------|--------|---------------|---------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| D[15:8] | RSV    | RESERVED      | 5       | Reserved. Always read as 0x05.                                                                                                                                                                                                                                                                                                                                                                                                                              |
| D[7:5]  | R      | CUR_STORED_CH | 0       | Records the current stored in the ADC-sensing channel to check what software is set for the ADC-sensing channel. ADC_INMUX selects which signal the ADC reads.<br>000: CH1, buck 1 input :V <sub>IN1</sub><br>001: CH2, buck 1 output: V <sub>OUT1</sub><br>010: CH3, buck 2 input :V <sub>IN2</sub><br>011: CH4, buck 2 output: V <sub>OUT2</sub><br>100: CH5, VCC voltage: V <sub>CC</sub><br>101: Part temperature: T <sub>J</sub><br>110, 111: Not used |

|        |     |               |     |                                                                                                                                                                                                                                                                                                                                  |
|--------|-----|---------------|-----|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| D[4]   | R   | ADC_READY     | 0   | Returns the ADC ready signal.<br>1: The ADC is ready to be triggered to read new values, or the readout value from the ADC is available<br>0: The ADC is busy                                                                                                                                                                    |
| D[3]   | R/W | TRIG_ADC_READ | 0   | Triggers the ADC to start reading. This bit automatically returns to 0 when reading is finished. Write 1 to this bit to start ADC reading.                                                                                                                                                                                       |
| D[2:0] | R/W | ADC_INMUX     | 000 | Selects which signal the ADC reads.<br>000: CH1, buck 1 input :V <sub>IN1</sub><br>001: CH2, buck 1 output: V <sub>OUT1</sub><br>010: CH3, buck 2 input :V <sub>IN2</sub><br>011: CH4, buck 2 output: V <sub>OUT2</sub><br>100: CH5, VCC voltage: V <sub>CC</sub><br>101: Part temperature: T <sub>J</sub><br>110, 111: Not used |

### ADC\_DATA (0x13)

**Default:** 0x0000

**POR:** N/A

The ADC\_DATA command stores the ADC readout data. The ADC\_DATA is refreshed once another command from register 0x12, bit D[3] (TRIG\_ADC\_READ) write 1 is finished.

| Bits     | Access | Bit Name | Default | Description                  |
|----------|--------|----------|---------|------------------------------|
| D[15:10] | RSV    | RESERVED | 0       | Reserved. Always read as 0.  |
| D[9:0]   | R      | ADC_DATA | 0       | Returns the 10-bit ADC data. |

### OTP\_STATUS (0x15)

**Default:** 0x0000

**POR:** N/A

The OTP\_STATUS command stores the device's OTP information.

| Bits    | Access | Bit Name               | Default | Description                                                                                                                              |
|---------|--------|------------------------|---------|------------------------------------------------------------------------------------------------------------------------------------------|
| D[15]   | RSV    | RESERVED               | 0       | Reserved. Always read as 0.                                                                                                              |
| D[14]   | R      | DA_OTP_RDY             | 0       | 1: OTP reading to digital is complete<br>0: OTP reading to digital is not complete                                                       |
| D[13]   | R      | OTP_CRC_ERR_FLAG       | 0       | Indicates the OTP CRC result.<br>1: OTP CRC error<br>0: No OTP CRC error                                                                 |
| D[12]   | R      | TRIM_PAGE_CRC_ERR_FLAG | 0       | Indicates the OTP CRC result of a trimmed page.<br>1: There is a trimmed page OTP CRC error<br>0: There is no trimmed page OTP CRC error |
| D[11]   | R      | USER_PAGE_CRC_ERR_FLAG | 0       | Indicates the user page OTP CRC result.<br>1: OTP CRC error<br>0: No OTP CRC error                                                       |
| D[10:0] | RSV    | RESERVED               | 0       | Reserved. Always read as 0.                                                                                                              |

## BUCK\_EN (0x20)

**Default:** 0x0000

**POR:** Load from the OTP

The BUCK\_EN command controls buck 1 and buck 2's on/off information.

| Bits    | Access | Bit Name | Default | Description                                  |
|---------|--------|----------|---------|----------------------------------------------|
| D[15:8] | RSV    | RESERVED | 0       | Reserved. Always read as 0.                  |
| D[7]    | R/W    | BUCK1_EN | 0       | Enables buck 1.<br>0: Enabled<br>1: Disabled |
| D[6:4]  | RSV    | RESERVED | 0       | Reserved. Always read as 0.                  |
| D[3]    | R/W    | BUCK2_EN | 0       | Enables buck 2.<br>0: Enabled<br>1: Disabled |
| D[2:0]  | RSV    | RESERVED | 0       | Reserved. Always read as 0.                  |

## APPLICATION INFORMATION

### Setting the LED Current

The external resistor connected between the ISP<sub>x</sub> and ISN<sub>x</sub> pins sets I<sub>LED</sub>. Select the sensing resistor package based on the power dissipation. I<sub>LED</sub> can be estimated with Equation (6):

$$I_{LED} (A) = \frac{0.2}{R_{SEN} (\Omega)} \quad (6)$$

V<sub>REF</sub> (0.2V) can also be adjusted via the SPI by changing the analog dimming register 0x06, bits[7:0], which means V<sub>REF</sub> can be adjusted from 10mV to 255mV.

### Dimming Mode Selection

The dimming mode can be configured via register 0x03. There are three dimming modes; for more details, see the Pulse-Width Modulation (PWM) Dimming section on page 27. The dimming mode should work with DIM pin to initialize the IC.

For example, if the PWM dimming mode is set to PWM dimming mode 3, pull the DIM pin low and set the internal PWM dimming duty cycle to 0%. After VIN, VCC, and EN pull high, the initial current is 0A; the current can be changed via the SPI's analog dimming and PWM dimming registers.

### Selecting the Switching Frequency (f<sub>sw</sub>)

f<sub>sw</sub> can be set to 220kHz, 420kHz, 1.1MHz, or 2.3MHz via the OTP. A higher f<sub>sw</sub> can reduce the inductance and capacitance, but it increases power loss and may result in thermal issues. High-frequency operation is recommended for applications with a low LED current. The thermal and cooling conditions should be validated on a system level.

### Selecting the Inductor

For most applications, use an inductor with an inductance between 2.2μH and 330μH and a DC current rating higher than the maximum inductor current. Include the inductor's DC resistance when estimating the output current and the inductor's power consumption.

For buck converter designs, calculate the required inductance with Equation (7):

$$L = \frac{V_{OUT} \times (V_{IN} - V_{OUT})}{V_{IN} \times \Delta I_L \times f_{SW}} \quad (7)$$

Choose the inductor ripple current to be 10% to 30% of the LED current. The inductor peak current can be calculated with Equation (8):

$$I_{L\_PEAK} = I_{L\_AVG} + \frac{\Delta I_L}{2} \quad (8)$$

Where I<sub>L\_AVG</sub> is the average current through the inductor. I<sub>L\_AVG</sub> is equal to the output load current (I<sub>LED</sub>) for buck applications. Under low-I<sub>LED</sub> conditions, use a larger-value inductor to prevent the part from entering DCM.

### Selecting the Input Capacitor

The step-down converter has a discontinuous input current in buck or buck-boost mode, and requires a capacitor to supply AC current to the converter while maintaining the DC input voltage. For the best performance, use low-ESR capacitors. Ceramic capacitors with X7R dielectrics are highly recommended because of their low ESR and small temperature coefficients.

For most applications, use a 4.7μF to 22μF capacitor. The input capacitor can be electrolytic, tantalum, or ceramic. When using electrolytic or tantalum capacitors, it is strongly recommended to use another lower-value capacitor (e.g. 0.1μF) with a small package size (0603) to absorb high-frequency switching noise. Place the smaller capacitor as close as possible to VIN and GND.

In buck mode, since the input capacitor (C<sub>IN</sub>) absorbs the input switching current, it requires an adequate ripple current rating. The RMS current in the input capacitor can be estimated with Equation (9):

$$I_{CIN} = I_{LOAD} \times \sqrt{\frac{V_{OUT}}{V_{IN}} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right)} \quad (9)$$

The worst-case condition occurs at V<sub>IN</sub> = 2 × V<sub>OUT</sub>, calculated with Equation (10):

$$I_{CIN} = \frac{I_{LOAD}}{2} \quad (10)$$

For simplification, choose an input capacitor with an RMS current rating greater than half of the maximum load current.

The input voltage ripple caused by the capacitance can be estimated with Equation (11):

$$\Delta V_{IN} = \frac{I_{LOAD}}{f_{SW} \times C_{IN}} \times \frac{V_{OUT}}{V_{IN}} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \quad (11)$$

### Selecting the Output Capacitor

The output capacitor maintains the DC output voltage. Ceramic, tantalum, or low-ESR electrolytic capacitors are recommended. For the best results, use low-ESR capacitors to keep the output voltage ripple low.

In buck mode, the output voltage ripple can be calculated with Equation (12):

$$\Delta V_{OUT} = \frac{V_{OUT}}{f_{SW} \times L} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \times \left(R_{ESR} + \frac{1}{8 \times f_{SW} \times C_{OUT}}\right) \quad (12)$$

Where L is the inductance, and  $R_{ESR}$  is the equivalent series resistance (ESR) of the output capacitor. For ceramic capacitors, the capacitance dominates the impedance at the switching frequency, and causes the majority of the output voltage ripple. For simplification, the output voltage ripple can be estimated with Equation (13):

$$\Delta V_{OUT} = \frac{V_{OUT}}{8 \times f_{SW}^2 \times L \times C_{OUT}} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \quad (13)$$

For tantalum or electrolytic capacitors, the ESR dominates the impedance at the switching frequency. For simplification, the output ripple can be calculated with Equation (14):

$$\Delta V_{OUT} = \frac{V_{OUT}}{f_{SW} \times L} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \times R_{ESR} \quad (14)$$

To meet the shunt FET dimming and LED matrix manager device application requirements,  $V_{OUT}$  must have a fast transient speed. A large output capacitance means it will take too long to charge  $V_{OUT}$  up to high. When the output is shorted, the output capacitor's energy bypasses through the shunt FET. The FET may be damaged if the capacitance is too high and the slew rate is too fast. For these scenarios, a 100nF to 1μF capacitor is recommended.

### Selecting the VCC Capacitor

The device is powered by an external 5V supply connected to the VCC pin. Operation is enabled when  $V_{CC}$  exceeds its rising threshold (typically 4.2V) and is disabled when  $V_{CC}$  drops below the

falling threshold (typically 4V). The bypass capacitor from VCC to GND must have a capacitance 10 times greater than the bootstrap capacitance ( $C_{BST}$ ) to support proper operation during PWM dimming. When choosing the VCC capacitor, select a capacitor between 1μF and 10μF. For most applications, use a 4.7μF/10V, X7R capacitor. A low-dropout (LDO) regulator with >10mA current ability is required to power VCC.

### Selecting the BST Resistor and Capacitor

It is recommended to place a resistor in series with  $C_{BST}$  to reduce the SW spike voltage. A higher resistance improves SW spike reduction, but it compromises efficiency. The recommended external  $C_{BST}$  is a ceramic capacitor between 22nF and 220nF with a 10V or 16V DC derating. A maximum 20Ω resistor with a 0603/0402 package is recommended for efficiency and EMI performance.

### Output Short Circuits

The voltage transient on the ISP<sub>x</sub> and ISN<sub>x</sub> inputs during a short circuit is dependent on the output capacitance and the cable harness impedance. The inductance associated with a long cable harness resonates with the charge stored on the output capacitor, which forces the ISP<sub>x</sub> and ISN<sub>x</sub> voltages to ring below ground. The negative voltage and current are dependent on the parasitic cable harness's inductance and resistance.

When using a long cable harness, a diode is recommended to clamp the negative voltage across the ISP<sub>x</sub> and ISN<sub>x</sub> inputs (see Figure 9).

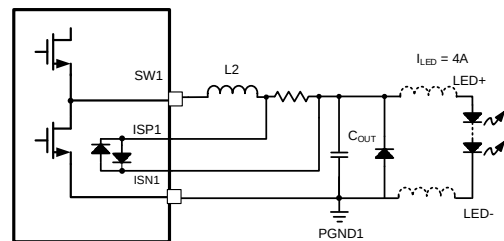


**Figure 9: Transient Protection Using an External Diode**

Place the diode close to the output capacitor and ensure that the current flowing through the ISP<sub>x</sub> and ISN<sub>x</sub> nodes under negative transient conditions is below the absolute maximum rating of the device.

It is recommended to use a low forward voltage Schottky diode or a fast recovery silicon diode with a reverse blocking voltage rating greater than the maximum output voltage.

If an output short occurs, a UV condition is detected, and the device responds based on the selected UVP action.

### LED Open Load

If an LED open condition occurs, the MPQ7210 switches with a maximum duty cycle close to 100%, which makes  $V_{OUT}$  rise close to  $V_{IN}$ . The dynamic behavior of the buck converter's  $V_{OUT}$  during an LED open is influenced by the  $I_L$ , output capacitance ( $C_{OUT}$ ), and  $V_{IN}$ .

The switching operation under open-load conditions makes inductor and output capacitor resonance, forcing  $V_{OUT}$  to oscillate. This oscillation may result in output overshoot with a small  $C_{OUT}$ . At LED load hot-plug conditions, this overshoot may exceed the ISP<sub>x</sub> and ISN<sub>x</sub> breakdown voltages, so it is recommended to connect a larger-value capacitor or a diode (IN4148) from VOUT to VIN (see Figure 10).

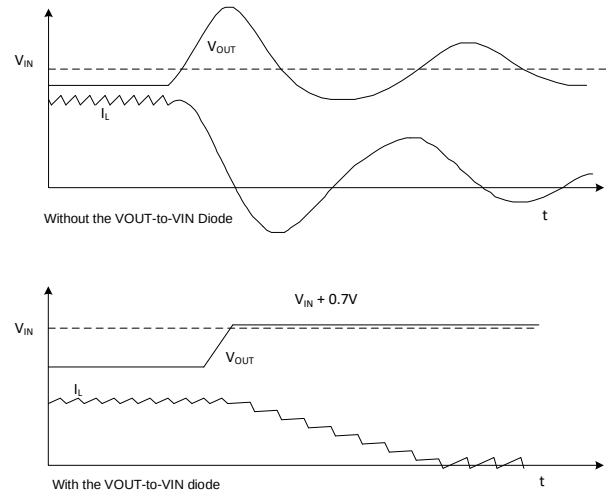


Figure 10: LED Load Open Condition

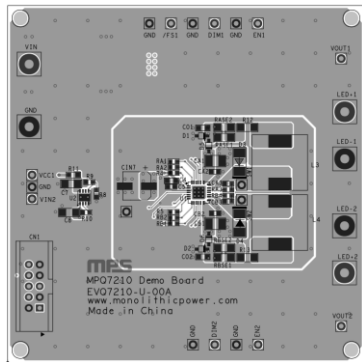
### Selecting the SW-to-PGND Node Diode

The SW-to-PGND node diode is necessary for most cases. The forward voltage of the body diode drops at high temperatures; at heavy loads, there is a sub-injection current that goes through the LS-FET's body diode. In this scenario, a Schottky diode with a low forward voltage (e.g. B360) is required.

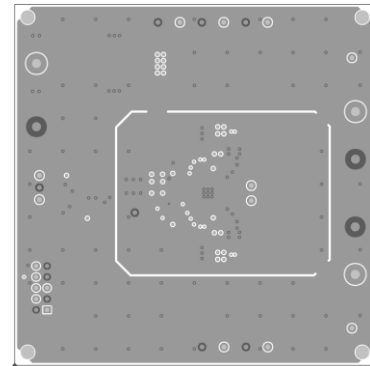
## PCB Layout Guidelines

Efficient PCB layout, especially for the input capacitor placement, is critical for stable operation. A 4-layer layout is strongly recommended to improve thermal performance. For the best results, refer to Figure 11 and follow the guidelines below:

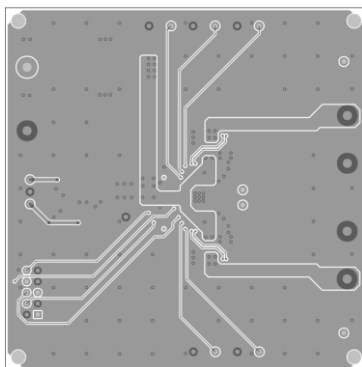
1. Place the symmetric input capacitors as close to VIN1, VIN2, and GND as possible.
2. Use a large ground plane to connect directly to PGND.
3. Add vias near PGND if the bottom layer is a ground plane.
4. Ensure that the high-current paths at GND and VINx have short, direct, and wide traces.
5. Place the ceramic input capacitor, especially the small package size (0603) input bypass capacitor, as close to VIN and PGND as possible to minimize high-frequency noise.
6. Place the VCC capacitor as close to VCC and GND as possible.
7. Place the SW-to-PGND diode close to the SW pin and the PGND pin.
8. Route SW and BST away from sensitive analog areas, such as ISPx and ISNx traces.
9. Route the ISPx and ISNx sense lines close together with a Kelvin connection to reduce the line drop error.
10. The top layer should include the power, signal, and GND.
11. Cover GND in all areas on the top layer, except for the signal and power path.
12. The second layer should only include GND to shield noise interference on the top layer.
13. The third layer should include the power, signal, and GND.
14. Cover GND in all areas on the bottom layer, except for the signal and power path.



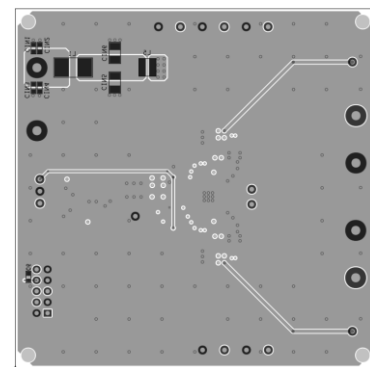
**Top Layer**



**Mid-Layer 1**



**Mid-Layer 2**



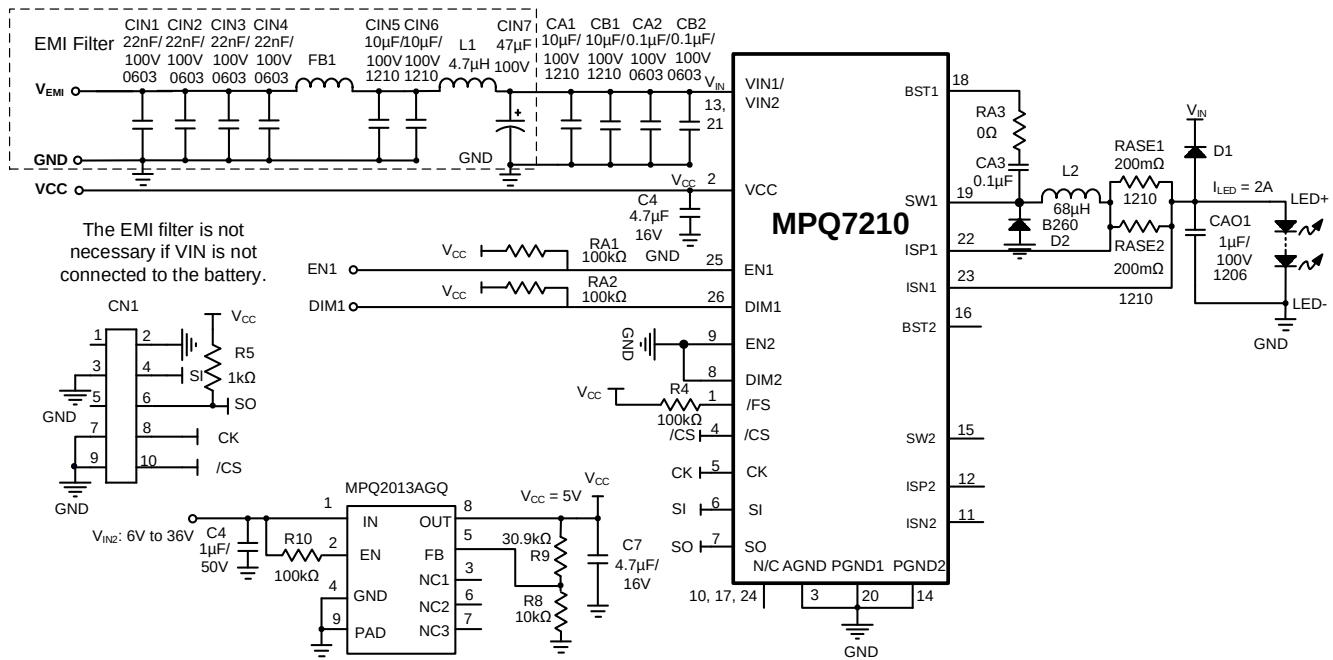
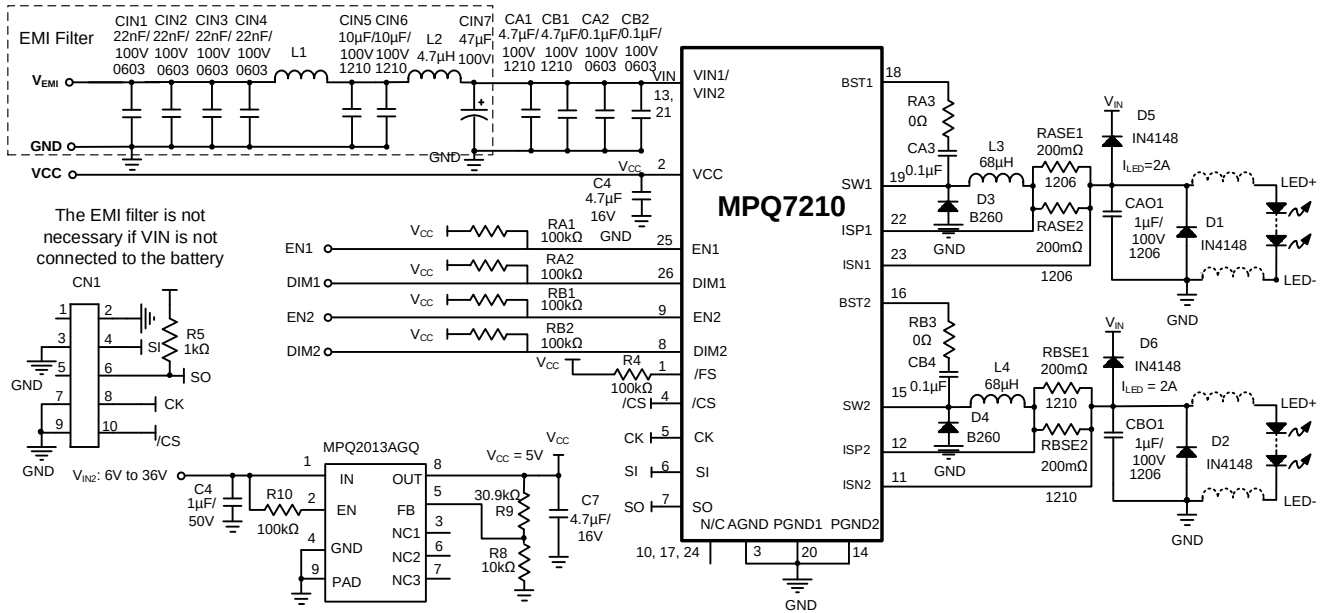
**Bottom Layer**

**Figure 11: Recommended PCB Layout**

### Note:

10) The recommended PCB layout is based on Figure 12 on page 48.

## TYPICAL APPLICATION CIRCUITS



**TYPICAL APPLICATION CIRCUITS (continued)**

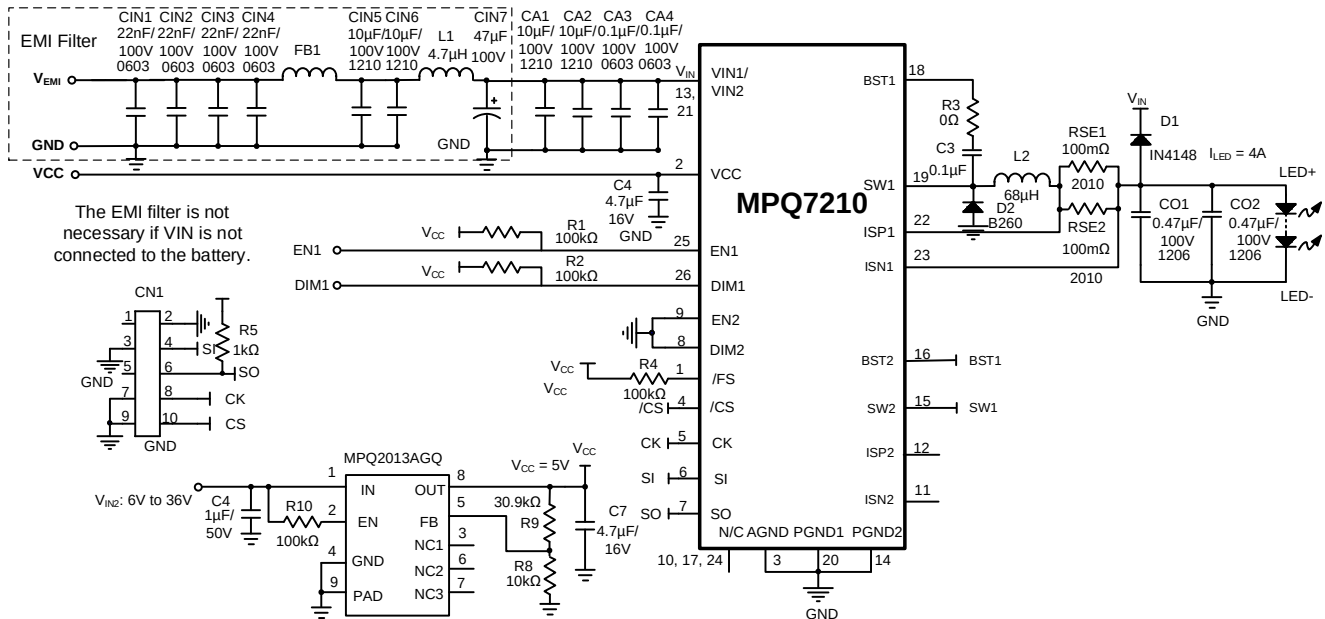


**Figure 14: Typical Application Circuit (OTP, Single-Channel,  $f_{sw} = 420\text{kHz}$ ,  $I_{LED} = 4\text{A}$ )**

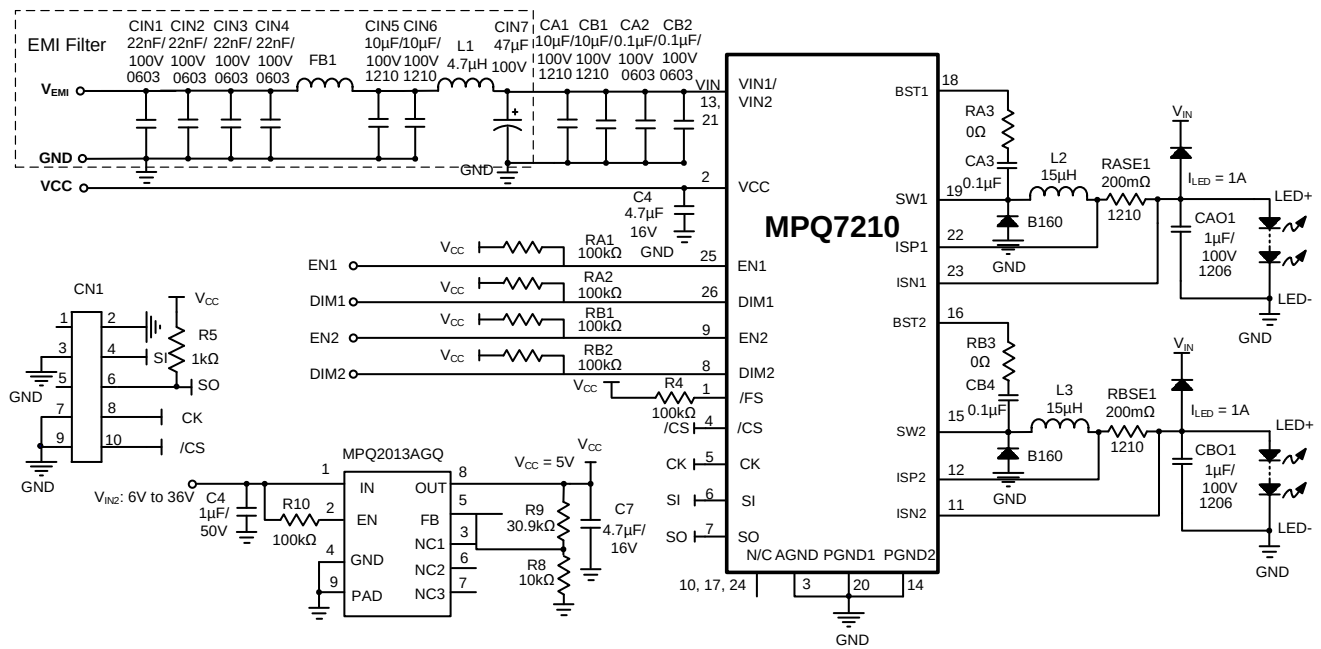
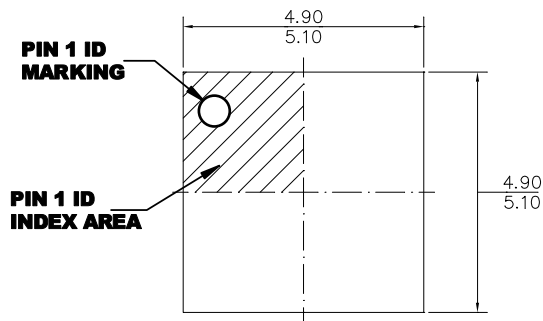


**Figure 15: Typical Application Circuit (OTP, Dual-Channel,  $f_{sw} = 2.3\text{MHz}$ ,  $I_{LED} = 1\text{A/Channel}$ )**

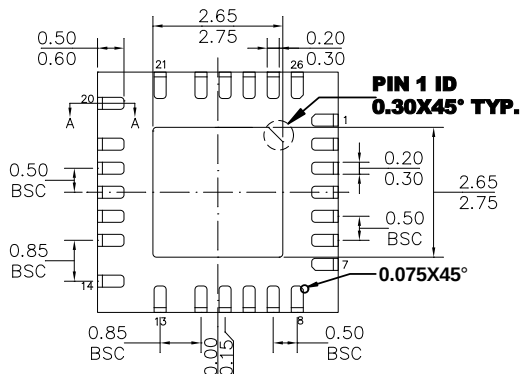
# PACKAGE INFORMATION

## QFN-26 (5mmx5mm)

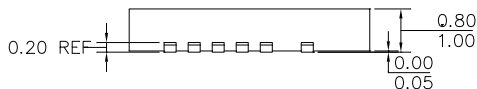
### Wettable Flank



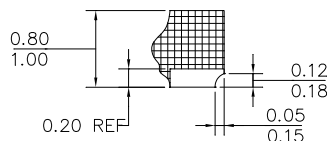
**TOP VIEW**



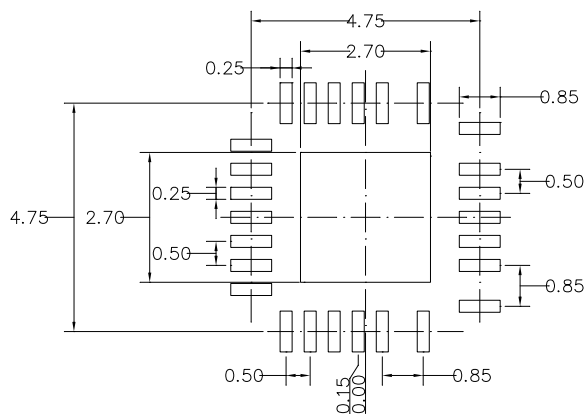
**BOTTOM VIEW**



**SIDE VIEW**



**SECTION A-A**

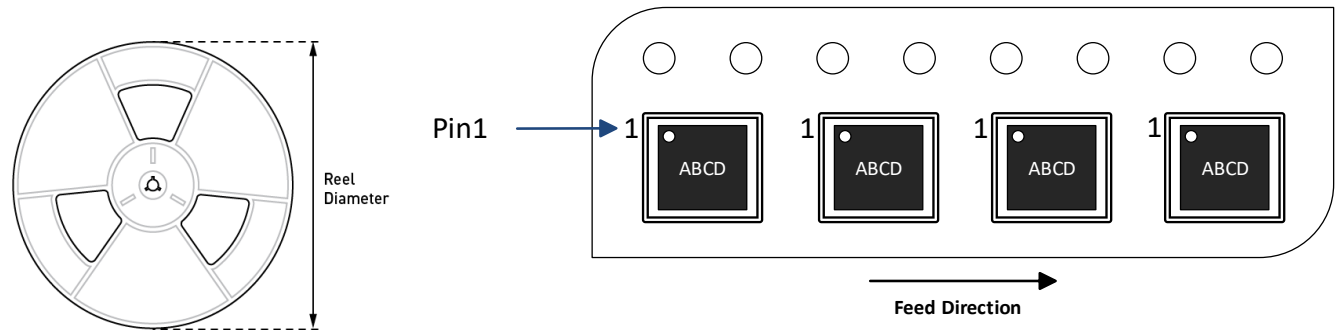


**RECOMMENDED LAND PATTERN**

#### NOTE:

- 1) THE LEAD SIDE IS WETTABLE.
- 2) ALL DIMENSIONS ARE IN MILLIMETERS.
- 3) EXPOSED PADDLE SIZE DOES NOT INCLUDE MOLD FLASH.
- 4) LEAD COPLANARITY SHALL BE 0.08 MILLIMETERS MAX.
- 5) DRAWING CONFIRMS TO JEDEC MO-220.
- 6) DRAWING IS NOT TO SCALE.

CARRIER INFORMATION



| Part Number            | Package Description | Quantity/ Reel | Quantity/ Tube | Quantity/ Tray | Reel Diameter | Carrier Tape Width | Carrier Tape Pitch |
|------------------------|---------------------|----------------|----------------|----------------|---------------|--------------------|--------------------|
| MPQ7210GUE-xxxx-AEC1-Z | QFN-26 (5mmx5mm)    | 5000           | N/A            | N/A            | 13in          | 12mm               | 8mm                |

## REVISION HISTORY

| Revision # | Revision Date | Description                                                                                                                                                                                                                                                                                                                            | Pages Updated |
|------------|---------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|---------------|
| 1.0        | 10/18/2023    | Initial Release                                                                                                                                                                                                                                                                                                                        | -             |
| 1.1        | 11/1/2024     | Updated the Description section: <ul style="list-style-type: none"> <li>Corrected the grammar error “a” with below: “The MPQ7210 is a synchronous, dual-buck LED driver.”</li> <li>Deleted the “such as the MPQ7241,” in this sentence “When paired with a matrix manager, such as the MPQ7241, the MPQ7210 can achieve...”</li> </ul> | 1             |
|            |               | Updated the Fixed-Frequency Band-to-Band Control section: <ul style="list-style-type: none"> <li>Updated the <math>f_{sw}</math> extended description to: “<math>f_{sw}</math> is extended and the real <math>f_{sw}</math> is <math>(D / t_{ON\_MIN})</math> or <math>((1 - D) / t_{OFF\_MIN})...</math>”</li> </ul>                  | 26            |
|            |               | Updated the Analog-to-Digital Converter (ADC) section: Updated “Register 0x12, bit D[4] can control...” to “Register 0x12, bit D[3] can control...”                                                                                                                                                                                    | 27            |
|            |               | Updated register 0x20, bit D[3] from BUCK1_EN to BUCK2_EN                                                                                                                                                                                                                                                                              | 33            |
|            |               | Updated ADC_CTRL (0x12), bits D[15:8] default to 0x05                                                                                                                                                                                                                                                                                  | 33, 41        |
|            |               | <ul style="list-style-type: none"> <li>Updated PWM_DIM register to PWM_DIM1</li> </ul> Updated PWM_DIM1 register to PWM_DIM2                                                                                                                                                                                                           | 35            |

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