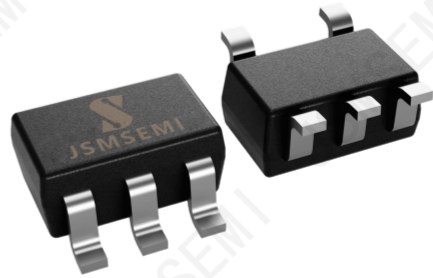


Description

The SN74LV1T08 device is a single 2-input positive-AND gate. The device performs the Boolean function $Y = A \cdot B$ or $Y = A + B$ in positive logic. Low I_{CC} current allows this device to be used in power-sensitive or battery-powered applications.

The SN74LV1T08 is available in Green SOT23-5 and SOT-353 packages. It operates over an ambient temperature range of -40°C to $+125^{\circ}\text{C}$.



Features

- Operating Range: 2.0 V to 5.5 V
- Typ t_{pd} of 4.1 ns at 5 V
- Low Power Consumption: Maximum I_{CC} of $1\mu\text{A}$
- $\pm 32\text{mA}$ Output Drive at 5 V
- Inputs Are TTL-Voltage Compatible
- Operating Temperature Range: -40°C to $+125^{\circ}\text{C}$
- Packages: SOT23-5, SOT-353(SC70-5)
- RoSH compatible

Applications

- TV, Set-Top Box, and Audio
- Wireless Infrastructure
- Factory Automation and Control
- PC and Notebooks
- Building Automation
- Grid Infrastructure
- Medical, Healthcare, and Fitness
- Printers
- Test and Measurement
- EPOS (Electronic Point of Sale)
- Telecom Infrastructure
- Projectors

Logic Diagram



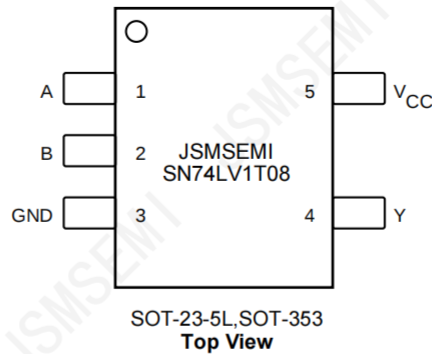
Function Table

INPUTS		OUTPUT
A	B	Y
H	H	H
L	X	L
X	L	L

Ordering Information

Order number	Package	Marking	Operation Temperature Range	MSL Grade	Ship,Quantity	Green
SN74LV1T08DBVR-JSM	SOT-23-5L	B08S	-40 to 125°C	3	TR&3000	Rohs
SN74LV1T08DCKR-JSM	SOT-353	BEG	-40 to 125°C	3	TR&3000	Rohs

Pin Configuration and Functions



Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
A	1	I	Input A
B	2	I	Input B
GND	3	—	Ground Pin
V _{CC}	5	—	Supply Pin
Y	4	O	Output

Specifications

Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted).⁽¹⁾⁽²⁾

		MIN	MAX	UNIT
V _{CC}	Supply voltage range	-0.5	6.5	V
V _I	Input voltage range ⁽²⁾	-0.5	6.5	V
V _O	Voltage range applied to any output in the high-impedance or power-off state ⁽²⁾	-0.5	6.5	V
V _O	Voltage range applied to any output in the high or low state ⁽²⁾⁽³⁾	-0.5	V _{CC} +0.5	V
I _{IK}	Input clamp current		-50	mA
I _{OK}	Output clamp current		-50	mA
I _O	Continuous output current		±50	mA
	Continuous current through V _{CC} or GND		±100	mA
θ _{JA}	Package thermal impedance ⁽⁴⁾	SOT23-5	230	°C/W
		SC70-5	376	
T _J	Junction temperature ⁽⁵⁾	-65	150	°C
T _{stg}	Storage temperature	-65	150	°C

- Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under Recommended Operating Conditions is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- The input and output negative-voltage ratings may be exceeded if the input and output current ratings are observed.
- The value of V_{CC} is provided in the Recommended Operating Conditions table.
- The package thermal impedance is calculated in accordance with JESD-51.
- The maximum power dissipation is a function of T_{J(MAX)}, R_{θJA}, and T_A. The maximum allowable power dissipation at any ambient temperature is P_D = (T_{J(MAX)} - T_A) / R_{θJA}. All numbers apply for packages soldered directly onto a PCB.

ESD Ratings

		VALUE	UNIT
V _(ESD)	Electrostatic discharge	Human-body model (HBM)	±2500
		Charged-device model (CDM)	±1000

Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)⁽¹⁾

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	MAX	UNIT
Supply voltage	V _{CC}	Operating	2.0	5.5	V
High-level input voltage	V _{IH}	V _{CC} =2.0V	1.0		V
		V _{CC} =3.3V	1.5		
		V _{CC} =4.5V to 5.5V	2.0		
Low-level input voltage	V _{IL}	V _{CC} =2.0V		0.3	V
		V _{CC} =3.3V		0.55	
		V _{CC} =4.5V to 5.5V		0.8	
Input voltage	V _I		0	5.5	V
Output voltage	V _O		0	V _{CC}	V
Input transition rise or fall	Δt/Δv	V _{CC} =2.0V to 5.5V		5	ns/V
Operating temperature	T _A		-40	+125	°C

(1) All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation.

Electrical Characteristics

over recommended operating free-air temperature range (TYP values are at T_A = +25°C, Full=-40°C to 125°C, unless otherwise noted.)

PARAMETER		TEST CONDITIONS	V _{CC}	TEMP	MIN ⁽²⁾	TYP ⁽³⁾	MAX ⁽²⁾	UNIT
V _{OH}		I _{OH} = -100μA	2.0V to 5.5V	Full	V _{CC} -0.1			V
		I _{OH} = -8mA	2.0		1.6			
		I _{OH} = -24mA	3.3		2.5			
		I _{OH} = -32mA	4.5V		3.8			
			5V		4.2			
			5.5V		4.8			
V _{OL}		I _{OL} = 100μA	2.0V to 5.5V	Full			0.1	V
		I _{OH} = 8mA	2.0				0.45	
		I _{OH} = 24mA	3.3				0.55	
		I _{OL} = 32mA	4.5V				0.55	
			5V				0.5	
			5.5V				0.45	
I _I	A or B inputs	V _I =5.5V or GND	0V to 5.5V	+25°C		±0.1	±1	μA
				Full			±5	
I _{off}		V _I or V _O =5.5V	0V	+25°C		±0.1	±1	μA
				Full			±10	
I _{CC}		V _I =5.5V or GND, I _O =0	2.0V to 5.5V	+25°C		0.1	1	μA
				Full			10	
ICCT		One input at 3.4V, Other inputs at V _{CC} or GND	5.5V	Full			500	μA
C _i (Input Capacitance)		V _{CC} =0V, f=10MHz	0V	+25°C		6		pF

(1) All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation.

(2) Limits are 100% production tested at 25°C. Limits over the operating temperature range are ensured through correlations using statistical quality control (SQC) method.

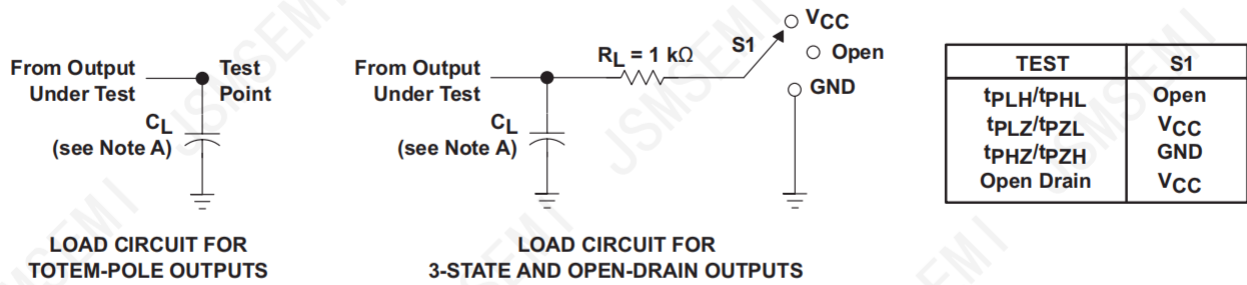
(3) Typical values represent the most likely parametric norm as determined at the time of characterization. Actual typical values may vary over time and will also depend on the application and configuration.

PARAMETER	SYMBOL	TEST CONDITIONS		MIN ⁽²⁾	TYP ⁽³⁾	MAX ⁽²⁾	UNIT
Propagation Delay	t_{pd}	$V_{CC}=2.0V\pm0.2V$	$C_L=30pF, R_L=500\Omega$		15.5		ns
		$V_{CC}=3.3V\pm0.3V$	$C_L=50pF, R_L=500\Omega$		13.5		
		$V_{CC}=5V\pm0.5V$	$C_L=50pF, R_L=500\Omega$		4.1		
Power dissipation capacitance	C_{pd}	$V_{CC}=5V$	$f=10MHz$		22		pF

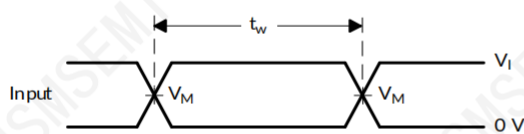
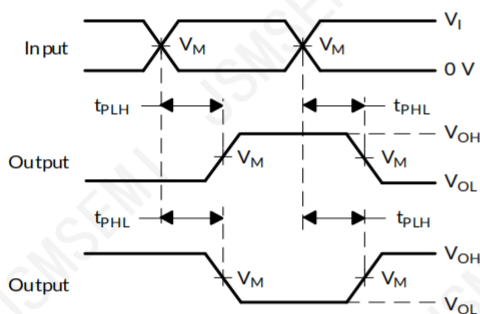
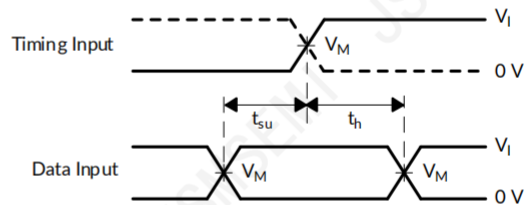
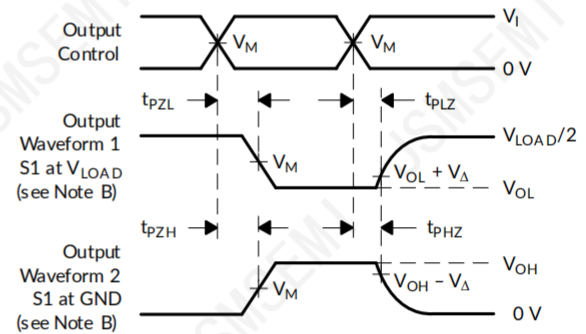
(1) All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation.

(2) This parameter is ensured by design and/or characterization and is not tested in production.

(3) Typical values represent the most likely parametric norm as determined at the time of characterization. Actual typical values may vary over time and will also depend on the application and configuration.

Parameter Measurement Information


V_{CC}	INPUTS		V_M	V_{LOAD}	C_L	R_L	V_{Δ}
	V_I	t_r/t_f					
$2.0V \pm 0.2V$	V_{CC}	$\leq 2ns$	$V_{CC}/2$	$2 \times V_{CC}$	30pF	500Ω	0.15V
$3.3V \pm 0.3V$	3V	$\leq 2.5ns$	1.5V	6V	50pF	500Ω	0.3V
$5V \pm 0.5V$	V_{CC}	$\leq 2.5ns$	$V_{CC}/2$	$2 \times V_{CC}$	50pF	500Ω	0.3V


VOLTAGE WAVEFORMS
PULSE DURATION

VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
INVERTING AND NONINVERTING OUTPUTS

VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES

VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING
NOTES:

- CL includes probe and jig capacitance.
- Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
- All input pulses are supplied by generators having the following characteristics: $PRR \leq 10 \text{ MHz}$, $Z_O = 50\Omega$.
- The outputs are measured one at a time, with one transition per measurement.
- t_{PLZ} and t_{PHZ} are the same as t_{dis} .
- t_{PZL} and t_{PZH} are the same as t_{en} .
- t_{PLH} and t_{PHL} are the same as t_{pd} .
- All parameters and waveforms are not applicable to all devices.

Figure1. Load Circuit and Voltage Waveforms

Detailed Description

Overview

The SN74LV1T08 device is a single 2-input positive-AND gate. The device performs the Boolean AND function ($Y = A \cdot B$ or $Y = A + B$) in positive logic. Low I_{CC} current allows this device to be used in power-sensitive or battery-powered applications. Robust inputs allow the device to up-translate with a propagation delay of 20 ns.

Functional Block Diagram



Figure2. Logic Diagram(Positive Logic)

Feature Description

The V_{CC} for the device is optimized at 5 V.

The inputs accept V_{IH} levels of 2 V.

Output ringing is minimized by slow edge rates.

Inputs are TTL-Voltage compatible.

Device Functional Modes

Table 1 lists the functional modes of the SN74LV1T08.

Table 1. Function Table

INPUTS		OUTPUT
A	B	Y
H	H	H
L	X	L
X	L	L

Application Information

The SN74LV1T08 device is a single AND gate, which is often used for many common functions like power sequencing or an on LED indicator. Because the device is configured to output LOW unless all inputs are HIGH, an LED tied to the output of the device will only turn HIGH when all systems connected are sending a HIGH, or ready signal.

Typical Application

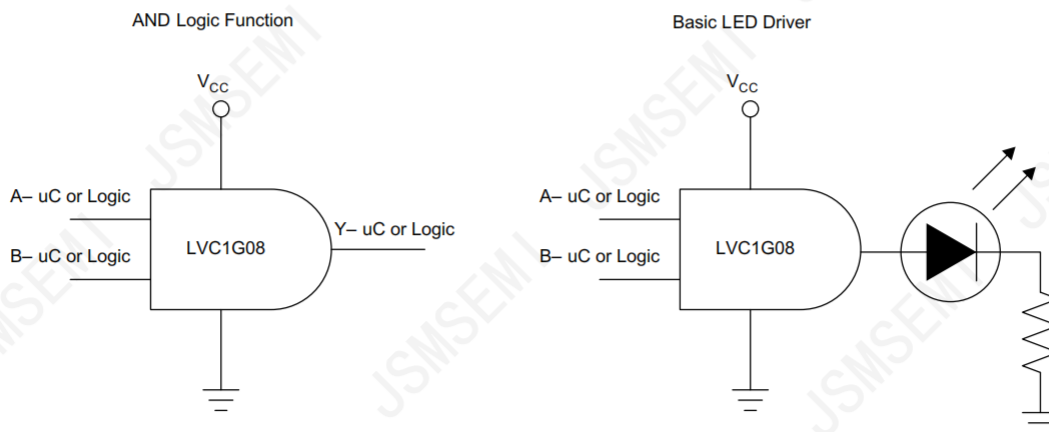


Figure3. Typical Application Diagram

Power Supply Recommendations

The power supply can be any voltage between the minimum and maximum supply voltage rating located in Recommended Operating Conditions.

Each V_{CC} pin must have a good bypass capacitor to prevent power disturbance. Recommends a $0.1\mu\text{F}$ capacitor for devices with a single supply; and a $0.01\mu\text{F}$ or $0.022\mu\text{F}$ capacitor for each power pin if there are multiple V_{CC} pins. It is ok to parallel multiple bypass capacitors to reject different frequencies of noise. $0.1\mu\text{F}$ and $1\mu\text{F}$ capacitors are commonly used in parallel. The bypass capacitor must be installed as close to the power pin as possible for best results.

Layout

Layout Guidelines

When using multiple bit logic devices inputs must not ever float. In many cases, functions or parts of functions of digital logic devices are unused; for example, when only two inputs of a triple-input AND gate are used or only 3 of the 4 buffer gates are used. Such input pins must not be left unconnected because the undefined voltages at the outside connections result in undefined operational states. Observe the following rules under all circumstances.

- All unused inputs of digital logic devices must be connected to a high or low bias to prevent them from floating.
- The logic level that must be applied to any particular unused input depends on the function of the device. Generally they will be tied to GND or V_{CC} , whichever make more sense or is more convenient.

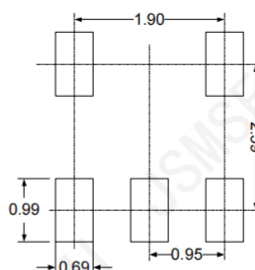
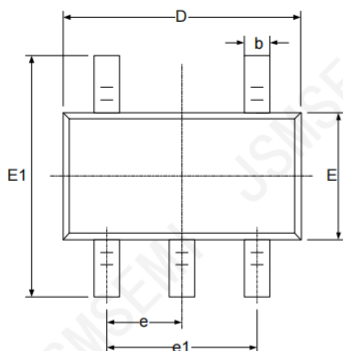
Layout Example



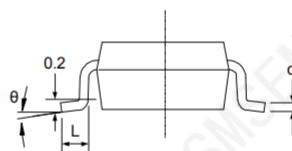
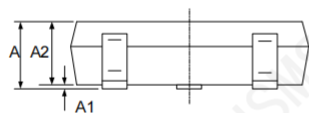
Figure 4. Layout Diagram

Package Information

SOT-23-5L



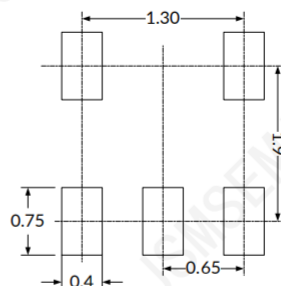
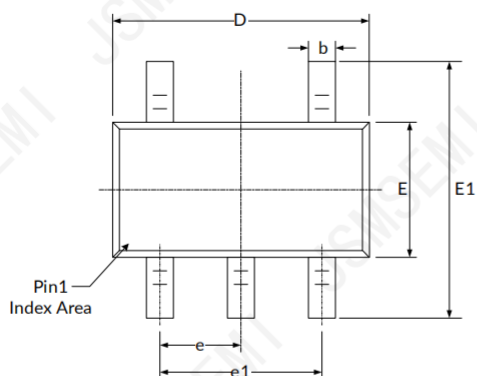
RECOMMENDED LAND PATTERN (Unit: mm)



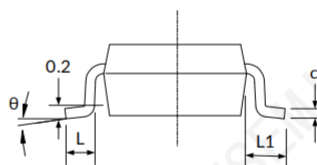
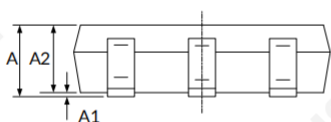
Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	1.050	1.250	0.041	0.049
A1	0.000	0.100	0.000	0.004
A2	1.050	1.150	0.041	0.045
b	0.300	0.500	0.012	0.020
c	0.100	0.200	0.004	0.008
D	2.820	3.020	0.111	0.119
E	1.500	1.700	0.059	0.067
E1	2.650	2.950	0.104	0.116
e	0.950(BSC)		0.037(BSC)	
e1	1.800	2.000	0.071	0.079
L	0.300	0.600	0.012	0.024
θ	0°	8°	0°	8°

Package Information

SOT-353(SC70-5)



RECOMMENDED LAND PATTERN (Unit: mm)



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	0.900	1.100	0.035	0.043
A1	0.000	0.100	0.000	0.004
A2	0.900	1.000	0.035	0.039
b	0.150	0.350	0.006	0.014
c	0.080	0.150	0.003	0.006
D ⁽¹⁾	2.000	2.200	0.079	0.087
E ⁽¹⁾	1.150	1.350	0.045	0.053
E1	2.150	2.450	0.085	0.096
e	0.650(BSC)		0.026(BSC)	
e1	1.300(BSC)		0.051(BSC)	
L	0.260	0.460	0.010	0.018
L1	0.525		0.021	
θ	0°	8°	0°	8°

Revision History

Rev.	Change	Date
V1.0	Initial version	3/17/2023

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