

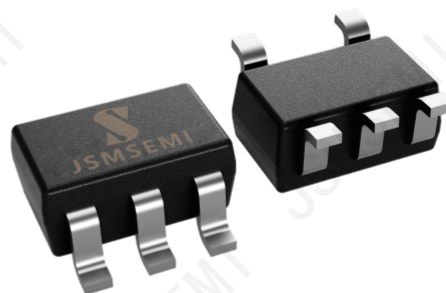
Description

This single 2-input positive-OR gate is designed for 1.65-V to 5.5-V V_{CC} operation.

The SN74LVC1G32 device performs the Boolean function $Y = A + B$ or $Y = \overline{A} \cdot \overline{B}$ in positive logic.

The CMOS device has high output drive while maintaining low static power dissipation over a broad V_{CC} operating range.

The SN74LVC1G32 device is available in Green SOT23-5 and SOT-353 packages. It operates over an ambient temperature range of -40°C to $+125^{\circ}\text{C}$.



Applications

- AV Receiver
- Blu-ray Player and Home Theater
- Digital Picture Frame (DPF)
- Embedded PC
- IP Phone: Wireless
- High-Speed Data Acquisition and Generation
- Motor Control: High-Voltage
- Optical Networking: Video Over Fiber and EPON
- Personal Navigation Device (GPS)
- Portable Media Player
- Private Branch Exchange (PBX)
- Server PSU
- SSD: Internal and External
- TV: LCD/Digital and High-Definition (HDTV)
- Telecom Shelter: Power Distribution Unit (PDU), Power Monitoring Unit (PMU), Wireless Battery Monitoring, Remote Electrical Tilt Unit (RET), Remote Radio Unit (RRU), Tower Mounted Amplifier (TMA)
- Video Conferencing: IP-Based HD
- Vector Signal Analyzer and Generator
- WiMAX and Wireless Infrastructure Equipment
- Wireless Headset, Keyboard, Mouse, and Repeater

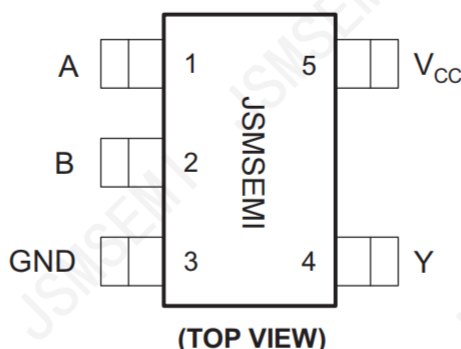
Features

- Packages: SOT23-5, SOT-353(SC70-5)
- Supports 5V V_{CC} Operation
- Inputs Accept Voltages to 5.5V
- Supports Down Translation to V_{CC}
- Typ t_{pd} of 4.1ns at 3.3V
- Low Power Consumption, 1 μA Max I_{CC}
- $\pm 24\text{mA}$ Output Drive at 3V
- I_{off} Supports Live Insertion, Partial-Power-Down Mode, and Back-Drive Protection
- Latch-Up Performance Exceeds 100 mA
- ESD Protection Exceeds JESD 22
 - 2000-V Human-Body Model
 - 200-V Machine Model
 - 1000-V Charged-Device Model
- Operating Temperature Range: -40°C to $+125^{\circ}\text{C}$
- RoSH compatible

Ordering Information

Order number	Package	Marking	Operation Temperature Range	MSL Grade	Ship,Quantity	Green
SN74LVC1G32DBVR-JSM	SOT-23-5L	C32R	-40 to 125°C	3	TR&3000	Rohs
SN74LVC1G32DCKR-JSM	SOT-353	CG5	-40 to 125°C	3	TR&3000	Rohs

Pin Configuration and Functions



Pin Functions

PIN		DESCRIPTION
NAME	SOT23-5 SOT-353	
A	1	Input
B	2	Input
GND	3	Ground
Y	4	Output
VCC	5	Power pin

Specifications

Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)⁽¹⁾

		MIN	MAX	UNIT
V _{CC}	Supply voltage range	-0.5	6.5	V
V _I	Input voltage range ⁽²⁾	-0.5	6.5	V
V _O	Voltage range applied to any output in the high-impedance or power-off state ⁽²⁾	-0.5	6.5	V
V _O	Voltage range applied to any output in the high or low state ⁽²⁾⁽³⁾	-0.5	V _{CC} + 0.5	V
I _{IK}	Input clamp current		-50	mA
I _{OK}	Output clamp current		-50	mA
I _O	Continuous output current		±50	mA
	Continuous current through V _{CC} or GND		±100	mA
T _J	Junction temperature	-65	150	°C
T _{stg}	Storage temperature	-65	150	°C

(1) Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under Recommended Operating Conditions is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

(2) The input and output negative-voltage ratings may be exceeded if the input and output current ratings are observed.

(3) The value of V_{CC} is provided in the Recommended Operating Conditions table.

ESD Ratings

PARAMETER	DEFINITION	VAUE	UNIT
V _(ESD) Electrostatic discharge	Human body model (HBM)	±2000	V
	Charged device model (CDM)	±1000	

Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)⁽¹⁾

			MIN	MAX	UNIT
V _{CC}	Supply voltage	Operating	1.65	5.5	V
		Data retention only	1.5		
V _{IH}	High-level input voltage	V _{CC} = 1.65 V to 1.95 V	0.65 × V _{CC}		V
		V _{CC} = 2.3 V to 2.7 V	1.7		
		V _{CC} = 3 V to 3.6 V	2		
		V _{CC} = 4.5 V to 5.5 V	0.7 × V _{CC}		
V _{IL}	Low-level input voltage	V _{CC} = 1.65 V to 1.95 V		0.15 × V _{CC}	V
		V _{CC} = 2.3 V to 2.7 V		0.3	
		V _{CC} = 3 V to 3.6 V		0.4	
		V _{CC} = 4.5 V to 5.5 V		0.15 × V _{CC}	
V _I	Input voltage		0	5.5	V
V _O	Output voltage		0	V _{CC}	V
I _{OH}	High-level output current	V _{CC} = 1.65 V		−4	mA
		V _{CC} = 2.3 V		−8	
		V _{CC} = 3 V		−16	
		V _{CC} = 4.5 V		−24	
I _{OL}	Low-level output current	V _{CC} = 1.65 V		4	mA
		V _{CC} = 2.3 V		8	
		V _{CC} = 3 V		16	
		V _{CC} = 4.5 V		32	
Δt/Δv	Input transition rise or fall rate	V _{CC} = 1.8 V ± 0.15 V, 2.5 V ± 0.2 V		20	ns/V
		V _{CC} = 3.3 V ± 0.3 V		10	
		V _{CC} = 5 V ± 0.5 V		5	
T _A	Operating free-air temperature	All other packages	−40	125	°C

(1) All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation.

Thermal Information

THERMAL METRIC ⁽¹⁾		SN74LVC1G32		UNIT
		SOT23	SC70	
		5 PINS	5 PINS	
R _{θJA}	Junction-to-ambient thermal resistance	229	278	°C/W
R _{θJctop}	Junction-to-case (top) thermal resistance	164	93	
R _{θJB}	Junction-to-board thermal resistance	62	65	
Ψ _{JT}	Junction-to-top characterization parameter	44	2	
Ψ _{JB}	Junction-to-board characterization parameter	62	64	
R _{θJcbot}	Junction-to-case (bottom) thermal resistance	—	—	

Electrical Characteristics—DC Limit Changes

 over recommended operating free-air temperature range (TYP values are at $T_A = +25^\circ\text{C}$, unless otherwise noted.) ⁽¹⁾

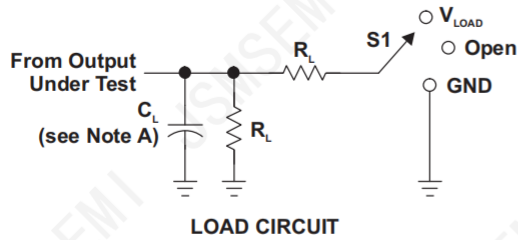
PARAMETER		TEST CONDITIONS	V _{CC}	TEMP	MIN	TYP	MAX	UNIT
V _{OH}		I _{OH} = -100μA	1.65V to 5.5V	Full	V _{CC} -0.1			V
		I _{OH} = -4mA	1.65V		1.2			
		I _{OH} = -8mA	2.3V		1.9			
		I _{OH} = -16mA	3V		2.4			
		I _{OH} = -24mA			2.3			
		I _{OH} = -32mA	4.5V		3.8			
V _{OL}		I _{OL} = 100μA	1.65V to 5.5V	Full			0.1	V
		I _{OL} = 4mA	1.65V				0.45	
		I _{OL} = 8mA	2.3V				0.3	
		I _{OL} = 16mA	3V				0.4	
		I _{OL} = 24mA					0.55	
		I _{OL} = 32mA	4.5V				0.55	
I _I	A or B inputs	V _I =5.5V or GND	0V to 5.5V	+25°C		±0.1	±1	μA
				Full			±5	
I _{off}		V _I or V _O =5.5V	0	+25°C		±0.1	±1	μA
				Full			±10	
I _{CC}		V _I =5.5V or GND, I _O =0	1.65V to 5.5V	+25°C		0.1	1	μA
				Full			10	
ΔI _{CC}		One input at V _{CC} -0.6V, Other inputs at V _{CC} or GND	3V to 5.5V	Full			500	μA

Electrical Characteristics—AC Limit Changes

PARAMETER	SYMBOL	TEST CONDITIONS		TEMP	MIN	TYP	MAX	UNIT
Propagation Delay	t_{pd}	$V_{CC}=1.8\text{V}\pm 0.15\text{V}$	$C_L=30\text{pF}$, $R_L=1\text{k}\Omega$	Full		8.0		ns
		$V_{CC}=2.5\text{V}\pm 0.2\text{V}$	$C_L=30\text{pF}$, $R_L=500\Omega$	Full		3.7		
		$V_{CC}=3.3\text{V}\pm 0.3\text{V}$	$C_L=50\text{pF}$, $R_L=500\Omega$	Full		2.5		
		$V_{CC}=5\text{V}\pm 0.5\text{V}$	$C_L=50\text{pF}$, $R_L=500\Omega$	Full		2.7		
Input Capacitance	C_i	$V_{CC}=3.3\text{V}$	$V_I=V_{CC}$ or GND	Full		4		pF
Power dissipation capacitance	C_{pd}	$V_{CC}=1.8\text{V}$	$f=10\text{MHz}$	$+25^\circ\text{C}$		20		pF
		$V_{CC}=2.5\text{V}$				21		
		$V_{CC}=3.3\text{V}$				22		
		$V_{CC}=5\text{V}$				25		

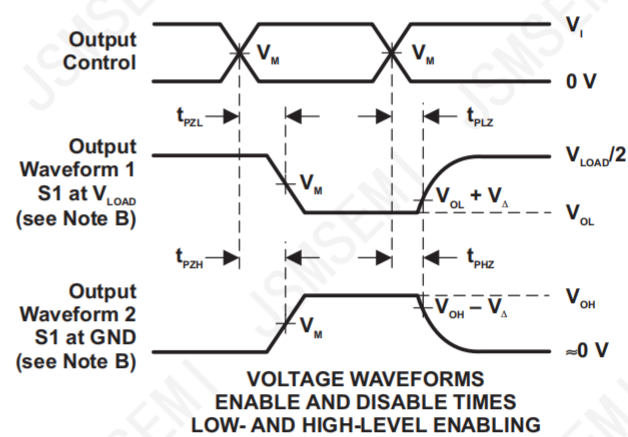
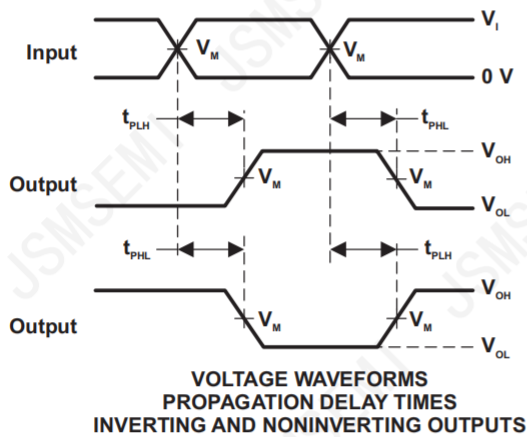
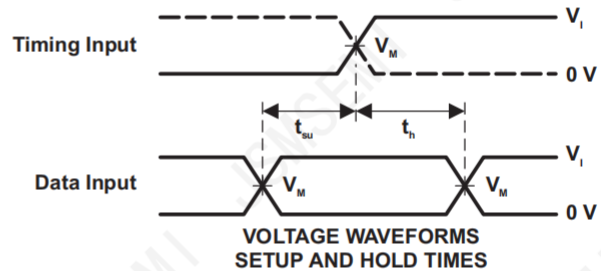
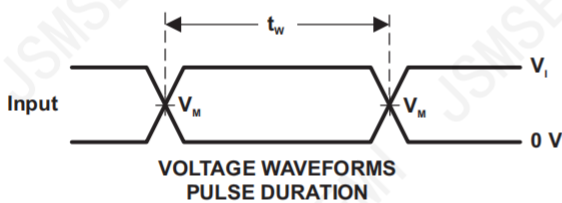
 (1) All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation.

Parameter Measurement Information



TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	V_{LOAD}
t_{PHZ}/t_{PZH}	GND

V_{CC}	INPUTS		V_M	V_{LOAD}	C_L		R_L		V_{Δ}
	V_I	t_r/t_f							
$1.8V \pm 0.15V$	V_{CC}	$\leq 2ns$	$V_{CC}/2$	$2 \times V_{CC}$	15pF	30pF	1M Ω	1k Ω	0.15V
$2.5V \pm 0.2V$	V_{CC}	$\leq 2ns$	$V_{CC}/2$	$2 \times V_{CC}$	15pF	30pF	1M Ω	500 Ω	0.15V
$3.3V \pm 0.3V$	3V	$\leq 2.5ns$	1.5V	6V	15pF	50pF	1M Ω	500 Ω	0.3V
$5V \pm 0.5V$	V_{CC}	$\leq 2.5ns$	$V_{CC}/2$	$2 \times V_{CC}$	15pF	50pF	1M Ω	500 Ω	0.3V



- NOTES:
- C_L includes probe and jig capacitance.
 - Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
 - All input pulses are supplied by generators having the following characteristics: $PRR \leq 10 \text{ MHz}$, $Z_o = 50 \Omega$.
 - The outputs are measured one at a time, with one transition per measurement.
 - t_{PLZ} and t_{PHZ} are the same as t_{SU} .
 - t_{PZL} and t_{PZH} are the same as t_{H} .
 - t_{PLH} and t_{PHL} are the same as t_{pd} .
 - All parameters and waveforms are not applicable to all devices.

Figure 1. Load Circuit and Voltage Waveforms

Detailed Description

Overview

The SN74LVC1G32 device contains one 2-input positive OR gate device and performs the Boolean function $Y = A + B$ or $Y = \overline{A} \cdot \overline{B}$. This device is fully specified for partial-power-down applications using I_{off} . The I_{off} circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down.

Functional Block Diagram



Feature Description

- Wide operating voltage range.
 - Operates from 1.65 V to 5.5 V.
- Allows down voltage translation.
- Inputs accept voltages to 5.5 V.
- I_{off} feature allows voltages on the inputs and outputs, when V_{CC} is 0 V.

Device Functional Modes

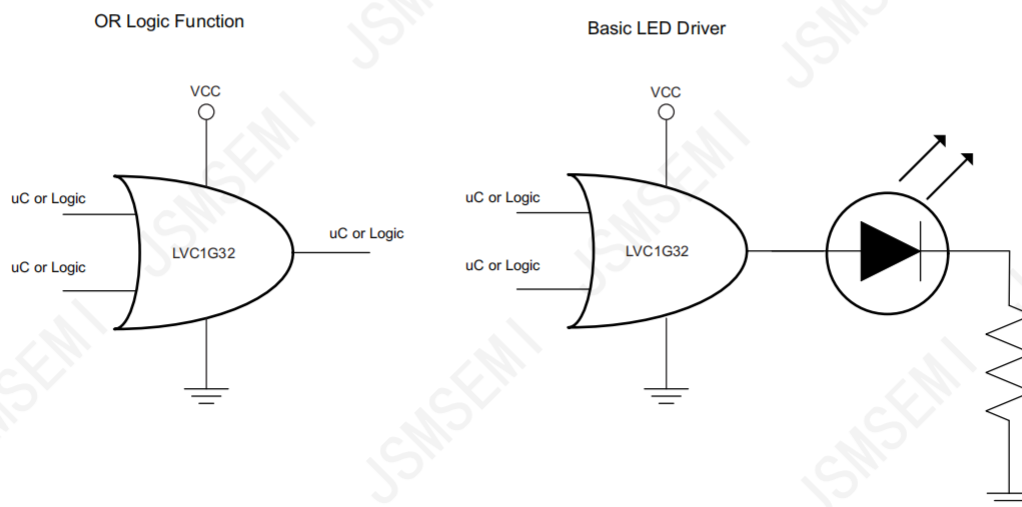
Function Table

INPUTS		OUTPUT Y
A	B	
H	X	H
X	H	H
L	L	L

Application Information

The SN74LVC1G32 device is a high drive CMOS device that can be used for implementing OR logic with a high output drive, such as an LED application. It can produce 24 mA of drive current at 3.3 V making it ideal for driving multiple outputs and good for high speed applications up to 100 MHz. The inputs are 5.5-V tolerant allowing translation down to V_{CC} .

Typical Application



Power Supply Recommendations

The power supply can be any voltage between the min and max supply voltage rating located in the Recommended Operating Conditions table.

Each VCC pin should have a good bypass capacitor to prevent power disturbance. For devices with a single supply, a 0.1 μ F capacitor is recommended. If there are multiple VCC pins, then a 0.01 μ F or 0.022 μ F capacitor is recommended for each power pin. It is ok to parallel multiple bypass capacitors to reject different frequencies of noise. A 0.1 μ F and 1- μ F capacitors are commonly used in parallel. The bypass capacitor should be installed as close to the power pin as possible for best results.

Layout

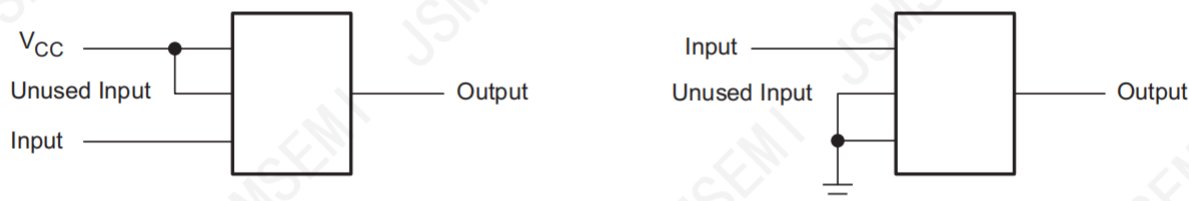
Layout Guidelines

When using multiple bit logic devices inputs should not ever float.

In many cases, functions or parts of functions of digital logic devices are unused; for example, when only two inputs of a triple-input AND gate are used, or only 3 of the 4 buffer gates are used. Such input pins should not be left unconnected because the undefined voltages at the outside connections result in undefined operational states.

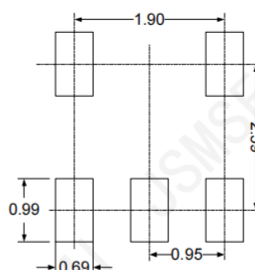
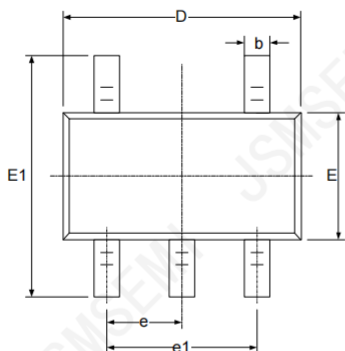
Specified in Layout Example are the rules that must be observed under all circumstances. All unused inputs of digital logic devices must be connected to a high or low bias to prevent them from floating. The logic level that should be applied to any particular unused input depends on the function of the device. Generally they will be tied to GND or VCC, whichever make more sense or is more convenient.

Layout Example

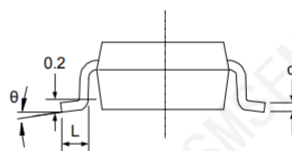
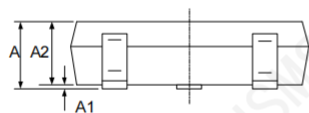


Package Information

SOT-23-5L



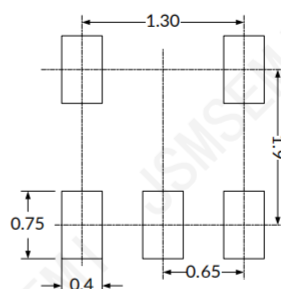
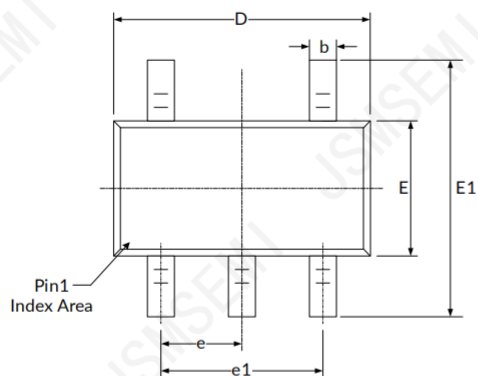
RECOMMENDED LAND PATTERN (Unit: mm)



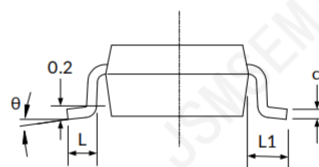
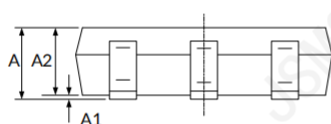
Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	1.050	1.250	0.041	0.049
A1	0.000	0.100	0.000	0.004
A2	1.050	1.150	0.041	0.045
b	0.300	0.500	0.012	0.020
c	0.100	0.200	0.004	0.008
D	2.820	3.020	0.111	0.119
E	1.500	1.700	0.059	0.067
E1	2.650	2.950	0.104	0.116
e	0.950(BSC)		0.037(BSC)	
e1	1.800	2.000	0.071	0.079
L	0.300	0.600	0.012	0.024
θ	0°	8°	0°	8°

Package Information

SOT-353(SC70-5)



RECOMMENDED LAND PATTERN (Unit: mm)



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	0.900	1.100	0.035	0.043
A1	0.000	0.100	0.000	0.004
A2	0.900	1.000	0.035	0.039
b	0.150	0.350	0.006	0.014
c	0.080	0.150	0.003	0.006
D ⁽¹⁾	2.000	2.200	0.079	0.087
E ⁽¹⁾	1.150	1.350	0.045	0.053
E1	2.150	2.450	0.085	0.096
e	0.650(BSC)		0.026(BSC)	
e1	1.300(BSC)		0.051(BSC)	
L	0.260	0.460	0.010	0.018
L1	0.525		0.021	
θ	0°	8°	0°	8°

Revision History

Rev.	Change	Date
V1.0	Initial version	6/27/2021

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