MP2761

I²C-Controlled, 2-Cell to 4-Cell Buck-Boost Charger with NVDC Power Path Management

DESCRIPTION

The MP2761 is a buck-boost charger IC designed for battery packs with 2-cell to 4-cell in series. The device can accept a wide 4V to 22V input voltage (V_{IN}) range to charge the battery. The buck-boost topology allows the battery voltage (V_{BATT}) to be above or below V_{IN}.

When the input is present, the MP2761 operates in charge mode. It measures V_{BATT} and charges the battery with four phases: constant-current trickle charge, constant-current pre-charge, constant-current fast charge, and constant-voltage charge. Additional features include charge termination and auto-recharge.

The MP2761 also integrates the input current (I_{IN}) limit and V_{IN} limit to avoid overloading the input power source. This is compliant to the USB and power delivery (PD) specifications.

The MP2761 provides narrow-voltage DC (NVDC) power path management. An integrated N-channel MOSFET driver (BGATE) controls an external N-channel MOSFET (BATFET) to regulate the system's minimum voltage and provide a battery supplement function. The device can also supply a wide voltage range (4V to 21V) at the IN pin when source mode is enabled. The device also has an IN output current limit in source mode (I_{IN_SRC}) with a high resolution. These are compliant with USB PD specifications.

The I²C/SMBus interface can configure the charge and discharge parameters, including the I_{IN} limit, V_{IN} limit, charge current, battery-full regulation voltage, IN output voltage in source mode (V_{IN_SRC}), and I_{IN_SRC}. The MP2761 can also provide information on statuses and faults through the I²C/SMBus registers.

To guarantee safe operation, the device limits the die temperature to a configurable threshold. Other safety features include input over-voltage protection (OVP), battery OVP, system OVP, thermal shutdown, and a configurable timer to prevent prolonged charging of a dead battery.

The MP2761 is available in a TQFN-30 (4mmx5mm) package.

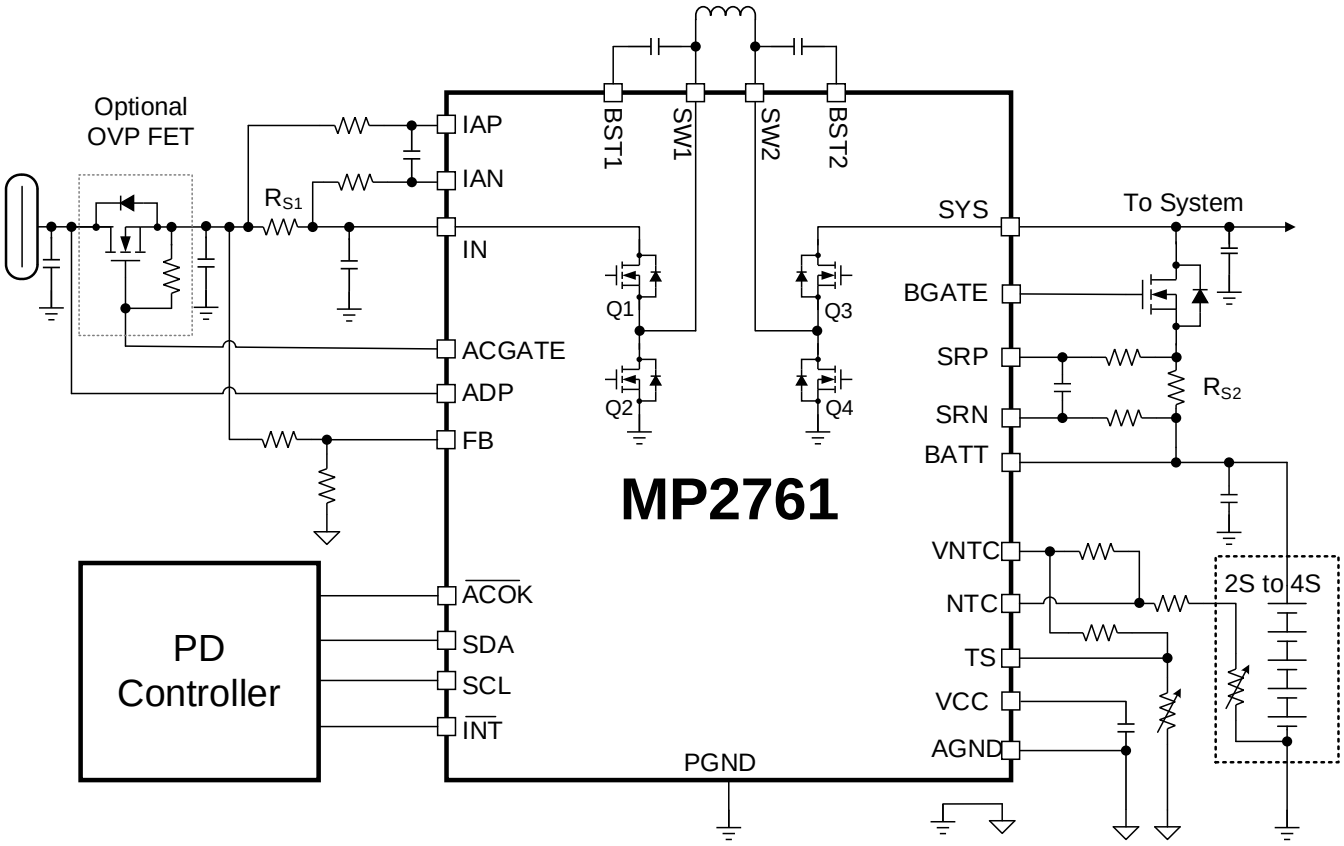
FEATURES

- Buck-Boost Charger for 2-Cell to 4-Cell in Series Battery Packs
- 4V to 22V Operation Input Voltage (V_{IN})
- Up to 26V Sustainable Voltage (Up to 28V with External MOSFET)
- Supports USB 2.0, USB 3.0, USB 3.1, USB 3.2, USB Type-C, and USB PD 3.0 Settings
- Smooth Transition for Buck and Boost Modes
- Configurable Maximum Input Current (I_{IN}) Limit and Minimum V_{IN} Limit
- Up to 6A Configurable Charge Current
- Configurable Battery-Full Voltage Up to 18.72V with 0.5% Accuracy
- Configurable 4V to 21V IN Output Voltage in Source Mode (V_{IN_SRC}) with 20mV/Step
- Up to 6A Output Current in Source Mode (I_{IN_SRC}) with 50mA/Step
- 375kHz to 770kHz Configurable Switching Frequency (f_{SW})
- I²C or SMBus Host Control Interface
- Input Power Source Status Indicator
- Integrated 10-Bit ADC for Monitoring
- Analog Output Pin to Monitor Battery Current in Charge Mode and Source Mode
- Input OVP, System OVP, and Battery OVP
- System SCP in Charge Mode
- IN Output SCP in USB PD Source Mode
- Battery Missing Detection
- NTC Pin Floating Detection
- Integrated N-Channel MOSFET Driver for Input Power Pass-Through or OVP
- Integrated N-Channel MOSFET Driver for NVDC Power Path Control
- Configurable Battery Temperature Protection
- Thermal Regulation and Thermal Shutdown
- Available in a TQFN-30 (4mmx5mm) Package

APPLICATIONS

- USB Power Delivery (PD) Devices
- General Multiple-Cell Applications

TYPICAL APPLICATION



ORDERING INFORMATION

Part Number*	Package	Top Marking	MSL Rating
MP2761GVT-xxxx**	TQFN-30 (4mmx5mm)	*See Below*	1
MP2761GVT-0000***		*See Below*	1
MP2761GVT-0300****		*See Below*	1
MP2761GVT-0400*****		*See Below*	1
EVKT-MP2761	Evaluation Kit	-	-

* For Tape & Reel, add suffix -Z (e.g. MP2761GVT-xxxx-Z).

** "xxxx" is the register setting option. Contact an MPS FAE to obtain an "xxxx" value.

*** "0000" is the factory default for 2-cell applications. This content can be viewed in the I^2C register map.

**** "0300" is the factory default for 3-cell applications.

***** "0400" is the factory default for 4-cell applications.

TOP MARKING

MPSYWW

MP2761

LLLLLL

MPS: MPS prefix
Y: Year code
WW: Week code
MP2761: Part number
LLLLLL: Lot number

EVALUATION KIT EVKT-MP2761

EVKT-MP2761 kit contents (items below can be ordered separately):

#	Part Number	Item	Quantity
1	EVL2761-VT-00A	MP2761-0000 evaluation board	1
2	EVKT-USBI2C-02 bag	Includes one USB-to-I^2C communication interface, one USB cable, and one ribbon cable	1
3	Online resources	Include datasheet, user guide, product brief, and GUI	-

Order directly from MonolithicPower.com or our distributors.

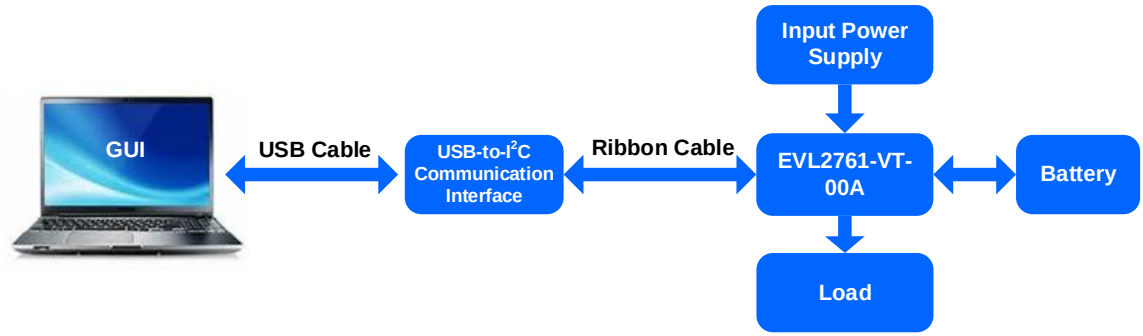
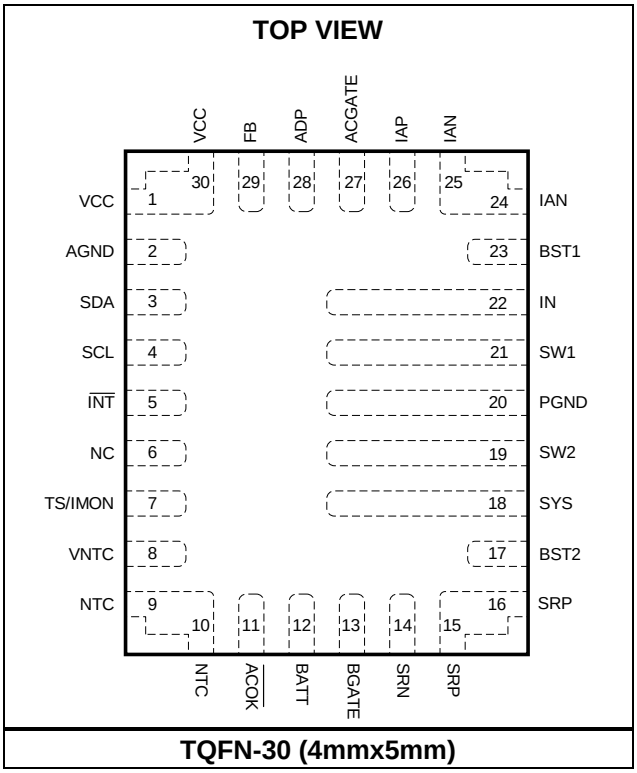


Figure 1: EVKT-MP2761 Evaluation Kit Set-Up

PACKAGE REFERENCE



TQFN-30 (4mmx5mm)

PIN FUNCTIONS

Pin #	Name	Description
1, 30	VCC	**VCC low-dropout (LDO) output.** Connect a 4.7µF ceramic capacitor from the VCC pin to AGND. VCC is a 3.6V output that can pull up the internal circuit and open-drain pins.
2	AGND	**Analog ground.** All parameter settings refer to this ground.
3	SDA	**I²C/SMBus data.** Connect SDA to the logic rail through a 10kΩ resistor.
4	SCL	**I²C/SMBus clock.**Connect SCL to the logic rail through a 10kΩ resistor.
5	$\overline{\text{INT}}$	**Interrupt request output.** This is an open-drain structure that must be pulled up to VCC via an external 10kΩ resistor. This pin can be floated if it is not used.
6	NC	**Leave this pin floating.**
7	TS/IMON	**Temperature sense/current monitor.** This pin can be used as either a temperature-sense pin (TS) or a current monitor pin (IMON). If this pin is configured as IMON, it can monitor the battery charging current in charge mode, and the discharging current in source mode.
8	VNTC	**Battery temperature-sense bias.** This pin is used as the voltage bias of the NTC and TS comparators' voltage dividers for both the feedback and reference.
9, 10	NTC	**Negative temperature coefficient (NTC) thermistor pin.** The NTC pin is the battery's temperature-sense input.
11	$\overline{\text{ACOK}}$	**Input power good (PG) indication.** This pin is an open-drain output that indicates when the adapter is present. This pin must be pulled up to VCC via an external 10kΩ resistor. This pin can be floated if it is not used.
12	BATT	**Battery voltage sense pin.** Connect the BATT pin to the battery pack's positive terminal. It is recommended to use two 22µF ceramic capacitors. To reduce the constant-voltage (CV) phase time, place the battery pack's positive terminal as close as possible to the BATT pin.
13	BGATE	**Battery N-channel MOSFET gate driver.** The BGATE pin drives the N-channel MOSFET between the SYS and SRP pins.
14	SRN	**Sense resistor negative terminal.**
15, 16	SRP	**Sense resistor positive terminal.**
17	BST2	**Bootstrap.** Connect a 100nF bootstrap capacitor between the BSTx and SWx pins to form a floating supply across the power switch driver. This drives the power switch's gate above the supply voltage.
23	BST1	
18	SYS	**System pin.** SYS is the power output of the MP2761. Place a 1µF ceramic capacitor from SYS to PGND, and as close as possible to the IC. It is recommended to use four 22µF ceramic capacitors.
19	SW2	**Switching node.** SW2 is the middle point of the boost phase's half-bridge.
20	PGND	**Power ground.**
21	SW1	**Switching node.** SW1 is the middle point of the buck phase's half-bridge.
22	IN	**Input pin.** IN is the power stage input of the IC. It is recommended to place four 10µF ceramic capacitors at IN.
24, 25	IAN	**Input current-sense negative terminal.**
26	IAP	**Input current-sense positive terminal.**
27	ACGATE	**Input N-channel MOSFET gate driver.** The ACGATE pin drives the external pass-through N-channel MOSFET. Connect a 1MΩ resistor between ACGATE and the N-channel MOSFET's source port.
28	ADP	**Adapter voltage sense.** If the ADP pin's over-voltage protection (OVP) threshold is reached, an external OVP MOSFET (if available) is turned off by the ACGATE driver, and the power stage is disabled. The ADP pin also provides the IC's internal bias voltage. It is recommended to place three 10µF ceramic capacitors at ADP.
29	FB	**Feedback pin.** The FB pin is the output voltage (V_{IN_SRC}) feedback pin in source mode. If V_{IN_SRC} feedback is configured via the register, this pin is not functional. Leave the FB pin floating or connect it to AGND.

ABSOLUTE MAXIMUM RATINGS (1)

ADP, ACGATE to PGND (DC).....-0.3V to +28V
IAP, IAN, IN to PGND (DC).....-0.3V to +26V
IAP, IAN, IN to PGND (20ns).....-0.3V to +28V
IAP to IAN .....-3.6V to +3.6V
SW1, SW2 to PGND (DC) .....-0.3V to +24V
SW1, SW2 to PGND (20ns).....-2V to +28V
SYS, BATT to PGND .....-0.3V to +24V
SRP, SRN to PGND .....-0.3V to +24V
SRP to SRN.....-3.6V to +3.6V
BGATE to PGND... . . . . . -0.3V to +26V
VCC to AGND……-0.3V to +4V
BST1 to SW1 ..... 0 to 4V
BST2 to SW2 ..... 0 to 4V
All others pins to AGND .....-0.3V to V_{CC} + 0.3V
Junction temperature (T_J) .....150°C
Lead temperature .....260°C
Continuous power dissipation (T_A = 25°C) (2)
..... 3.29W
Storage temperature……..-65°C to +150°C

ESD Ratings

Human body model (HBM) 2kV
Charged-device model (CDM) 750V

Recommended Operating Conditions (3)

Supply voltage (V_{IN}) .....4V to 22V
Input current (I_{IN}).....Up to 6A
System current (I_{SYS}).....Up to 6A
Charge current (I_{CC}) .....Up to 6A
Battery voltage (V_{BATT}) .....Up to 22V
Operating junction temp (T_J).... -40°C to +125°C

Thermal Resistance θ_{JA} (4) θ_{JC} (5)

TQFN-30 (4mmx5mm) ..... 32 ..... 1.8 .. °C/W

Notes:

1) Exceeding these ratings may damage the device.
2) The maximum allowable power dissipation is a function of the maximum junction temperature, T_J (MAX), the junction-to-ambient thermal resistance, θ_{JA}, and the ambient temperature, T_A. The maximum allowable continuous power dissipation at any ambient temperature is calculated by P_D (MAX) = (T_J (MAX) - T_A) / θ_{JA}. Exceeding the maximum allowable power dissipation can produce an excessive die temperature, and the regulator may go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
3) The device is not guaranteed to function outside of its operating conditions.
4) The simulated junction-to-ambient thermal resistance result. The simulation model is set up following JESD51-2 and JESD51-7.
5) The simulated junction-to-case (bottom) thermal resistance result.

ELECTRICAL CHARACTERISTICS

V_{IN} = 5V, V_{BATT} = 3.7V/cell, 4-cell setting, T_A = 25°C, unless otherwise noted.

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Input Power Characteristic						
Input voltage range	V_{IN}		4		22	V
ADP under-voltage lockout (UVLO) threshold	V_{ADP_UVLO}	ADP voltage (V_{ADP}) falling	2.4	2.6	3.05	V
ADP UVLO hysteresis		V_{ADP} rising		1		V
ADP over-voltage protection (OVP) threshold	V_{ADP_OVP}	V_{ADP} rising	23	23.9	24.7	V
ADP OVP hysteresis		V_{ADP} falling		500		mV
ADP OVP recover deglitch time		V_{ADP} falling		100		ms
Input under-voltage protection (UVP)	V_{IN_UVP}	V_{IN} falling, REG11h, bits[9:8] = 00	2.9	3.2	3.5	V
		V_{IN} falling, REG11h, bits[9:8] = 01	6	6.4	6.8	V
		V_{IN} falling, REG11h, bits[9:8] = 10	11.5	12	12.5	V
		V_{IN} falling, REG11h, bits[9:8] = 11	16.2	16.8	17.4	V
Input UVP threshold hysteresis		V_{IN} rising, REG11h, bits[9:8] = 01, 10, or 11		328		mV
		V_{IN} rising, REG11h, bits[9:8] = 00		490		mV
Input UVP recovery deglitch time	t_{INUVP_DGL}	V_{IN} rising		30		ms
Input OVP threshold	V_{IN_OVP}	V_{IN} rising, REG11h, bits[7:6] = 00	6.9	7.25	7.6	V
		V_{IN} rising, REG11h, bits[7:6] = 01	10.8	11.25	11.7	V
		V_{IN} rising, REG11h, bits[7:6] = 10	17	17.65	18.25	V
		V_{IN} rising, REG11h, bits[7:6] = 11	22	22.45	23.15	V
Input OVP deglitch time	t_{INOVP_DGL}	V_{IN} rising, REG11h, bit[10] = 0		1		µs
		V_{IN} rising, REG11h, bit[10] = 1		15		ms
Input OVP hysteresis		V_{IN} falling		320		mV
Input OVP recovery deglitch time		V_{IN} falling		30		ms
DC/DC Converter						
Input quiescent current	I_{IN_Q}	V_{IN} = 5V, buck-boost mode, DC/DC disable, ACGATE and BGATE are disabled		550	620	µA
		V_{IN} = 5V/9V, buck-boost mode, DC/DC disable, BGATE is disabled, ACGATE is enabled		1	1.2	mA
		V_{IN} = 5V/9V, buck-boost mode, BGATE and ACGATE are enabled, DC/DC enable, charging disabled		7	9.1	mA
VCC low-dropout (LDO) output voltage	V_{VCC}	V_{IN} = 5V, I_{VCC} = 15mA		3.6		V
VCC LDO current limit	I_{VCC}	V_{IN} = 5V, V_{VCC} = 3.3V		23		mA

ELECTRICAL CHARACTERISTICS *(continued)*

V_{IN} = 5V, V_{BATT} = 3.7V/cell, 4-cell setting, T_A = 25°C, unless otherwise noted.

Parameter	Symbol	Conditions	Min	Typ	Max	Units
IN to SW1 N-channel MOSFET (Q1) on resistance	R_{ON_Q1}			10		mΩ
SW1 to PGND N-channel MOSFET (Q2) on resistance	R_{ON_Q2}			8		mΩ
SYS to SW2 N-channel MOSFET (Q3) on resistance	R_{ON_Q3}			8		mΩ
SW2 to PGND N-channel MOSFET (Q4) on resistance	R_{ON_Q4}			20		mΩ
Operation frequency	f_{SW}	REG0Eh, bits[6:4] = 000		375		kHz
		REG0Eh, bits[6:4] = 001		425		kHz
		REG0Eh, bits[6:4] = 010		475		kHz
		REG0Eh, bits[6:4] = 011		510		kHz
		REG0Eh, bits[6:4] = 100		550		kHz
		REG0Eh, bits[6:4] = 101		625		kHz
		REG0Eh, bits[6:4] = 110		700		kHz
		REG0Eh, bits[6:4] = 111		770		kHz
Minimum system voltage setting	V_{SYS_MIN}	2-cell OTP code setting, REG07h, bits[6:0] = 010 0000	6.2	6.4	6.6	V
		3-cell OTP code setting, REG07h, bits[6:0] = 010 1101	8.73	9	9.27	V
		4-cell OTP code setting, REG07h, bits[6:0] = 011 1100	11.64	12	12.36	V
Battery track regulation voltage	V_{TRACK}	T_A = 25°C, 2-cell OTP code setting, REG10h, bits[10:9] = 01, REG10h, bits[4:0] = 10100,		200		mV
		T_A = 25°C, 3-cell OTP code setting, REG10h, bits[10:9] = 10, REG10h, bits[4:0] = 10100		300		mV
		T_A = 25°C, 4-cell OTP code setting, REG10h, bits[10:9] = 11, REG10h, bits[4:0] = 10100		430		mV
SYS OVP threshold	V_{SYS_OV}	V_{SYS} rising, as a percentage of V_{SYS} regulation, REG11h, bits[14:13] = 11		110		%
SYS OVP hysteresis		V_{SYS} falling		5		%
SYS UVP threshold	V_{SYS_UV}	V_{SYS} falling, as a percentage of V_{SYS} regulation, REG11h, bits[12:11] = 00		75		%
SYS UVP hysteresis		V_{SYS} falling, as a percentage of V_{SYS} regulation		5		%
SYS UVP deglitch time	t_{SYSUVP_DGL}	V_{SYS} falling		10		ms

ELECTRICAL CHARACTERISTICS *(continued)*

V_{IN} = 5V, V_{BATT} = 3.7V/cell, 4-cell setting, T_A = 25°C, unless otherwise noted.

Parameter	Symbol	Conditions	Min	Typ	Max	Units
SYS UV recovery deglitch time		V_{SYS} rising		375		ms
Battery Charger						
Battery charge voltage regulation range		2-cell	6.8		9.34	V
		3-cell	10.2		14.01	V
		4-cell	13.6		18.68	V
Battery charge voltage regulation accuracy		V_{BATT_REG} = 8.4V, 2-cell	-0.5		+0.5	%
		T_A = 0°C to 70°C, V_{BATT_REG} = 8.4V, 2-cell	-0.7		+0.7	%
		V_{BATT_REG} = 12.6V, 3-cell	-0.5		+0.5	%
		T_A = 0°C to 70°C, V_{BATT_REG} = 12.6V, 3-cell	-0.7		+0.7	%
		V_{BATT_REG} = 16.8V, 4-cell	-0.5		+0.5	%
		T_A = 0°C to 70°C, V_{BATT_REG} = 16.8V, 4-cell	-0.7		+0.7	%
Fast charge current range	I_{CC}	R_{S2} = 10mΩ, REG10h, bit[7] = 0	0		6.35	A
Fast charge current accuracy (V_{BATT} > $V_{SYS\_REG\_MIN}$)	I_{CC_ACC}	I_{CC} = 6A, V_{BATT} = 7.6V, REG14h, bits[13:6] = 0111 1000	5.82	6.13	6.37	A
		I_{CC} = 3A, V_{BATT} = 7.6V, REG14h, bits[13:6] = 0011 1100	2.92	3.08	3.22	A
		I_{CC} = 2A, V_{BATT} = 7.6V, REG14h, bits[13:6] = 0010 1000	1.95	2.07	2.20	A
		I_{CC} = 500mA, V_{BATT} = 7.6V, REG14h, bits[13:6] = 0000 1010	0.45	0.55	0.65	A
Fast charge current accuracy (V_{BATT} >V_{BATT_PRE})		I_{CC} = 2A, V_{BATT} = 6.2V, V_{SYS_MIN} = 6.4V, V_{TRACK} = 100mV	-10		+10	%
Pre-charge to fast charge threshold	V_{BATT_PRE}	REG0Bh, bit[12] = 1	2.9	3	3.1	V/cell
		REG0Bh, bit[12] = 0	2.45	2.55	2.6	V/cell
Pre-charge to fast charge deglitch time				30		ms
Pre-charge to fast charge hysteresis		MP2761-0000		190		mV
		MP2761-0300		240		mV
		MP2761-0400		315		mV
Pre-charge current range	I_{PRE}	2-cell OTP code setting, R_{S2} = 10mΩ, REG10h, bit[7] = 0	0		1.5	A
Pre-charge current accuracy		2-cell OTP code setting, V_{BATT} = 5V, I_{PRE} = 300mA, REG0Fh, bits[7:4] = 0011	-20		+20	%
		2-cell OTP code setting, V_{BATT} = 5V, I_{PRE} = 500mA, REG0Fh, bits[7:4] = 0101	-15		+15	%

ELECTRICAL CHARACTERISTICS *(continued)*

V_{IN} = 5V, V_{BATT} = 3.7V/cell, 4-cell setting, T_A = 25°C, unless otherwise noted.

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Trickle charge to pre-charge threshold	V_{BATT_TC}	V_{BATT} rising		2		V/cell
Trickle charge to pre-charge hysteresis		V_{BATT} falling		200		mV/cell
Trickle charge current range	I_{TC}	2-cell OTP code setting, R_{S2} = 10mΩ, REG10h, bit[7] = 0	0		750	mA
Trickle charge current		2-cell OTP code setting, V_{BATT} = 3V, REG0Fh, bits[11:8] = 0010, I_{TC} = 100mA	55	100	155	mA
Auto-recharge battery voltage threshold		V_{BATT} falling, REG10h, bit[11] = 0, V_{BATT_REG} = 4.2V/cell		120		mV/cell
Battery auto-recharge deglitch time	t_{RECH_DGL}			240		ms
Battery OVP threshold	V_{BATT_OVP}	V_{BATT} rising, V_{BATT_REG} = 4.2V/cell	170	230	285	mV/cell
Battery OVP hysteresis		V_{BATT} falling, V_{BATT_REG} = 4.2V/cell		113		mV/cell
Battery OVP deglitch time				30		ms
Linear charge timer		V_{BATT}<$V_{SYS\_REG\_MIN}$	1.8	2	2.2	hours
Switching charge timer		V_{BATT}>$V_{SYS\_REG\_MIN}$, REG12h, bits[12:11] = 11	18	20	22	hours
Termination current accuracy	I_{TERM}	2-cell OTP code setting, I_{TERM} = 100mA, REG0Fh, bits[3:0] = 0010	47	100	146	mA
		2-cell OTP code setting, I_{TERM} = 200mA, REG0Fh, bits[3:0] = 0100	150	200	257	mA
		2-cell OTP code setting, I_{TERM} = 400mA, REG0Fh, bits[3:0] = 1000	353	400	460	mA
Charge termination deglitch time	t_{TERM_DGL}			1		sec
Pin Leakage Current						
SRP/SRN leakage current	$I_{LKG\_SRP\_SRN}$		-0.5		+0.5	µA
IAP/IAN leakage current	$I_{LKG\_IAP\_IAN}$		-0.5		+0.5	µA
Input Current Limit and Input Voltage Limit						
Input current limit range		R_{S1} = 10mΩ	0		5.8	A

ELECTRICAL CHARACTERISTICS *(continued)*

V_{IN} = 5V, V_{BATT} = 3.7V/cell, 4-cell setting, T_A = 25°C, unless otherwise noted.

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Input maximum current limit regulation	I_{IN_LIM}	REG08h, bits[6:0] = 000 1010, I_{IN_LIM} = 0.5A	0.368	0.43	0.5	A
		REG08h, bits[6:0] = 001 0010, I_{IN_LIM} = 0.9A	0.768	0.82	0.9	A
		REG08h, bits[6:0] = 001 1110, I_{IN_LIM} = 1.5A	1.32	1.41	1.5	A
		REG08h, bits[6:0] = 011 1100, I_{IN_LIM} = 3.0A	2.76	2.87	2.98	A
		REG08h, bits[6:0] = 110 0100, I_{IN_LIM} = 5.0A	4.688	4.836	4.98	A
Input minimum voltage limit regulation	V_{IN_MIN}	REG06h, bits[7:0] = 0011 1001, V_{IN_MIN} = 4.56V	4.44	4.58	4.72	V
		REG06h, bits[7:0] = 1000 0010, V_{IN_MIN} = 10.4V	10.19	10.4	10.61	V
		REG06h, bits[7:0] = 1010 1010, V_{IN_MIN} = 13.6V	13.33	13.6	13.87	V
		REG06h, bits[7:0] = 1110 0111, V_{IN_MIN} = 18.48V	18.11	18.48	18.85	V
Thermal Regulation and Protection						
Thermal shutdown rising threshold (6)	T_{J_SHDN}	T_J rising		150		°C
Thermal shutdown hysteresis (6)				20		°C
Thermal regulation threshold	T_{J_REG}	REG0Fh, bits[14:12] = 111		120		°C
Battery Temperature Monitoring						
NTC floating threshold	V_{NTC_FLT}	V_{NTC} rising as a percentage of V_{VNTC}		95		%
NTC floating threshold hysteresis		V_{NTC} falling as a percentage of V_{VNTC}		3		%
NTC cold temp threshold	V_{COLD}	V_{NTC} rising as a percentage of V_{VNTC} , REG0Dh, bits[1:0] = 01	73.5	74.5	75.5	%
NTC cold temp threshold hysteresis		V_{NTC} falling as a percentage of V_{VNTC}		1.2		%
NTC cool temp threshold	V_{COOL}	V_{NTC} rising as a percentage of V_{VNTC} ,REG0Dh, bits[3:2] = 10	64.2	65.2	66.2	%
NTC cool temp threshold hysteresis		V_{NTC} falling as a percentage of V_{VNTC}		1.2		%
NTC warm temp threshold	V_{WARM}	V_{NTC} falling as a percentage of V_{VNTC} , REG0Dh, bits[5:4] = 01	32.2	33.2	34.2	%
NTC warm temp threshold hysteresis		V_{NTC} rising as a percentage of V_{VNTC}		1.2		%
NTC hot temp threshold	V_{HOT}	V_{NTC} falling as percentage of V_{NTC}, REG0Dh, bits[7:6] = 10	22.6	23.6	24.6	%
NTC hot temp threshold hysteresis		V_{NTC} rising as percentage of V_{NTC}		1.2		%

ELECTRICAL CHARACTERISTICS *(continued)*

V_{IN} = 5V, V_{BATT} = 3.7V/cell, 4-cell setting, T_A = 25°C, unless otherwise noted.

Parameter	Symbol	Conditions	Min	Typ	Max	Units
TS hot	V_{TS_HOT}	REG0Dh, bits[12:10] = 100	12.24	14.95	15.66	%
VNTC	V_{VNTC}	T_A = 0°C to 70°C	1.26	1.28	1.30	V
Source Mode						
IN output voltage in source mode	V_{IN_SRC}	I_{IN_SRC} = 0A, V_{BATT} = 7.6V, REG09h, bits[9:0] = 00 1111 1010	4.85	5.0	5.15	V
		I_{DSCHG} = 0A, V_{BATT} = 7.6V, REG09h, bits[9:0] = 01 1100 0010	8.82	9.0	9.18	V
		I_{DSCHG} = 0A, V_{BATT} = 7.6V, REG09h, bits[9:0] = 10 0101 1000	11.76	12.0	12.24	V
		I_{DSCHG} = 0A, V_{BATT} = 7.6V, REG09h, bits[9:0] = 10 1110 1110	14.7	15.0	15.3	V
		I_{DSCHG} = 0A, V_{BATT} = 7.6V, REG09h, bits[9:0] = 11 1110 1000	19.7	20.0	20.3	V
FB reference voltage for external setting	V_{FB}	REG09h, bits[9:0] = 11 1110 1000	1.196	1.213	1.229	V
		REG09h, bits[9:0] = 00 1111 1010	0.306	0.313	0.32	V
Output OVP in source mode	$V_{IN\_SRC\_OV}$	V_{BATT} = 7.4V, V_{IN_SRC} rising, percentage of output voltage setting in source mode, REG11h, bits[14:13] = 11		110		%
Output OVP hysteresis in source mode		V_{IN_SRC} falling		4		%
Output UVP in source mode	$V_{IN\_SRC\_UV}$	REG11h, bits[12:11] = 00		75		%
Output UVP hysteresis in source mode				5		%
Output UV deglitch time in source mode	$t_{IN\_SRC\_UV\_DGL}$	V_{IN_SRC} falling		10		ms
Output UV recover deglitch time in source mode		V_{IN_SRC} rising		30		ms
Output current regulation in source mode	I_{IN_SRC}	REG0Ah, bits[6:0] = 001 0101, V_{BATT} = 7.4V	0.9			A
		REG0Ah, bits[6:0] = 010 0010, V_{BATT} = 7.4V	1.5			A
		REG0Ah, bits[6:0] = 100 0001, V_{BATT} = 7.4V	3.0			A
Battery UVLO threshold	V_{BATT_UVLO}	V_{BATT} falling	2.5	2.6	2.7	V/cell
Battery UVLO hysteresis		V_{BATT} rising		280		mV/cell
Battery low voltage threshold	V_{BATT_LOW}	V_{BATT} falling, REG0Bh, bits[10:9] = 10	3.1	3.2	3.3	V/cell
Battery low voltage hysteresis		V_{BATT} rising		200		mV/cell
Battery low voltage deglitch time		V_{BATT} falling		30		ms

ELECTRICAL CHARACTERISTICS *(continued)*

V_{IN} = 5V, V_{BATT} = 3.7V/cell, 4-cell setting, T_A = 25°C, unless otherwise noted.

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Battery standby current	$I_{BATT\_STANDBY}$	V_{IN} = 0V, V_{BATT} = 8.4V, source mode disabled, BGATE disabled, ACGATE disabled, ADC off, watchdog timer (REG05h, bit[9]) disable.	28	33	39.3	µA
Battery quiescent current	I_{BATT_Q}	V_{IN} = 0V, V_{BATT} = 8.4V, BGATE is enabled, source mode is disabled, ADC off, watchdog timer (REG05h, bit[9]) and ACGATE driver are disabled		70	81.8	µA
		V_{IN} = 0V, V_{BATT} = 8.4V, BGATE is enabled, watchdog timer (REG05h, bit[9]) is enabled, source mode is disabled, ADC off, ACGATE driver is disabled,			0.655	mA
		V_{IN} = 0V, V_{BATT} = 8.4V, BGATE is enabled, both ADC and watchdog timer(REG05h, bit[9]) are enabled, source mode is disabled, ACGATE driver is disabled			3.2	mA
Ultrasonic Mode (USM)						
USM regulation frequency	f_{USM}	REG07h, bit[8] = 1		30		kHz
BGATE and ACGATE Driver						
BGATE	V_{BGATE}	2 cell, V_{BATT} = 8.4V, above V_{SYS} when enabled	6			V
		BGATE disabled	0			V
ACGATE	V_{ACGATE}	Above V_{ADP} when enabled		6		V
		ACGATE disabled		0		V
Open-Drain Pin Characteristics (INT, ACOK)						
Low logic voltage threshold	V_L	Sink 10mA current			0.4	V
ADC						
Sample rate				50		kHz
ADC reference				1.28		V
ADC resolution				10		bits
SMBus Interface (7)						
Input high threshold level	V_{IH}	$V_{PULL\ UP}$ = 1.8V, SDA and SCL	1.3			V
Input low threshold level	V_{IL}	V_{PULL_UP} = 1.8V, SDA and SCL			0.4	V
Output low threshold level	V_{OL}	I_{SINK} = 1mA			0.4	V
Input leakage current	I_{LEAK}		-0.2		+0.2	µA
SMBus Timing Characteristics (6)						
SMBus clock frequency	f_{SCL}		10		400	kHz
Bus free time		Between a stop and start command	1.3			µs

ELECTRICAL CHARACTERISTICS *(continued)*

V_{IN} = 5V, V_{BATT} = 3.7V/cell, 4-cell setting, T_A = 25°C, unless otherwise noted.

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Start command hold time after which first clock is generated			0.6			µs
Start command set-up time			0.6			µs
Stop command set-up time			0.6			µs
Data hold time			0			ns
Data setup time			100			ns
Clock low timeout			25		35	ms
Clock low period			1.3			µs
Clock high period			0.6			µs
Clock/data falling time					300	ns
Clock/data rising time					300	ns

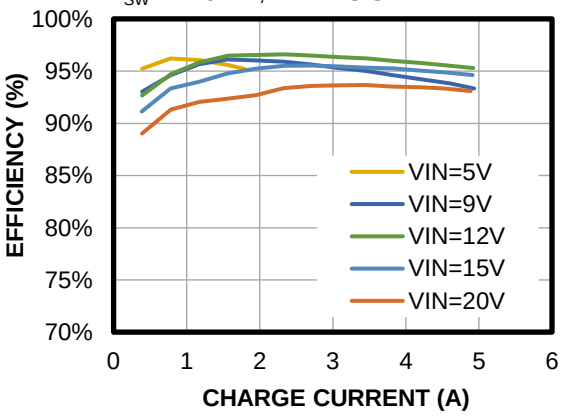
Notes:

6) Not tested in production and guaranteed by design and characterization.
7) SMBus should cover the I^2C specifications. The I^2C/SMBus lines are compatible with 1.8V/3.3V logic.

TYPICAL CHARACTERISTICS

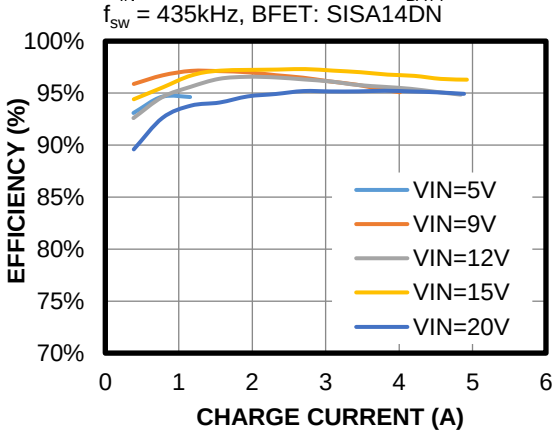
Efficiency vs. Charge Current

V_{IN} = 5V/9V/12V/15V/20V, V_{BATT} = 8V,
f_{SW} = 425kHz, BFET: SISA14DN



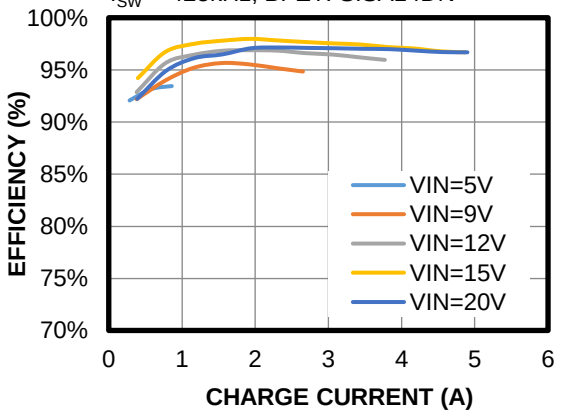
Efficiency vs. Charge Current

V_{IN} = 5V/9V/12V/15V/20V, V_{BATT} = 12V,
f_{sw} = 435kHz, BFET: SISA14DN



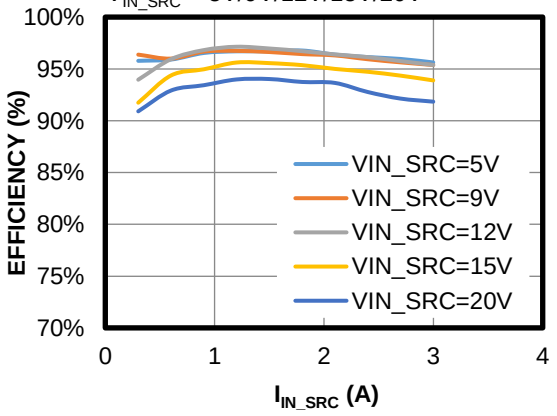
Efficiency vs. Charge Current

V_{IN} = 5V/9V/12V/15V/20V, V_{BATT} = 16V,
f_{SW} = 425kHz, BFET: SISA14DN



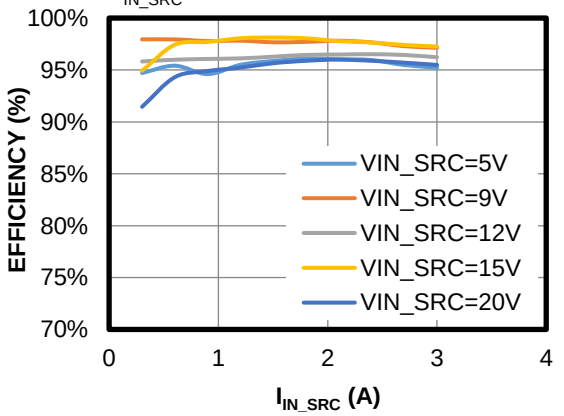
Efficiency vs. I_{IN_SRC}

V_{BATT} = 8.4V, f_{SW} = 425kHz,
V_{IN_SRC} = 5V/9V/12V/15V/20V



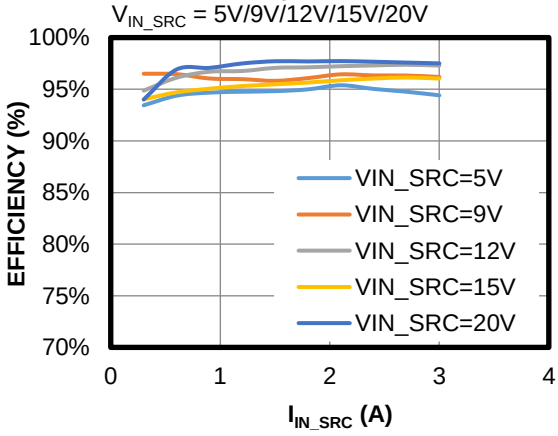
Efficiency vs. I_{IN_SRC}

V_{BATT} = 12.6V, f_{SW} = 425kHz,
V_{IN_SRC} = 5V/9V/12V/15V/20V



Efficiency vs. I_{IN_SRC}

V_{BATT} = 16.8V, f_{SW} = 425kHz,
V_{IN_SRC} = 5V/9V/12V/15V/20V

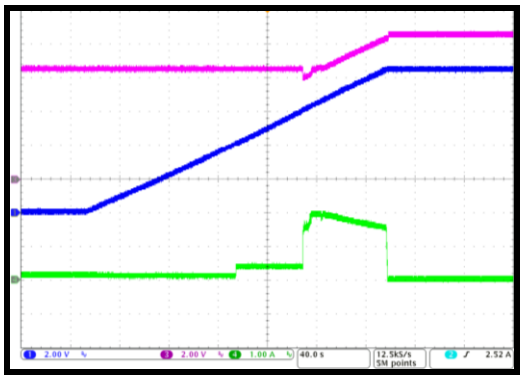


TYPICAL PERFORMANCE CHARACTERISTICS

C_{IN} = 10µF x 3pcs, C_{SYS} = 22µF x 2pcs, C_{BATT} = 22µF x 2pcs, L = 4.7µH, f_{SW} = 425kHz, I_{IN_LIM} = 5000mA, I_{CC} = 3000mA, 2-cell application, V_{BATT_REG} = 8.4V, unless otherwise noted.

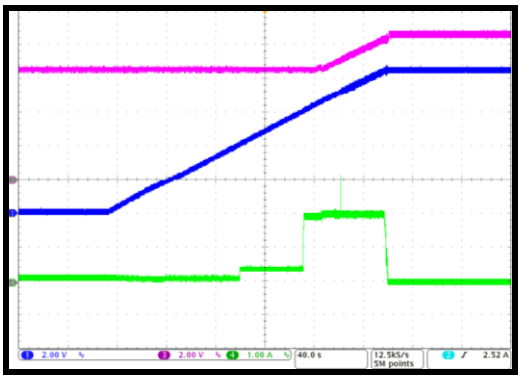
Charge Profile

5V/3A input, V_{BATT_REG} = 8.4V (2-cell), I_{CC} = 2A, battery simulator with 10mV/step



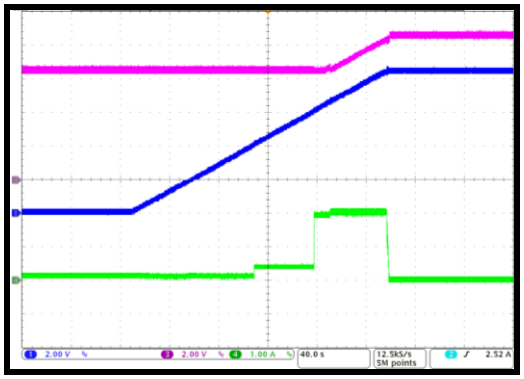
Charge Profile

9V/3A input, V_{BATT_REG} = 8.4V (2-cell), I_{CC} = 2A, battery simulator with 10mV/step



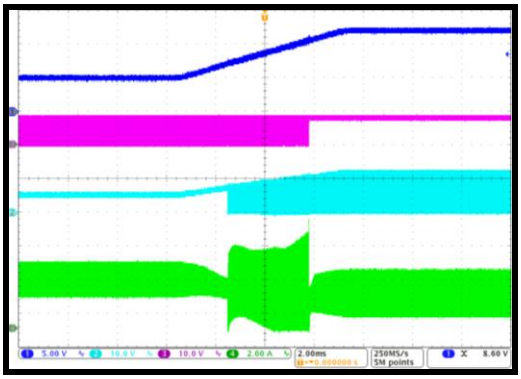
Charge Profile

20/3A input, V_{BATT_REG} = 8.4V (2-cell), I_{CC} = 2A, battery simulator with 10mV/step



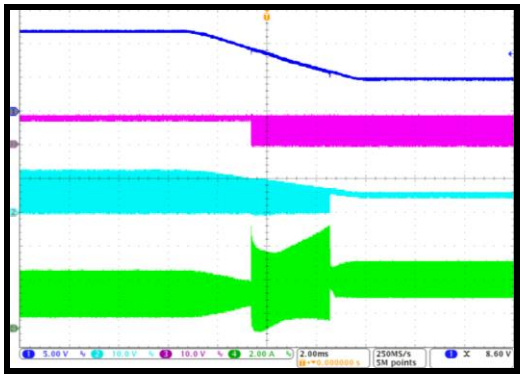
V_{IN} Stepping from 5V to 12V

V_{BATT} = 7.6V (2-cell), I_{CC} = 2A, charge enabled



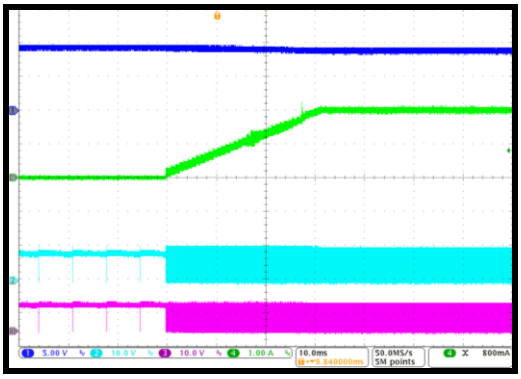
V_{IN} Stepping from 12V to 5V

V_{BATT} = 7.6V (2-cell), I_{CC} = 2A, charge enabled



Charge Enabled

9V input, V_{BATT} = 7.4V (2-cell), I_{CC} = 2A

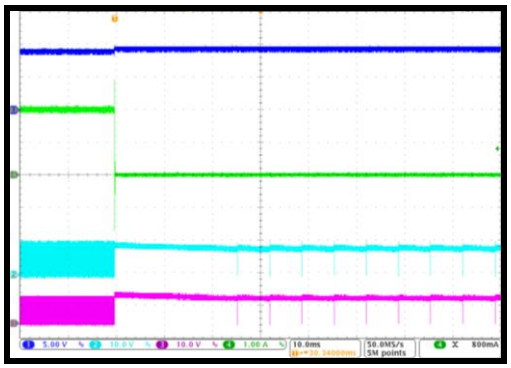


TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

C_{IN} = 10µF x 3pcs, C_{SYS} = 22µF x 2pcs, C_{BATT} = 22µF x 2pcs, L = 4.7µH, f_{SW} = 425kHz, I_{IN_LIM} = 5000mA, I_{CC} = 3000mA, 2-cell application, V_{BATT_REG} = 8.4V, unless otherwise noted.

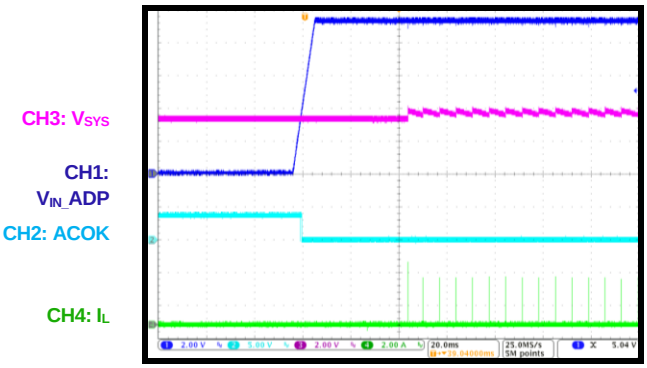
Charge Disabled

9V input, 7.4V (2-cell) and 2A charge



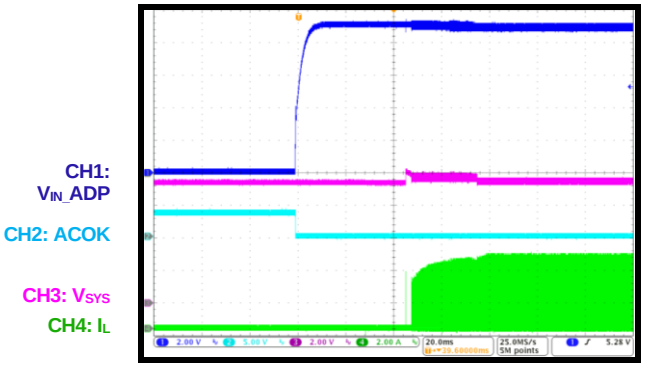
Start-Up through VIN

9V input power on, V_{BATT} = 7.4V (2-cell), I_{CC} = 2A, charge disable, I_{SYS} = 0A



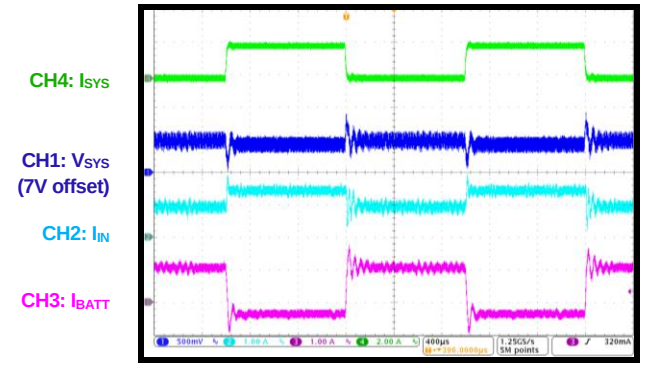
Start-Up through VIN

9V input power on, V_{BATT} = 7.4V (2-cell), I_{CC} = 2A, charge enabled, I_{SYS} = 0A



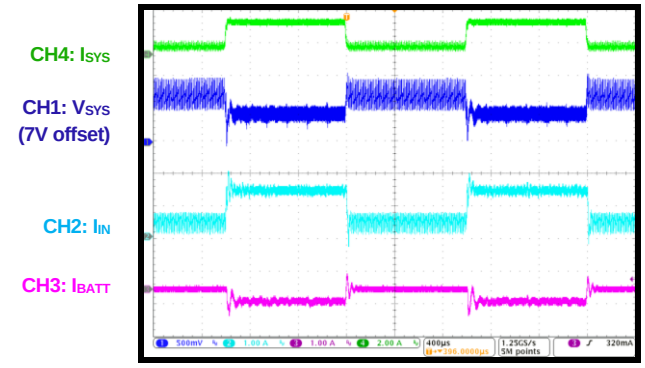
I_{IN_MIN} Transient Response

9V input, I_{IN_MIN} = 1.5A, V_{BATT} = 7.4V (2-cell), I_{CC} = 1A, charge enabled, I_{SYS} = 0A to 2A



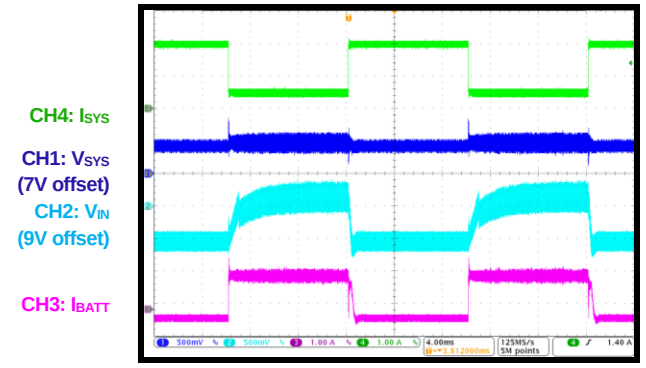
I_{IN_LIM} Transient Response

9V input, I_{IN_MIN} = 1.5A, V_{BATT} = 7.4V (2-cell), charge disabled, I_{SYS} = 0.5A to 2A



V_{IN_MIN} Transient Response

9V/1A input, V_{IN_MIN} = 8.4V, V_{BATT} = 7.4V (2-cell), I_{CC} = 1A, charge enabled, I_{SYS} = 0.5A to 2A

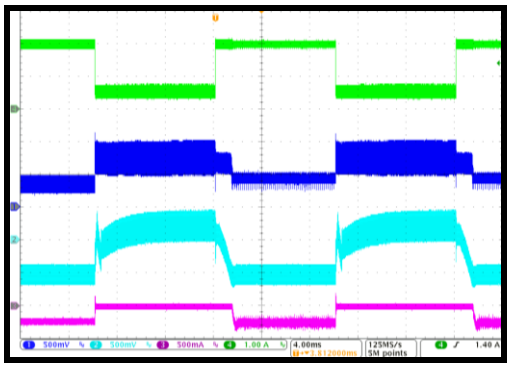


TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

C_{IN} = 10µF x 3pcs, C_{SYS} = 22µF x 2pcs, C_{BATT} = 22µF x 2pcs, L = 4.7µH, f_{SW} = 425kHz, I_{IN_LIM} = 5000mA, I_{CC} = 3000mA, 2-cell application, V_{BATT_REG} = 8.4V, unless otherwise noted.

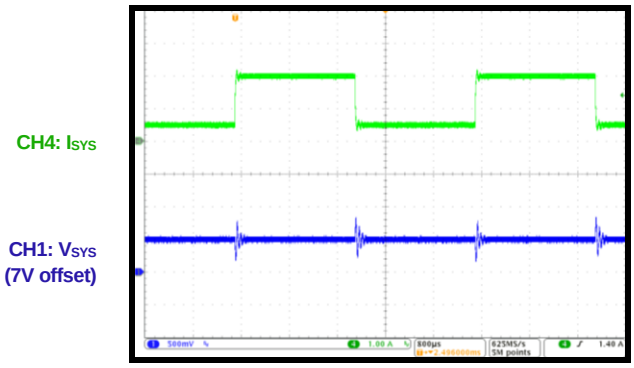
V_{IN_MIN} Transient Response

9V/1A input, V_{IN_MIN} = 8.4V, V_{BATT} = 7.4V (2-cell), I_{CC} = 1A, charge disabled, I_{SYS} = 0.5A to 2A



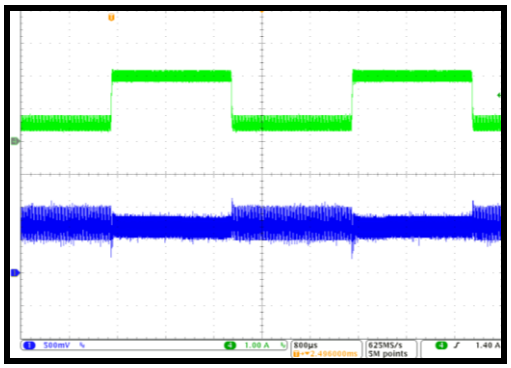
System Load Transient

5V input, V_{BATT} = 7.4V (2-cell), charge disabled, I_{SYS} = 0.5A to 2A



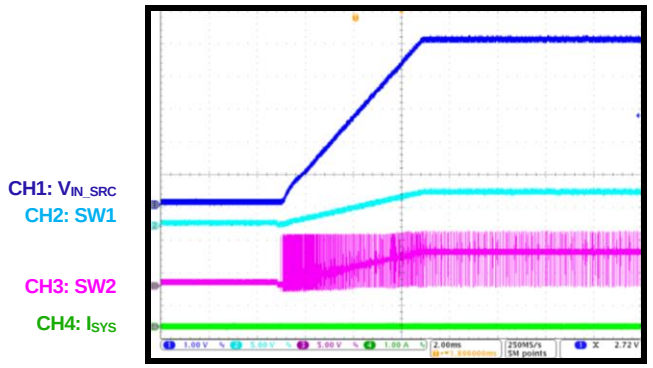
System Load Transient

9V input, V_{BATT} = 7.4V (2-cell), charge disabled, I_{SYS} = 0.5A to 2A



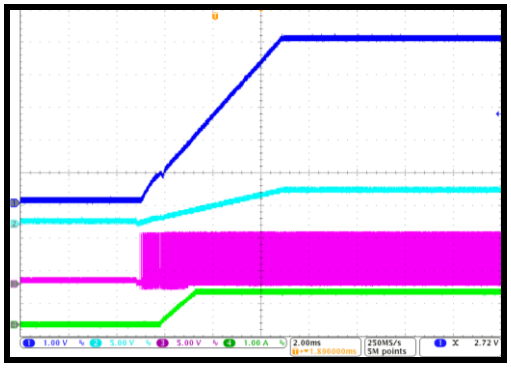
V_{IN_SRC} Start-Up in Source Mode

V_{BATT} = 7.4V (2-cell), V_{IN_SRC} = 5V, no load current



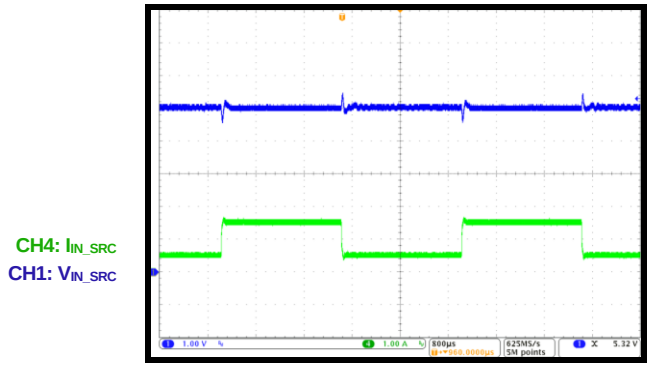
V_{IN_SRC} Start-Up in Source Mode

V_{BATT} = 7.4V (2-cell), V_{IN_SRC} = 5V, 1A load current



Load Transient in Source Mode

V_{BATT} = 7.4V (2-cell), V_{IN_SRC} = 5V, load current between 0.5A and 1.5A

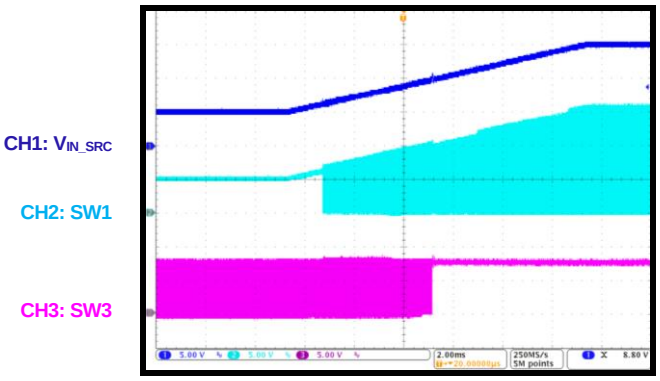


TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

C_{IN} = 10µF x 3pcs, C_{SYS} = 22µF x 2pcs, C_{BATT} = 22µF x 2pcs, L = 4.7µH, f_{SW} = 425kHz, I_{IN_LIM} = 5000mA, I_{CC} = 3000mA, 2-cell application, V_{BATT_REG} = 8.4V, unless otherwise noted.

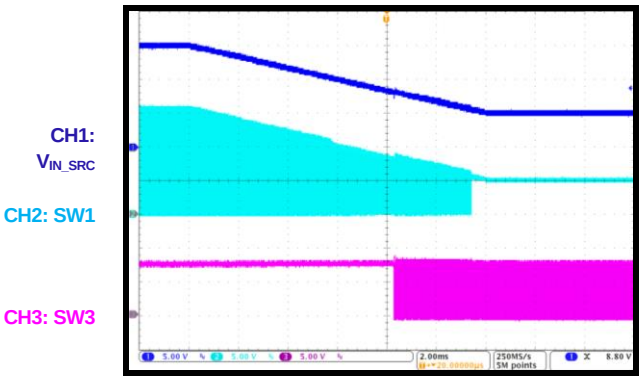
V_{IN_SRC} Stepping from 5V to 15V

V_{IN_SRC} from 5V to 15V, 1A load current



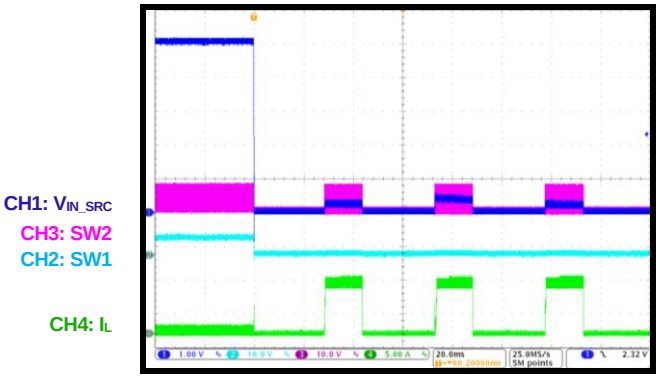
V_{IN_SRC} Stepping from 15V to 5V

V_{IN_SRC} from 15V to 5V, 1A load current



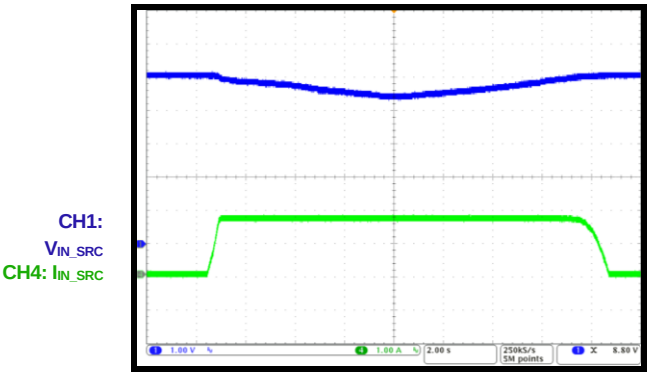
V_{IN_SRC} Short in Source Mode

V_{BATT} = 7.4V (2-cell), V_{IN_SRC} = 5V, no load current



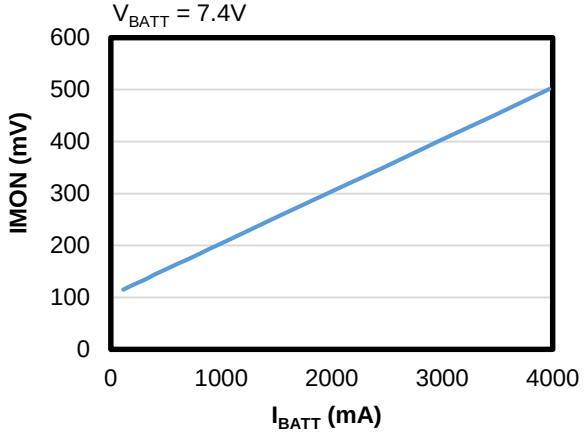
Output Current Limit in Source Mode

V_{BATT} = 7.4V (2-cell), V_{IN_SRC} = 5V, I_{IN_SRC} = 2A



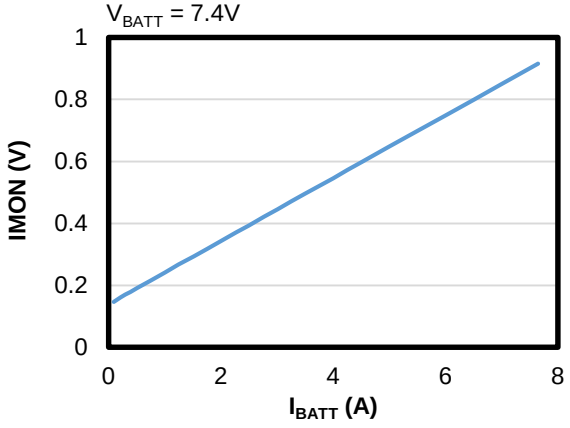
IMON Indicating I_{BATT} in Charge Mode

V_{BATT} = 7.4V



IMON Indicating I_{BATT} in Discharge Mode

V_{BATT} = 7.4V



FUNCTIONAL BLOCK DIAGRAM

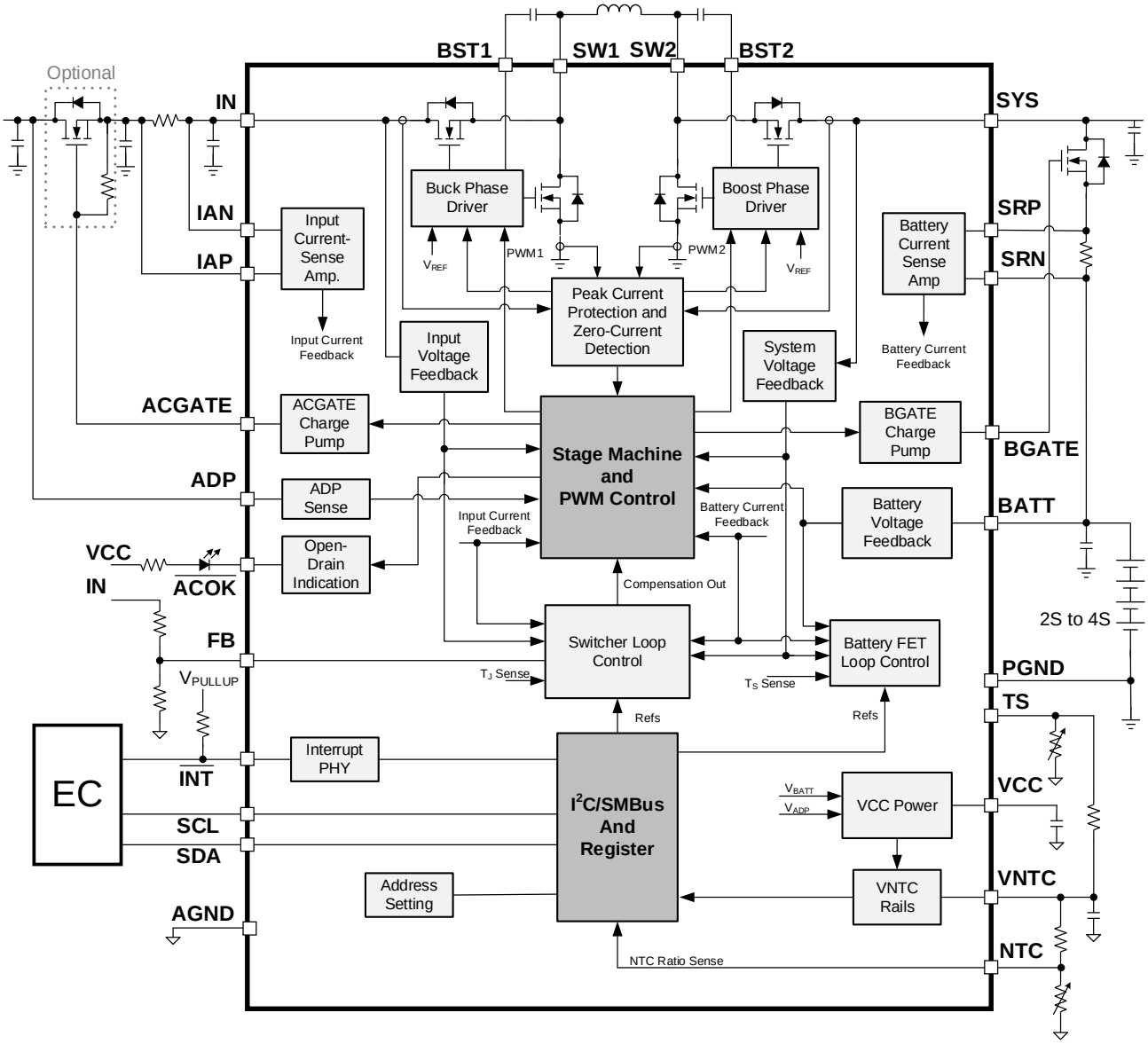


Figure 2: Functional Block Diagram

OPERATION

Introduction

The MP2761 is a highly integrated buck-boost charger IC with four switching FETs (Q1, Q2, Q3, and Q4) for battery packs with 2 to 4 cells in series. It also integrates two N-channel MOSFET drivers for input voltage pass-through, input over-voltage protection (ADP OVP), and narrow-voltage DC (NVDC) power path control.

The MP2761 can operate in reverse to power the input from the battery. This function is compliant with USB power delivery (PD) source mode.

When input power is present, the MP2761 operates in charge mode. The buck-boost converter has three operating modes:

- Boost mode when the input voltage (V_{IN}) is below the sys voltage (V_{SYS}).
- Buck mode when V_{IN} exceeds V_{SYS}.
- Buck-boost mode when V_{IN} is almost equal to V_{SYS}.

Figure 3 shows the MP2761's power structure.

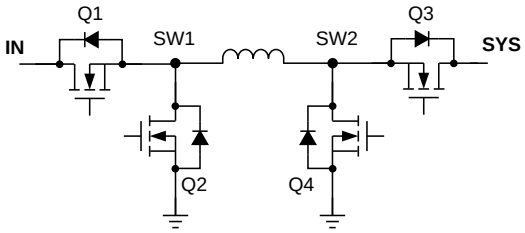


Figure 3: Power Stage of the MP2761

Table 1 shows the MOSFETs' operation in charge mode.

Table 1: MOSFETs' Operation in Charge Mode

MOSFET	Boost	Buck-Boost	Buck
Q1	On	Switching	Switching
Q2	Off	Switching	Switching
Q3	Switching	Switching	On
Q4	Switching	Switching	Off

Table 2 shows the MOSFETs' operation in source mode.

Table 2: MOSFETs' Operation in Source Mode

MOSFET	Boost	Buck-Boost	Buck
Q1	Switching	Switching	On
Q2	Switching	Switching	Off
Q3	On	Switching	Switching
Q4	Off	Switching	Switching

When the input is absent, the device operates in reverse to power the input from the battery via I²C/SMBus control. The MP2761 can provide a 4 to 21V output voltage (V_{IN_SRC}), with 20mV/step at the input. The device also has an output current limit (I_{IN_SRC}) with 50mA/step in this mode. Generally, this mode is called source mode in USB PD applications.

When the input is absent and source mode is disabled, the MP2761 operates in battery only mode if the default register setting is selected. In this mode, Q1–Q4 are turned off, and the system is powered by the battery via the external battery FET (BATFET).

VCC Low-Dropout (LDO) Regulator Output

The MP2761 integrates a low-dropout (LDO) regulator to power the internal circuit, including the I²C block, FET driver, and bias current. The LDO can also pull up open drains, such as the $\overline{ACOK}$ and $\overline{INT}$ pins.

VCC is powered by the ADP pin's voltage (V_{ADP}) or V_{BATT}. When V_{ADP} exceeds the under-voltage lockout threshold (V_{ADP_UVLO}), VCC is powered by V_{ADP}, regardless of whether the MP2761 is in charge mode or source mode. When the input is absent or V_{ADP} is below V_{ADP_UVLO}, VCC is powered by V_{BATT} while $V_{BATT} > V_{BATT\_UVLO}$.

Input Power Status Indication

The MP2761 has both an $\overline{ACOK}$ pin and PG_STAT (REG16h, bit[13]) to indicate whether the input power supply is present. The $\overline{ACOK}$ pin is an open-drain structure that is pulled to AGND when V_{IN} exceeds its under-voltage protection (UVP) threshold and is below its over-voltage protection (OVP) threshold ($V_{IN\_UVP} < V_{IN} < V_{IN\_OVP}$).

The MP2761 also has a status register (PG_STAT) that reports whether V_{IN} is within its normal operation range. This status is only valid in charge mode. It is set to 1 when V_{IN} exceeds V_{IN_UVP} but is below V_{IN_OVP}.

Input Over-Voltage Protection (OVP)

The MP2761 provides two input OVP thresholds: V_{ADP_OVP} and V_{IN_OVP}. The ADP pin senses the input voltage. If $V_{ADP} > V_{ADP\_OVP}$, the

ACGATE pin pulls down to turn off M1 immediately (see Figure 4).

Meanwhile, the buck-boost converter turns off. The MP2761 reports the ADP OVP fault via VADP_OV (REG17h, bit[12]). There is a 100ms deglitch time to recover from an ADP OVP fault.

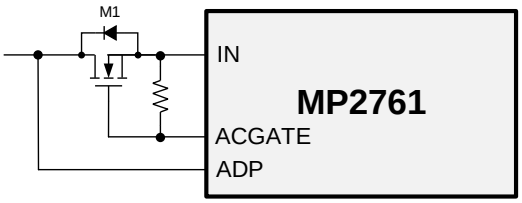


Figure 4: ACGATE Driver

When V_{IN_OVP} < V_{IN} < V_{ADP_OVP}, M1 turns on and the MP2761's switches are disabled. Then a fault is reported via VIN_OV (REG17h, bit[13]).

Input Current Limit and Input Voltage Limit Regulation

To meet the maximum current limit in the USB specification and avoid overloading the adapter, the MP2761 has both I_{IN} limit and V_{IN} limit regulation. If either the I_{IN} limit or V_{IN} limit is reached, the MP2761 regulates the duty cycles of Q1 and Q4 to limit the input power according to the setting.

Narrow-Voltage DC (NVDC) Power Path Management

The MP2761 provides a BGATE driver to support NVDC power path management. The BGATE driver is disabled by REG12h, bit[5] = 0 The BGATE driver provides the following features:

- The system instantly starts up after the input power turns on when V_{BATT} is low.
- The system voltage (V_{SYS}) stays almost equal to V_{BATT} to allow to use of a low-voltage point-of-load (POL).
- The battery can supplement the system power when the input power is limited.
- When the input is present, the system takes power from the input after charge termination.

Figure 5 shows the NVDC power path structure.

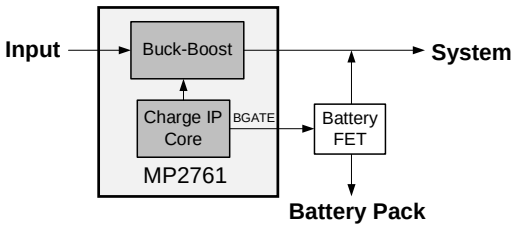


Figure 5: NVDC Power Path Management Structure

The MP2761 can regulate V_{SYS} at a minimum level, even when the battery is depleted. The MP2761 has a V_{SYS_MIN} setting. When charging is disabled (BATFET is off), V_{SYS} is regulated above the maximum values (V_{SYS_MIN}, V_{BATT}) by V_{TRACK}. When V_{BATT} > V_{SYS_MIN}, V_{SYS} always tracks the real battery voltage (see Figure 6).

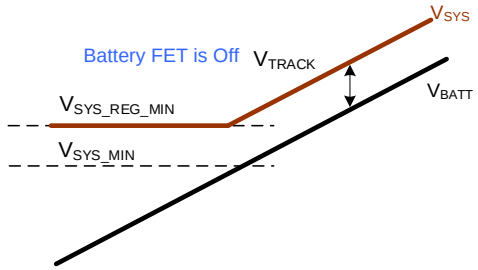


Figure 6: System Voltage Tracking

When charging is enabled and V_{BATT} > $V_{SYS\_REG\_MIN}$ (V_{SYS_MIN} + V_{TRACK}), the BATFET fully turns on. In this scenario, the charge current loop and battery voltage loop are implemented by the buck-boost converter's PWM control (see Figure 7).

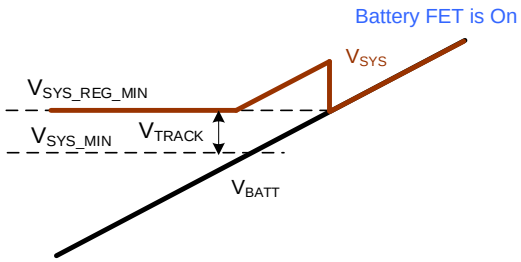


Figure 7: System Voltage Regulation

When charging is enabled and V_{BATT} < $V_{SYS\_REG\_MIN}$, the BATFET in linear mode(saturation region). The buck-boost converter controls the input current, input voltage, and system voltage. Meanwhile, BGATE controls the charge current loop (trickle current charge, pre-charge, and linear CC charge).

Table 3 on page 23 summarizes loop control.

Table 3: MP2761 Loop Control Summary

Condition	DC/DC EA	BGATE
V_{BATT} > $V_{SYS\_REG\_MIN}$	• I_{CC} • V_{BATT_REG} • I_{IN_LIM} • V_{IN_MIN} • T_{J_REG}	• V_{FWD}
V_{BATT} < $V_{SYS\_REG\_MIN}$	• $V_{SYS\_REG\_MIN}$ • I_{IN_LIM} • V_{IN_MIN}	• I_{TC} • I_{PRE} • I_{CC} • T_{J_REG} • V_{FWD}
Charge Disabled	• V_{SYS_REG} • I_{IN_LIM} • V_{IN_MIN}	• V_{FWD}

Active Current Foldback

When V_{IN} is sufficiently high and V_{BATT} is below $V_{SYS\_REG\_MIN}$, the system voltage is regulated at $V_{SYS\_REG\_MIN}$, and BATFET works linearly to charge the battery with a trickle charge current, pre-charge current, or constant charge current.

If the input current limit or input voltage limit is reached while the system load increases, V_{SYS} drops. Once V_{SYS} drops by 210mV/cell, BGATE pulls down to reduce the charge current and ensure that the system's power requirements are prioritized.

Battery Supplement Mode

When I_{IN} or V_{IN} is limited, the charge current is reduced to prevent I_{IN} or V_{IN} from dropping further. If the input source is still overloaded when the charge current has dropped to zero, V_{SYS} continues to fall. When V_{SYS} falls below the battery voltage (V_{SYS} < V_{BATT} - 30mV), the IC enters battery supplement mode. In battery supplement mode, the system load is powered by the battery and DC/DC converter simultaneously.

Virtual Diode Mode Control

Virtual diode mode is designed to optimize the control transition between the battery and the buck-boost converter. In virtual diode mode, BGATE regulates the BATFET's source-to-drain voltage (V_{SD}) under light discharge current conditions from the battery to the system. The virtual diode mode block is only valid when the input is present.

A comparator compares V_{SYS} to V_{BATT} to determine when the device should enter or exit virtual diode mode. When V_{SYS} < V_{BATT} - 30mV, virtual diode mode is enabled, and BGATE regulates V_{SD} to V_{FWD} (about 24mV). As the discharge current increases, the battery's gate drive increases while R_{DS} decreases, until the BATFET is fully on. When the system load current drops, V_{SYS} rises above V_{BATT}. The device exits virtual diode mode when V_{SYS} > V_{BATT} + 30mV.

Battery Charge Profile

In charge mode, the MP2761 regulates six control loops: V_{IN}, I_{IN}, charge current, battery-full regulation voltage, system voltage, and the device's junction temperature.

Re-plugging the input power or toggling the battery charging control bit (REG12h, bit[0]) can restart a new charge cycle without any of below faults:

- Thermistor fault
- Safety timer fault
- Battery over-voltage (OV) fault
- The BATFET forced off

The new charge cycle can start with any phase because the phase depends on V_{BATT}.

The device provides four main charging phases: constant current trickle charge, constant current pre-charge, constant current (CC) fast charge, and constant voltage (CV) charge (see Figure 8 on page 24).

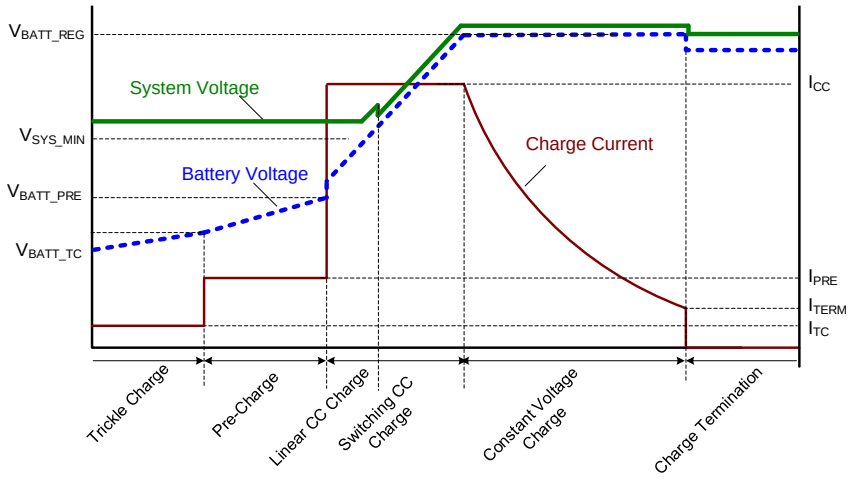


Figure 8: Charge Profile in NVDC Mode

Constant Current Trickle Charge (Phase 1):

When the input power qualifies as a good power supply, the IC checks V_{BATT} to determine whether trickle-charging is required. If V_{BATT} is below the trickle charge to pre-charge threshold (V_{BATT_TC}), a configurable trickle charging current is applied to the battery.

Constant Current Pre-Charge (Phase 2)

When V_{BATT} exceeds V_{BATT_TC}, the IC starts to safely pre-charge the deeply depleted battery until V_{BATT} reaches the pre-charge to fast charge threshold (V_{BATT_PRE}). If V_{BATT_PRE} is not reached before the linear charge timer (about 2 hours) expires, the charge cycle ends, and a corresponding timeout fault signal asserts. The pre-charge current can be configured via the I^2C register REG0Fh, bits[7:4], while V_{BATT_PRE} can be configured via REG0Bh, bit[12]. There are two options for this threshold: 2.5V/cell for $LiFePO_4$ batteries, and 3V/cell for Li-ion batteries.

Constant Current Fast Charge (Phase 3)

When V_{BATT} exceeds V_{BATT_PRE} (set via REG0Bh, bit[12]), the IC enters the constant current fast charge phase. The constant current charge has two different charge modes:

- Linear charge mode when $V_{BATT\_PRE} < V_{BATT} < V_{SYS\_REG\_MIN}$.

  In linear charge mode, V_{SYS} is regulated at $V_{SYS\_REG\_MIN}$, and the charge current loop is implemented by BGATE.

- Switching charge mode when $V_{BATT} > V_{SYS\_REG\_MIN}$.

  In switching charge mode, the BATFET is fully on and the charge current loop is implemented by the converter's PWM.

The fast charge current can be configured via REG14h, bits[13:6].

Constant Voltage Charge (Phase 4)

When V_{BATT} reaches the level of the configurable battery-full voltage (V_{BATT_REG}, set via REG15h, bits[14:4]), the charge current begins to taper off.

The charge cycle is considered complete when the charge current reaches the termination threshold (I_{TERM}, set via REG0Fh, bits[3:0]), assuming the termination function is enabled. If I_{TERM} is not reached before the safety charge timer expires, then the charge cycle ends and a corresponding timeout fault signal is asserted (see the Safety Timer section on page 26 for more details).

Table 4 on page 25 shows the battery-fully voltage range for different cells.

Table 4: Battery-Full Voltage Range at Different Cells

Cell No.	Battery Full Voltage Range	$V_{BATT\_REG\_MIN}$			$V_{BATT\_REG\_MAX}$		
		V_{BATT_REG} (mV)	Reg 15h, Bits[14:4] (Dec)	Reg 15h (Hex)	V_{BATT_REG} (mV)	Reg 15h, Bits[14:4] (Dec)	Reg 15h (Hex)
2-cell	6.8V to 9.34V	6800	680	0x2A80	9340	934	0x3A60
3-cell	10.2V to 14.01V	10200	1020	0x3FC0	14010	1401	0x5790
4-cell	13.6V to 18.68V	13600	1360	0x5500	18680	1868	0x74C0

Automatic Recharge

When the battery is full charged and charging is terminated, the battery may be discharged due to the self-discharge. When V_{BATT} falls below the configurable recharge threshold, the IC automatically starts a new charging cycle, without needing to manually restart a charging cycle if the input power is valid. The charge timer resets when the automatic recharge cycle begins.

Battery Over-Voltage Protection (OVP)

The IC has battery OVP. If V_{BATT} exceeds the battery OV threshold (230mV higher than the battery regulation voltage per cell), charging is disabled. Battery OVP has a 30ms deglitch time. Under this condition, the BATFET turns off and V_{SYS} is regulated at V_{TRACK} + V_{BATT_REG}.

Junction Temperature (T_J) Regulation

The thermal regulation loop always monitors the IC's internal junction temperature (T_J). If the internal T_J exceeds the temperature limit, the charge current is reduced to keep T_J at the regulated threshold. The multiple thermal regulation thresholds (from 80°C to 120°C) help the system design meet the thermal requirement for different applications. The junction temperature's regulation threshold can be set via REG0Fh, bits[14:12].

Transition Between Buck, Buck-Boost and Boost

The MP2761 always monitors the IN and SYS pin voltages to automatically switch between different modes (see Figure 9).

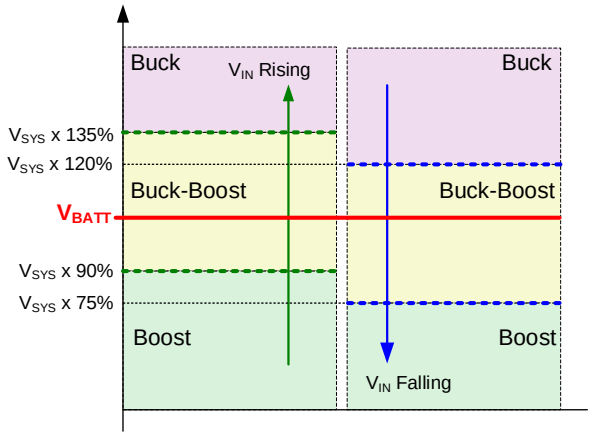


Figure 9: Mode Transition Threshold

When V_{IN} > 90% of V_{SYS}, the MP2761 transitions from boost mode to buck-boost mode.

When V_{IN} < 75% of V_{SYS}, the MP2761 transitions from buck-boost mode to boost mode.

When V_{IN} < 120% of V_{SYS}, the MP2761 transitions from buck mode to buck-boost mode.

When V_{IN} > 135% of V_{SYS}, the MP2761 transitions from buck-boost mode to buck mode.

Pulse-Skip Mode (PSM)

The MP2761 utilizes pulse-skip mode (PSM) control to improve the efficiency under light loads. In PSM, lighter loads mean the device skips more pulse width.

Ultrasonic Mode (USM) Operation

The MP2761 provides ultrasonic sound mode (USM) control to ensure the switching pulse interval exceeds 30kHz; this can be disabled by setting REG07h, bit[8] = 0.

Cycle-by-Cycle MOSFET Current Limit

The MP2761 senses both the high-side and low-side MOSFET (HS-FET and LS-FET,

respectively) currents. During loop control, the device provides a valley current limit in buck mode and a peak current limit in boost mode for each cycle-by-cycle switching period. In buck mode, the next period does not start until the inductor current (I_L) drops to the valley current limit. Then I_L rises during the minimum on time to fold back the frequency after triggering the valley current limit.

System Voltage Protection

The MP2761 has both over-voltage protection (OVP) and under-voltage protection (UVP) for system voltage regulation.

System Over-Voltage Protection (OVP)

When $V_{SYS} > V_{SYS\_OV}$ (configurable via REG11h, bits[14:13]), the PWM is disabled, and a system OV fault is reported in the status and fault register. The device recovers when V_{SYS} is below V_{SYS_OV} with a hysteresis.

System Under-voltage Protection (UVP)

When V_{SYS} is below the SYS UV threshold for 10ms, the switcher stops and automatically recovers to the starting point after 375ms. In addition to the 375ms off time, the MP2761 always has a 30ms delay between when the switcher is enabled and the pulse-width modulation (PWM) begins operating.

Analog-to-Digital Converter (ADC) Conversion and Multiplexer

The MP2761 integrates a built-in, 10-bit SAR analog-to-digital converter (ADC) with 50kSPS. A 10-channel multiplexer measures the device's parameters (see Table 5).

Table 5: ADC Channels

Sink Mode	Source Mode
• V_{IN} • I_{IN} • V_{SYS} • V_{BATT} • Charge current • Battery temperature (NTC pin voltage ratio) • TS pin voltage ratio • Chip junction temperature	• V_{IN_SRC} • I_{IN_SRC} • V_{SYS} • V_{BATT} • Battery discharge current • Battery temperature. • TS pin voltage ratio • Chip junction temperature

When the MP2761 works in charge mode and source mode, the ADC operates automatically. The ADC keeps running and each parameter is converted to a digital value every 370µs. When only the battery is present, the ADC operates when ADC_CONV (REG0Eh, bit[7]) is set to 1.

Safety Timer

The IC provides both a linear charge timer and switching constant current/constant voltage (CC/CV) timer to prevent an extended charging cycle due to abnormal battery conditions. The total safety timer for linear charge (including trickle charge, pre-charge, and linear CC charge) is 2 hours when V_{BATT} is below $V_{SYS\_REG\_MIN}$.

The switching CC/CV charge safety timer starts when the battery enters the switching CC charging phase. The user can configure this time via REG12h, bits[12:11].

Above two safety timers can be disabled via REG12h, bit[13]. The safety timer does not operate in the discharge mode.

The safety timer is reset at the beginning of a new charging cycle. The following actions restart the safety timer:

- Automatic recharge (reset when charging ends, restarts when the recharge cycle begins).
- Charge enable toggling (reset when charging is disabled, restarts when charging is enabled).
- Input power toggling (reset if input UVP or OVP occurs, restarts when PG_STAT = 1).
- USB suspend mode toggling (reset when the converter is disabled, restarts when the converter is enabled).
- Safety timer toggling (reset when the timer is disabled, restarts when the timer is enabled again).
- Thermal shutdown recovery (reset during thermal shutdown, restarts during thermal shutdown recovery).

The IC automatically suspends the timer if either of the following situations occur:

- Battery supplement mode is initiated.
- An NTC hot or cold fault.

During input voltage, current, or thermal regulation when the device does not enter battery supplement mode, the safety timer counts at a half-clock rate because the actual charge current is likely to be below the register setting. For example, if the charger is in input current limit regulation (IIN_LIM_STAT = 1) throughout the entire charging cycle, and the safety timer is set to 20 hours, then the timer expires in 40 hours. Once the IC resolves the above events, the timer returns to its standard clock rate. This half-clock rate feature can be disabled via REG12h, bit[10].

Watchdog Timer

The MP2761 has a watchdog timer to monitor the I²C interface. If the watchdog timer is enabled, the host must periodically reset the watchdog timer reset bit(REG12h,bit[9]) before the watchdog timer expires. If the watchdog timer expires, certain registers are reset to their default values. See the Register Map starting on page 32 to determine which registers are reset after the watchdog timer expires.

The following actions reset the watchdog timer and force the device to recover from a watchdog timer fault:

- Write to the watchdog timer reset bit.
- Write to the charge current register (REG14h).
- Write to the battery regulation voltage register (REG15h).

The watchdog timer can be disabled via REG12h, bits[8:7].

Battery Temperature Monitoring via the Negative Temperature Coefficient (NTC) Thermistor

Thermistor is the generic name given to thermally sensitive resistors. A negative temperature coefficient (NTC) thermistor is generally called a thermistor. Depending on the manufacturing method and the structure, there are many shapes and characteristics for a thermistor. Unless otherwise specified, the thermistor resistance values are classified at a standard temperature of 25°C. The resistance of a temperature is solely a function of its absolute temperature.

Refer to the thermistor's datasheet to obtain the relevant parameters. Calculate the relationship between the resistance and absolute temperature of a thermistor with Equation (1):

$$R_1 = R_2 \times e^{\beta \times \left(\frac{1}{T1} - \frac{1}{T2}\right)} \quad (1)$$

Where R_1 is the resistance at the absolute temperature T_1, R_2 is the resistance at the absolute temperature T_2, and β is a constant that depends on the thermistor's material.

The MP2761 continuously monitors the battery's temperature by measuring the voltage at the NTC pin (V_{NTC}). This voltage is determined by the resistor divider since its ratio is produced by the NTC thermistor's resistance when the battery is under different temperatures (see Figure 10).

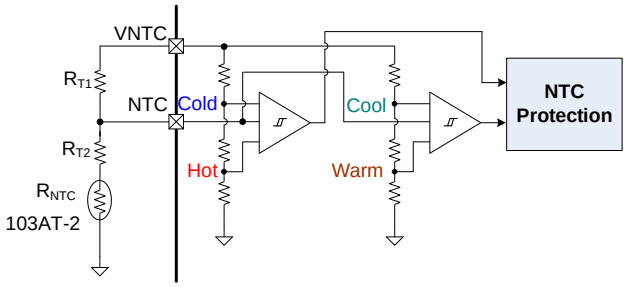


Figure 10: NTC Protection Circuit

The MP2761 internally sets a pre-determined upper and lower bound for the V_{NTC} range. If V_{NTC} goes out of this range, the temperature is outside of its safe operating limit. Then charging stops until the operating temperature returns into the safe range.

To satisfy the JEITA requirement, the MP2761 has four temperature thresholds: a cold battery threshold (0°C by default), a cool battery threshold (10°C by default), a warm battery threshold (45°C by default), and a hot battery threshold (60°C by default).

For a given NTC thermistor, these temperatures correspond to the V_{COLD}, V_{COOL}, V_{WARM}, and V_{HOT} thresholds, respectively. These values can be configured via REG0Dh, bits[7:0]. When $V_{NTC} < V_{HOT}$ or $V_{NTC} > V_{COLD}$, charging is suspended and the timers are suspended. When $V_{HOT} < V_{NTC} < V_{WARM}$ or when $V_{COOL} < V_{NTC} < V_{COLD}$, the charging behavior can be configured via REG0Ch, bits[14:4].

Figure 11 shows the JEITA control profile.

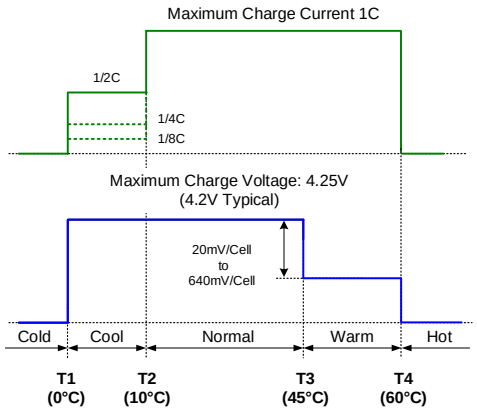


Figure 11: NTC Window

The MP2761 also monitors the battery temperature in discharge mode. If the NTC function is enabled, an interrupt (INT) asserts if the V_{NTC} is below the V_{HOT} threshold or exceeds the V_{COLD} threshold.

NTC Floating Detection

If V_{NTC} exceeds 95% of 1.28V, an NTC float is detected, INT asserts, and the corresponding status register changes. When the NTC is floating, BGATE turns off the external BATFET, and the system voltage is regulated to V_{BATT_REG} + V_{TRACK}.

Battery Missing Detection

The MP2761 counts how often charging terminates every 10s. If charge termination occurs more than three times in 10s, the MP2761 reports that the battery is missing via the status register and initiates an INT signal.

TS/IMON Pin Function

The MP2761 has a TS/IMON pin that monitors either the temperature monitoring (TS) or current monitoring (IMON). When REG10h, bit[12] = 0, this pin is configured for temperature monitoring (TS). When REG10h, bit[12] = 1, this pin is used for charge current monitoring.

Temperature Monitor (TS) Function

When the TS function is enabled, the TS/IMON pin can sense either the external BATFET temperature or the input USB connector temperature via REG0Dh, bits[14].

When the TS/IMON pin is configured to sense the input connector temperature, and the V_{TS_HOT} threshold (configured via REG0Dh, bits[12:10]) is reached, an INT signal asserts to indicate that a TS fault has occurred. In charging mode, the I_{IN} limit is reduced to 500mA with 50mA/step every 62.5ms. When the IC recovers from a TS fault, the I_{IN} limit rises to its set value with 50mA/step every 62.5ms.

When TS/IMON is configured to sense the BATFET temperature, and $V_{BATT} < V_{SYS\_REG\_MIN}$, the IC reduces the charging current if the BATFET temperature reaches the V_{TS_HOT} threshold. The INT signal asserts to indicate that thermal regulation has been initiated, though the INT signal can be masked via REG18h.

Current Monitor (IMON) Function

When the IMON function is used, the IMON pin indicates the real-time battery current with an offset of 0.1V and a gain of 0.1V/A in both charge and source mode.

Thermal Shutdown

The IC continuously monitors the internal T_J to maximize power delivery and avoid overheating the chip. When T_J reaches 150°C, the PWM converter shuts down. Normal operation does not resume until T_J drops below 120°C.

Host Mode and Default Mode

The IC is a host-controlled device. After VCC power-on reset (POR), all the registers are set to their default settings.

Any write to the IC forces it to host mode. All the device parameters can be configured by the host. To keep the device in host mode, the host has to reset the watchdog timer regularly by writing 1 to REG12h, bit[9] before the watchdog timer expires. If the watchdog timer expires, the IC goes back into default mode.

Impedance Compensation to Accelerate Charging

Throughout the entire charging cycle, the constant-voltage charging stage takes a longer time. To accelerate the charging cycle, it is recommended for the device to stay in the constant current fast charge stage for as long as possible.

The IC allows the user to compensate the intrinsic resistance of the battery by adjusting the battery regulation voltage according to the charge current and internal resistance.

In addition, a maximum allowed regulated voltage provides additional voltage ($V_{BATT\_REG\_ACT}$) that can be calculated with Equation (2):

$$V_{BATT\_REG\_ACT} = V_{BATT\_REG} + Min\ (V_{CLAMP},\ I_{CHG}\ x\ R_{BATT}) \quad (2)$$

Where $V_{BATT\_REG\_ACT}$ is the real battery regulation voltage, V_{BATT_REG} is the battery regulation voltage set via REG15h, bits[14:4], and I_{CHG} is the real-time charge current during the operation, and Min uses the lower value between V_{CLAMP} and (I_{CHG} x R_{BATT}).

Source Mode Operation

The MP2761 can operate in source mode to supply power to the IN pin using the battery. To ensure that the battery is not drained, the device does not enter this mode if the battery is below the configurable battery low threshold. Source mode operation can be enabled when REG12h, bit[3] = 1. When both charging and source mode are enabled, the source mode takes higher priority.

In source mode, the IC employs a fixed-frequency (375kHz to 770kHz, configurable) switching regulator. This regulator switches from PWM operation to PSM under light loads. This operation is similar to system voltage regulation in charge mode.

V_{IN_SRC} is compliant with USB PD specifications. It can be set to 5V, 9V, 12V, 15V, or 20V, with 20mV/step, via the digital-to-analog-converter (DAC) in the register or the external FB pin.

The I_{IN_SRC} limit can be configured via the I^2C/SMBus up to 5A, with 50mA/step. This is compliant with I^2C/SMBus specifications.

Source mode is enabled if the following conditions are met:

- $V_{BATT} > V_{BATT\_LOW}$
- REG12h, bit[3] = 1

To meet PD timing specifications, V_{IN_SRC} is settled within 275ms in source mode.

In source mode, the switcher can work in buck mode, boost mode, or buck-boost mode, according to V_{SYS} and the source V_{IN_SRC}.

Output Over-Voltage Protection (OVP) in Source Mode

The MP2761 features output OVP in source mode. The IC continuously monitors V_{IN_SRC} in source mode. If $V_{IN\_SRC} > V_{IN\_SRC\_OV}$, the PWM is disabled and an OV fault asserts in the status and fault registers. The PWM recovers once V_{IN_SRC} is lower than $V_{IN\_SRC\_OV}$ with a hysteresis (see the Electrical Characteristics section starting on page 12 for more details).

Output Short-Circuit Protection (SCP) in Source Mode

In addition to output OVP, the MP2761 features output short-circuit protection (SCP). When the load current reaches the IN output current limit (I_{IN_SRC}) in source mode, V_{IN_SRC} begins to fall. If V_{IN_SRC} falls below $V_{IN\_SRC\_UV}$ for more than 10ms, the IN output UVP fault asserts. The source mode is disabled for 30ms, then it restarts.

Battery Standby Mode

If only the battery is connected, the input source is absent, and the source mode is disabled, the VCC LDO stays on. When BGATE is disabled, ACGATE is disabled, the ADC is off, and the watchdog timer is disabled, the device's consumed current is 33μA ($I_{BATT\_STANDBY}$), which extends the batteries' runtime.

Battery Under-Voltage Protection (UVP)

The MP2761 has two types of battery under-voltage protection (UVP) in source mode. If $V_{BATT} < V_{BATT\_LOW}$ for 30ms, the MP2761 generates an INT signal to report that V_{BATT} is low, then the MP2761 turns off the buck-boost converter and latches the switcher off. Meanwhile, the external BATFET turns on to power the system from the battery. The user can configure the source mode behavior via REG0Bh, bit[11].

When REG0Bh, bit[11] = 0, source mode restarts automatically when V_{BATT} exceeds V_{BATT_LOW} with 200mV/cell. When REG0Bh, bit[11] = 1, source mode is latched, and the SRC_EN bit must be toggled to restart source mode.

The MP2761 also has a battery UVLO threshold. When V_{BATT} < 2.6V/cell, the switches stop and the BATFET turns off. When V_{BATT} >

(2.6V + 280mV)/cell, there is a 100ms deglitch time before the BATFET turns on.

SMBUS AND I²C COMPATIBILITY

The MP2761 has an SCL/SDA interface that is compatible with the SMBus/I²C interface. In addition, the MP2761's registers are 16 bits, which are compatible with both the SMBus and 16-bit I²C.

The system management bus (SMBus) is a two-wire, bidirectional serial interface, consisting of a data line (SDA) and a clock line (SCL). The lines are externally pulled to a bus voltage when they are idle. Connecting to the line, a initiator device generates the SCL signal and device address, then arranges the communication sequence. This is based on I²C operation principles.

The MP2761 interface is an SMBus target that supports both standard mode (100kHz) and fast mode (400kHz). The SMBus address is 0001 001x, where "x" is the read/write bit. The device receives control inputs from the initiator device, such as a microcontroller unit (MCU) or a digital signal processor.

Start and Stop Commands

All transactions begin with a start (S) command and are terminated by a stop (P) command. A start command is defined as a high-to-low transition on the SDA line while SCL is high. A stop command is defined as a low-to-high transition on the SDA line while the SCL is high (see Figure 12).

Start and stop commands are always generated by the initiator. The bus is considered busy after a start command; it is considered free after a stop command.

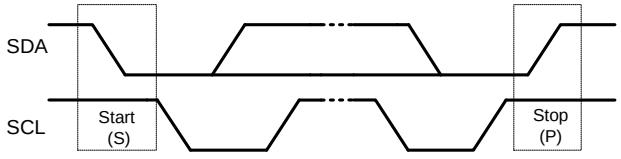


Figure 12: Start and Stop Commands

Data Validity

For data validity, the data on the SDA line must be stable during the high period of the clock. The high to low state of the SDA line can only change when the clock signal on the SCL line is low (see Figure 13).

When the bus is free, both lines are high. The SDA and SCL pins are open drains.

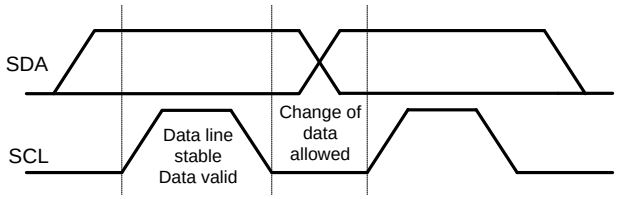


Figure 13: Data Validity

Interrupt to Host (INT)

The MP2761 has an alert mechanism that outputs an interrupt signal via the INT pin. If an interrupt is triggered, the device outputs a 256μs low-state INT pulse. The INT output is designed as an open-drain structure that must be externally pulled up to a voltage source for operation. The INT signal can be masked via the REG18h~19h registers.

SMBus Alert Response Address (ARA)

The SMBus alert response address (ARA) is a special address that can be used by the bus host.

If more than one target-only device is connected on the bus, and all the INT lines are connected together, a target-only device can signal to the host that it wants to talk through INT. The host processes the interrupt and simultaneously accesses all INT devices through the ARA. Only the device(s) that pull INT low to acknowledge the ARA.

The host performs a modified receive byte operation. The 7-bit device address provided by the target transmit device is placed in the 7 most significant bits (MSB) of the byte. The 8th bit can be a 0 or 1.

The SMBus ARA is 0001 100b.

Byte Format

Each byte on the SDA line must be 8 bits long. The number of bytes to be transmitted per transfer is unrestricted. Each byte must be followed by an acknowledge (ACK) bit. Data is transferred with the most significant bit (MSB) first.

The acknowledge takes place after every byte. The ACK bit allows the receiver to signal to the transmitter that the byte was successfully received, then another byte can be sent. All

clock pulses, including the acknowledge pulse (ninth clock pulse), are generated by the initiator (see Figure 14).

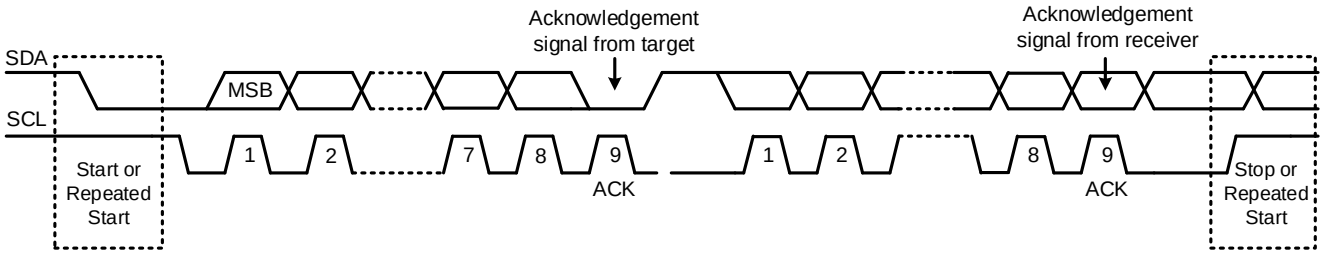


Figure 14: Acknowledge Bit

The transmitter releases the SDA line during the acknowledge clock pulse, so the receiver can pull the SDA line low. If the SDA line remains high during the ninth clock pulse; this is a not acknowledge (NACK) signal. The initiator can then generate either a stop command to abort the transfer or a repeated start command to start a transfer.

After the start command, a target address is sent. This address is 7 bits long, followed by an eighth data direction bit (R/W). A 0 indicates a transmission (write), and a 1 indicates a request for data (read). If the register address is not defined, the charger IC sends back NACK and returns to an idle state.

Figure 15, Figure 16, and Figure 17 show the complete data transfer.

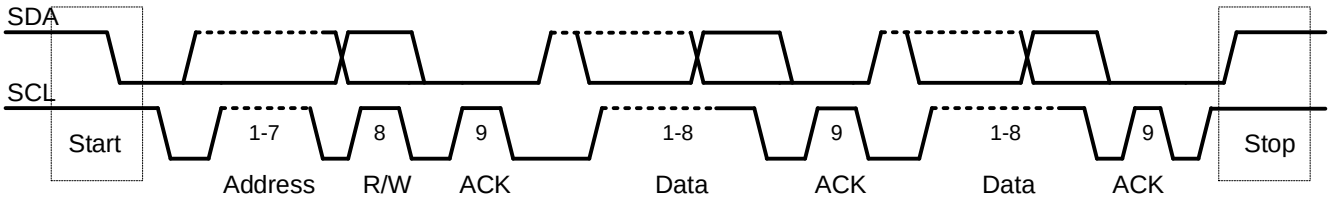


Figure 15: Byte Format

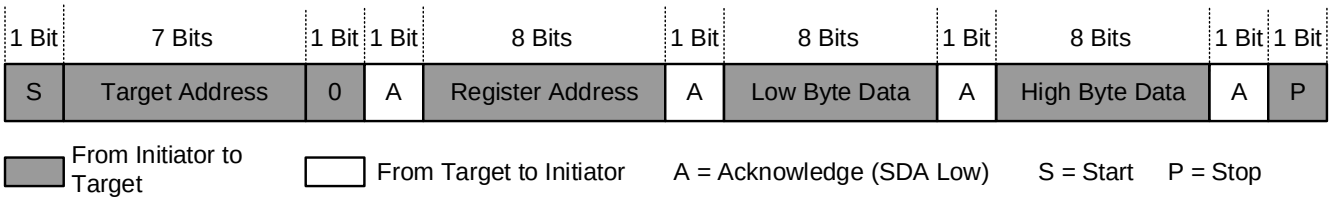


Figure 16: Single Word Write

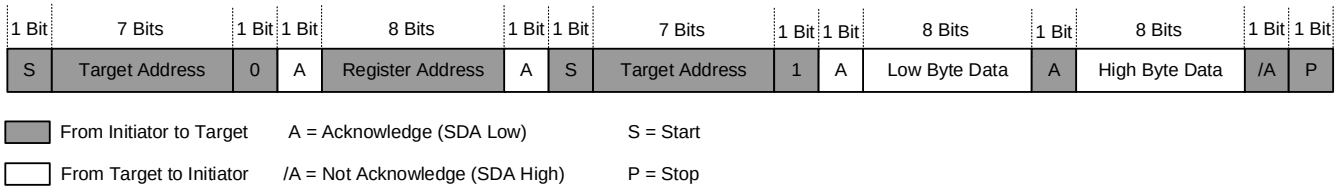


Figure 17: Single Word Read

REGISTER MAP

Register Name	Register Address	OTP (8)	R/W	Description
REG05h	0x05	Yes	R/W	Sets the device address. (9)
REG06h	0x06	Yes	R/W	Sets the input minimum voltage limit.
REG07h	0x07	Yes	R/W	Controls USM and sets the minimum system voltage.
REG08h	0x08	Yes	R/W	Sets the input current limit.
REG09h	0x09	No	R/W	Sets the IN output voltage in source mode.
REG0Ah	0x0A	No	R/W	Sets the battery impedance compensation and output current limit in source mode.
REG0Bh	0x0B	Yes	R/W	Sets the battery low voltage threshold and battery discharge current regulation in source mode.
REG0Ch	0x0C	No	R/W	Sets the JEITA action.
REG0Dh	0x0D	Yes	R/W	Sets the temperature protection.
REG0Eh	0x0E	Yes	R/W	Configuration register 0.
REG0Fh	0x0F	Yes	R/W	Configuration register 1.
REG10h	0x10	Yes	R/W	Configuration register 2.
REG11h	0x11	Yes	R/W	Configuration register 3.
REG12h	0x12	Yes	R/W	Configuration register 4.
REG14h	0x14	Yes	R/W	Sets the charge current.
REG15h	0x15	Yes	R/W	Sets the battery-regulation voltage.
REG16h	0x16	No	R	Status and fault register 0.
REG17h	0x17	No	R	Status and fault register 1.
REG18h	0x18	No	R/W	INT mask setting register 0.
REG19h	0x19	No	R/W	INT mask setting register 1.
REG23h	0x23	No	R	Returns the ADC result for the input voltage.
REG24h	0x24	No	R	Returns the ADC result for the input current.
REG25h	0x25	No	R	Returns the ADC result for the battery voltage.
REG26h	0x26	No	R	Returns the ADC result for the system voltage.
REG27h	0x27	No	R	Returns the ADC result for the battery charge current.
REG28h	0x28	No	R	Returns the ADC result for the NTC voltage ratio.
REG29h	0x29	No	R	Returns the ADC result for the TS voltage ratio.
REG2Ah	0x2A	No	R	Returns the ADC result for the junction temperature.
REG2Bh	0x2B	No	R	Returns the ADC result for the battery discharge current.
REG2Ch	0x2C	No	R	Returns the ADC result for the output voltage in discharge mode.
REG2Dh	0x2D	No	R	Returns the ADC result for the output current in discharge mode.

Notes:

8) “OTP” in this section means one-time programmable memory. For the bits specific to the OTP, see the register description.
9) The default device address is 69h.

REGISTER MAP FOR THE -0000 VERSION

REG05h

The REG05h register sets the device address, enables the watchdog, and selects the communication interface.

Bits	Access	Bit Name	Default	Description
15:10	R	RESERVED	0	Reserved.
9	R/W	WD_SET	1	When this bit is 0, the watchdog timer is automatically disabled when V_{IN} is absent. It is recommended to set this bit to 0. 0: Disabled 1: Enabled
8	R	TLOW_EN	0	To be compliant with the SMBus, the I^2C initiator pulls SCL low for longer than 25ms to make the device release SDA (reset the communication). This bit can be configured via the OTP. Default: 0 (I^2C) 0: Disabled (I^2C) 1: Enabled (SMBus)
7	R	RESERVED	1	Reserved.
6	R	ADDR[3]	1	Determines the highest 4 bits of the device's address. These bits can be configured via the OTP. Default: 0b1101
5	R	ADDR[2]	1	
4	R	ADDR[1]	0	
3	R	ADDR[0]	1	
2	R	RESERVED	0	Reserved.
1	R	RESERVED	0	Reserved.
0	R	RESERVED	1	Reserved.

REG06h

The REG06h register sets the input minimum voltage limit.

Bits	Access	Bit Name	Default	Description
15:8	R	RESERVED	0	Reserved.
7	R/W	V_{IN_MIN}[6]	0	Sets the minimum V_{IN} limit. These bits are reset when the watchdog is reset. These bits can be configured via the OTP. Range: 4V (0011 0010) ~ 20.4V (1111 1111) Default: 4.48V (0011 1000) LSB: 80mV V_{IN_MIN} = DEC(Bits[7:0]) x 80 (mV)
6	R/W	V_{IN_MIN}[6]	0	
5	R/W	V_{IN_MIN}[5]	1	
4	R/W	V_{IN_MIN}[4]	1	
3	R/W	V_{IN_MIN}[3]	1	
2	R/W	V_{IN_MIN}[2]	0	
1	R/W	V_{IN_MIN}[1]	0	
0	R/W	V_{IN_MIN}[0]	0	

REG07h

The REG07h register sets the system's minimum voltage limit and enables ultrasonic mode (USM).

Bits	Access	Bit Name	Default	Description
15:9	R	RESERVED	0	Reserved.

8	R/W	USM_EN	0	When entering pulse-frequency modulation (PFM) with no load, the frequency should be >30kHz, and the dummy load is modulated to discharge the output. This bit can be configured via the OTP. 0: Disabled 1: Enabled
7	R	RESERVED	0	Reserved.
6	R/W	V_{SYS_MIN}[6]	0	Sets the absolute minimum system regulation voltage. It is recommended to set this value according to the battery cell count. These bits are reset when the watchdog resets. These bits can be configured via the OTP. Range: Between V_{BATT_PRE} and V_{BATT_REG} Default: 6.4V (for 2 cells) LSB: 200mV V_{SYS_MIN} = DEC(Bits[6:0]) x 200 (mV)
5	R/W	V_{SYS_MIN}[5]	1	
4	R/W	V_{SYS_MIN}[4]	0	
3	R/W	V_{SYS_MIN}[3]	0	
2	R/W	V_{SYS_MIN}[2]	0	
1	R/W	V_{SYS_MIN}[1]	0	
0	R/W	V_{SYS_MIN}[0]	0	

REG08h

The REG08h register sets the input current limit.

Bits	Access	Bit Name	Default	Description
15:7	R	RESERVED	0	Reserved.
6	R/W	I_{IN_LIM}[6]	0	Sets the input current limit. These bits are reset when the watchdog resets. These bits can be configured via the OTP. Range: Up to 6A (111 1000) Default: 500mA (000 1010) LSB: 50mA I_{IN_LIM} = DEC(Bits[6:0]) x 50 (mA) When R_{S1} changes to 5mΩ, the internal gain should also be changed via REG10h, bit[8] so that the LSB stays unchanged.
5	R/W	I_{IN_LIM}[5]	0	
4	R/W	I_{IN_LIM}[4]	0	
3	R/W	I_{IN_LIM}[3]	1	
2	R/W	I_{IN_LIM}[2]	0	
1	R/W	I_{IN_LIM}[1]	1	
0	R/W	I_{IN_LIM}[0]	0	

REG09h

The REG09h register sets the IN output voltage in source mode (V_{IN_SRC}).

Bits	Access	Bit Name	Default	Description
15:12	R	RESERVED	0	Reserved.
11	R/W	$V_{IN\_SRC\_OS}$	0	When this bit is enabled, then V_{IN_SRC} is DEC(Bits[9:0]) + 0.64V. Keep this bit set to 0 in charge mode. 0: 0V 1: 0.64V
10	R/W	$V_{IN\_SRC\_CFG}$	0	Determines the method to configure V_{IN_SRC} in source mode. 0: Configured by V_{IN_SRC} 1: Configured by the FB pin
9	R/W	V_{IN_SRC}[9]	0	Sets V_{IN_SRC} in source mode. Range: Up to 20.46V (11 1111 1111) Default: 4.98V LSB: 20mV V_{IN_SRC} = DEC(Bits[9:0]) x 20 (mV) When $V_{IN\_SRC\_OS}$ = 1, V_{IN_SRC} is DEC(Bits[9:0]) x 20 (mV) + 0.64V. The maximum V_{IN_SRC} is 21V.
8	R/W	V_{IN_SRC}[8]	0	
7	R/W	V_{IN_SRC}[7]	1	
6	R/W	V_{IN_SRC}[6]	1	
5	R/W	V_{IN_SRC}[5]	1	
4	R/W	V_{IN_SRC}[4]	1	
3	R/W	V_{IN_SRC}[3]	1	
2	R/W	V_{IN_SRC}[2]	0	
1	R/W	V_{IN_SRC}[1]	0	
0	R/W	V_{IN_SRC}[0]	1	

REG0Ah

The REG0Ah register sets the battery impedance compensation, battery-full voltage regulation, and output current limit in source mode.

Bits	Access	Bit Name	Default	Description
15	R	RESERVED	0	Reserved.
14	R	RESERVED	0	Reserved.
13	R/W	BATTR[2]	0	Sets the predicted battery internal impedance and cable impedance. These bits are reset when the watchdog resets. Range: 0mΩ/cell to 350mΩ/cell Default: 50mΩ/cell LSB: 50mΩ BATTR = DEC(Bits[13:11]) x 50 (mΩ/cell)
12	R/W	BATTR[1]	0	
11	R/W	BATTR[0]	0	
10	R/W	V_{CLAMP}[2]	0	Sets the maximum compensation voltage, which should be added to the original battery-full regulation voltage if the IR compensation function is used. These bits are reset when the watchdog resets. Range: 0mV/cell to 420mV/cell Default: 0mV/cell LSB: 60mV V_{CLAMP} = DEC(Bits[10:8]) x 60 (mV/cell)
9	R/W	V_{CLAMP}[1]	0	
8	R/W	V_{CLAMP}[0]	0	
7	R	RESERVED	0	Reserved.
6	R/W	I_{IN_SRC}[6]	0	Sets the I_{IN_SRC} limit in source mode. These bits are reset when the watchdog resets. Range: 0A to 6A Default: 2A LSB: 50mA I_{IN_SRC} = DEC(Bits[6:0]) x 50 (mA) When R_{S1} changes to 5mΩ, the internal gain should also be changed via REG10h, bit[8] so that the LSB stays unchanged.
5	R/W	I_{IN_SRC}[5]	1	
4	R/W	I_{IN_SRC}[4]	0	
3	R/W	I_{IN_SRC}[3]	1	
2	R/W	I_{IN_SRC}[2]	0	
1	R/W	I_{IN_SRC}[1]	0	
0	R/W	I_{IN_SRC}[0]	0	

REG0Bh

The REG0Bh register sets the low battery voltage thresholds and battery discharge current regulation in source mode.

Bits	Access	Bit Name	Default	Description
15:14	R	RESERVED	0	Reserved.
13	R/W	$V_{BATT\_LOW\_EN}$	1	Enables the battery low-voltage protection. It is reset when the watchdog resets. This bit can be configured via the OTP. Default: Enabled 0: Disabled 1: Enabled
12	R/W	V_{BATT_PRE}	1	Sets the pre-charge to CC charge threshold. Default: 3V/cell 0: 2.55V/cell 1: 3V/cell

11	R/W	BATTLOW_ACT	0	Determines the behavior for the battery's low voltage protection when REG0Bh, bit[13] is set to 1. When V_{BATT} < V_{BATT_LOW} (which is set via REG0Bh, bits[10:9]), INT asserts and the DC/DC converter can also be latched off optionally. This bit is reset when the watchdog resets. This bit can be configured via the OTP. Default: 0 0: Generate INT and disable the DC/DC converter 1: Generate INT and latch-off the DC/DC converter After toggling the SRC_EN bit , the source mode can be enabled again. When source mode is disabled, the BATTLOW comparator does not operate.
10	R/W	V_{BATT_LOW}[1]	0	Sets the low battery voltage threshold for battery low-voltage protection. Default: 3V/cell 00: 3V/cell 01: 3.1V/cell 10: 3.2V/cell 11: 3.3V/cell
9	R/W	V_{BATT_LOW}[0]	0	
8	R/W	I_{BATT_DSCHG}EN	0	Enables the battery discharge current regulation in source mode. Default: Disabled 0: Disabled 1: Enabled
7	R/W	I_{BATT_DSCHG}[7]	1	Sets the battery discharge current in source mode. Range: Up to 12.75A Default: 6.4A LSB: 50mA IBATT_DIS_LIM = DEC(Bits[7:0]) x 50 (mA)
6	R/W	I_{BATT_DSCHG}[6]	0	
5	R/W	I_{BATT_DSCHG}[5]	0	
4	R/W	I_{BATT_DSCHG}[4]	0	
3	R/W	I_{BATT_DSCHG}[3]	0	
2	R/W	I_{BATT_DSCHG}[2]	0	
1	R/W	I_{BATT_DSCHG}[1]	0	
0	R/W	I_{BATT_DSCHG}[0]	0	

REG0Ch

The REG0Ch register controls the IC action during JEITA protection.

Bits	Access	Bit Name	Default	Description
15	R	RESERVED	0	Reserved.
14	R/W	WARM_ACT[1]	0	Determines the device's behavior if NTC warm protection occurs. These bits are reset when the watchdog resets. 00: No action 01: Only reduce V_{BATT_REG} 10: Only reduce I_{CC} 11: Reduce both V_{BATT_REG} and I_{CC}
13	R/W	WARM_ACT[0]	1	
12	R/W	COOL_ACT[1]	1	Determines the device's behavior if NTC cool protection occurs. These bits are reset when the watchdog resets. 00: No action 01: Only reduce V_{BATT_REG} 10: Only reduce I_{CC} 11: Reduce both V_{BATT_REG} and I_{CC} when NTC cool
11	R/W	COOL_ACT[0]	0	

10	R/W	JEITA_VSET[4]	1	Sets the decrement value for the battery-full voltage if NTC cool or warm protection occurs. The battery-full voltage can be set via REG15h. These bits are reset when the watchdog resets. Range: Up to 620mV/cell Default: 320mV/cell LSB: 20mV/cell JEITA_VSET = DEC([Bits[10:6]) x 20 (mV/cell)
9	R/W	JEITA_VSET[3]	0	
8	R/W	JEITA_VSET[2]	0	
7	R/W	JEITA_VSET[1]	0	
6	R/W	JEITA_VSET[0]	0	
5	R/W	JEITA_ISET[1]	0	Sets the scaling value of the constant current (CC) charge current. The CC charge current can be set via REG14h. These bits are reset when the watchdog resets. Default: 1/4 times 00: 1/2 times 01: 1/4 times 10: 1/8 times 11: 1/16 times
4	R/W	JEITA_ISET[0]	1	
3:0	R	RESERVED	0	Reserved.

REG0Dh

The REG0Dh register sets the JEITA thresholds and controls temperature protection.

Bits	Access	Bit Name	Default	Description
15	R/W	TS_EN	1	When TS_OPTION is set to 0, this bit enables the external temperature sense function. Default: Enabled 0: Disabled 1: Enabled When bit[14] of this command is set to 1, this bit determines the device's behavior if TS over-temperature protection (OTP) occurs. 0: Only take the BAGE regulation action and do not deliver an INT signal 1: Take the BGATE regulation action and deliver an INT signal
14	R/W	TS_OPTION	1	Determines where the temperature is sensed. This bit is reset when the watchdog resets. This bit can be configured via the OTP. Default: 1 (BATFET) 0: Input connector 1: BATFET
13	R/W	TS_ACT	0	When bit[14] of this command is set to 0, this bit determines the device's behavior if a TS over temperature (OT) fault occurs. INT asserts after TS OT occurs, and an additional I_{IN} regulation can be taken optionally. It is reset when watchdog resets. This bit can be configured via the OTP. Default: 0 0: Only deliver INT when reach TS threshold 1: Deliver INT and take TS action

12	R/W	V_{TS_HOT}[2]	1	Sets the TS OT threshold, which is a percentage of V_{NTC}. Assume that the thermistor is 103AT, and the pull-up resistor is 10kΩ. Default: 14.95% (80°C) 000: 9.68% (100°C) 001: 10.62% (95°C) 010: 11.98% (90°C) 011: 13.29% (85°C) 100: 14.95% (80°C) 101: 16.74% (75°C) 110: 18.74% (70°C) 111: 21.11% (65°C)
11	R/W	V_{TS_HOT}[1]	0	
10	R/W	V_{TS_HOT}[0]	0	
D9	R/W	NTC_EN	1	Enables NTC protection. Default: Enabled 0: Disabled 1: Enabled
8	R/W	NTC_ACT	1	Sets the device's behavior if NTC protection occurs. An INT asserts when NTC protection and addition actions can be taken optionally. This bit can be configured via the OTP. Default: 1 0: Only deliver INT when the NTC threshold is reached 1: Deliver INT and take NTC action
7	R/W	V_{HOT}[1]	1	Sets the NTC hot temperature threshold, which is as a percentage of V_{NTC}. Assume that the thermistor is 103AT. Default: 23.6% (60°C) 00: 29.63% (50°C) 01: 26.46% (55°C) 10: 23.6% (60°C) 11: 21.03% (65°C)
6	R/W	V_{HOT}[0]	0	
5	R/W	V_{WARM}[1]	0	Sets the NTC warm temperature threshold, which is as a percentage of V_{NTC}. Assume that the thermistor is 103AT. Default: 33.2% (45°C) 00: 36.86% (40°C) 01: 33.2% (45°C) 10: 29.61% (50°C) 11: 26.45% (55°C)
4	R/W	V_{WARM}[0]	1	
3	R/W	V_{COOL}[1]	1	Sets the NTC cool temperature threshold, which is as a percentage of V_{NTC}. Assume that the thermistor is 103AT. Default: 65.2% (10°C) 00: 74.68% (0°C) 01: 70.12% (5°C) 10: 65.2% (10°C) 11: 59.9% (15°C)
2	R/W	V_{COOL}[0]	0	
1	R/W	V_{COLD}[1]	0	These bits set the NTC cold temperature threshold, which is as a percentage of V_{NTC}. Assume that the thermistor is 103AT. Default: 74.5% (0°C) 00: 78.82% (-5°C) 01: 74.5% (0°C) 10: 70.12% (5°C) 11: 65.29% (10°C)
0	R/W	V_{COLD}[0]	1	

REG0Eh

The REG0Eh register controls the ADC and switching frequency (f_{SW}).

Bits	Access	Bit Name	Default	Description
15:9	R	RESERVED	0	Reserved.
8	R	RESERVED	0	Reserved.
7	R/W	ADC_CONV	0	When only the battery is present, this bit determines the behavior of ADC conversion. 0: Disable ADC 1: Continuous ADC conversion
6	R/W	SW_FREQ[2]	0	Sets the buck-boost converter's f_{SW}. These bits are reset when the watchdog resets. They can be configured via the OTP. Default: 425kHz 000: 375kHz 001: 425kHz 010: 475kHz 011: 510kHz 100: 550kHz 101: 625kHz 110: 700kHz 111: 770kHz
5	R/W	SW_FREQ[1]	0	
4	R/W	SW_FREQ[0]	1	
3	R	RESERVED	1	Reserved. Do not change this bit value.
2:0	R	RESERVED	0	Reserved. Do not change this bit value.

REG0Fh

The REG0Fh register sets the junction temperature (T_J), trickle charge current, pre-charge current, and termination current.

Bits	Access	Bit Name	Default	Description
15	R/W	T_{J_REG}_EN	1	This bit enables T_J. This bit is reset when watchdog resets. This bit can be configured via the OTP. Default: Enabled 0: Disabled 1: Enabled
14	R/W	T_{J_REG}[2]	1	Sets the T_J regulation point. These bits are reset when the watchdog resets. Default: 120°C 000: 80°C 001: 90°C 010: 95°C 011: 100°C 100: 105°C 101: 110°C 110: 115°C 111: 120°C
13	R/W	T_{J_REG}[1]	1	
12	R/W	T_{J_REG}[0]	1	
11	R/W	I_{TC}[3]	0	Sets the trickle-charge current. These bits are reset when the watchdog resets. These bits can be configured via the OTP. Range: 0 to 750mA Default: 100mA LSB: 50mA I_{TC} = DEC(Bits[11:8]) x 50 (mA)
10	R/W	I_{TC}[2]	0	
9	R/W	I_{TC}[1]	1	
8	R/W	I_{TC}[0]	0	

7	R/W	I_{PRE}[3]	0	Sets the pre-charge current. These bits are reset when the watchdog resets. These bits can be configured via the OTP. Range: Up to 1.5A Default: 400mA LSB: 100mA I_{PRE} = DEC(Bits[7:4]) x 100 (mA)
6	R/W	I_{PRE}[2]	1	
5	R/W	I_{PRE}[1]	0	
4	R/W	I_{PRE}[0]	0	
3	R/W	I_{TERM}[3]	0	Sets the termination current. These bits are reset when the watchdog resets. These bits can be configured via the OTP. Range: Up to 750mA Default: 200mA LSB: 50mA I_{TERM} = DEC(Bits[3:0]) x 50 (mA)
2	R/W	I_{TERM}[2]	1	
1	R/W	I_{TERM}[1]	0	
0	R/W	I_{TERM}[0]	0	

REG10h: Configuration Register 2

The REG10h register provides some control bits and sets the battery cell number and the voltage of V_{TRACK}.

Bits	Access	Bit Name	Default	Description
15	R	RESERVED	0	Reserved
14	R/W	ACGATE_CTRL	0	Controls ACGATE. This bit can force ACGATE to turn on the external MOSFET when it is set to 1. Default: 0 (ACGATE state depends on the ADP voltage) 0: Do not force ACGATE on 1: Force ACGATE on
13	R/W	BGATE_CTRL	0	Controls BGATE. This bit can force BGATE to turn off the external MOSFET when it is set to 1. The BGATE state depends on the BGATE control logic in NVDC mode. Default: 0 (do not force the BGATE off) 0: Do not force the BGATE off 1: Force the BGATE off
12	R/W	TS/IMON	0	Configures the function of the TS/IMON pin. This bit is reset when the watchdog timer resets. This bit can be configured via the OTP. Default: TS function 0: Act as the TS function 1: Act as the IMON function
11	R/W	VRECH	1	This bit sets the automatic recharge threshold, which is below the battery-full voltage. This bit is reset when the watchdog timer resets. This bit can be configured via the OTP. Default: 200mV/cell 0: 100mV/cell 1: 200mV/cell
10	R/W	BAT_NUM[1]	0	Sets the battery cells in series. These bits are reset when the watchdog timer resets. These bits can be configured via the OTP. Default: 2-cell 01: 2-cell 10: 3-cell 11: 4-cell
9	R/W	BAT_NUM[0]	1	

8	R/W	IN_RSNS	0	Sets the I_{IN} sense gain. This bit should be set according to the external sense resistor (R_{S1}). This bit is reset when the watchdog timer resets. This bit can be configured via the OTP. Default: 10mΩ 0: 10mΩ 1: 5mΩ
7	R/W	IBATT_RSNS	0	Sets the battery current-sense gain. This bit should be set according to the external sense resistor (R_{S2}). This bit is reset when the watchdog timer resets. This bit can be configured via the OTP. Default: 10mΩ 0: 10mΩ 1: 5mΩ
6	R/W	ACGATE_EN	1	Enabled the ACGATE driver. Default: Enabled 0: Disable the ACGATE driver (external ACFET is off mandatorily) 1: Enable the ACGATE driver
5	R	RESERVED	1	Reserved. Do not change the values of these bits.
4	R/W	V_{TRACK}[4]	1	Sets the track voltage in NVDC power path management control. The minimum system voltage ($V_{SYS\_MIN\_REG}$) is regulated at V_{SYS_MIN} + (V_{TRACK} x BAT_NUM). BAT_NUM refers to REG10h, bits[10:9]. These bits are reset when the watchdog resets. These bits can be configured via the OTP. Range: Up to 155mV/cell Default: 100mV/cell LSB: 5mV/cell V_{TRACK} = DEC(Bits[4:0]) x 5 (mV/cell)
3	R/W	V_{TRACK}[3]	0	
2	R/W	V_{TRACK}[2]	1	
1	R/W	V_{TRACK}[1]	0	
0	R/W	V_{TRACK}[0]	0	

REG11h: Configuration Register 3

The REG11h register sets the system voltage protection and input voltage protection in charge mode, and controls battery over-voltage protection (OVP).

Bits	Access	Bit Name	Default	Description
15	R	RESERVED	0	Reserved.
14	R/W	V_{SYS_OV}[1]	1	Sets the system (SYS) over-voltage (OV) threshold (as a percentage of the system regulation voltage). This value is also used as the output OV threshold in source mode. Default: 110% 00: 106% 01: 120% 10: 115% 11: 110%
13	R/W	V_{SYS_OV}[0]	1	
12	R/W	V_{SYS_UV}[1]	0	Sets the system under-voltage (UV) threshold, which is as percentage of the system regulation voltage. This is also reused for the output UV threshold in source mode. Default: 75% 00: 75% 01: 80% 10: 85% 11: 30%
11	R/W	V_{SYS_UV}[0]	0	

10	R/W	t_{INOVP_DGL}	0	Sets the deglitch time for input OVP in charging mode. Default: 1μs 0: 1μs 1: 15ms
9	R/W	V_{IN_UVP}[1]	0	Sets the input under-voltage protection (UVP) threshold. These bits are reset when the watchdog timer resets. These bits can be configured via the OTP. Default: 3.2V 00: 3.2V 01: 6.4V 10: 12V 11: 16.8V
8	R/W	V_{IN_UVP}[0]	0	
7	R/W	V_{IN_OVP}[1]	1	Sets the input OVP threshold. These bits are reset when the watchdog timer resets. These bits can be configured via the OTP. Default: 22.45V 00: 7.25V 01: 11.25V 10: 17.65V 11: 22.45V
6	R/W	V_{IN_OVP}[0]	1	
5	R/W	SYSOVP_EN	1	Enables system OVP. Default: Enabled 0: Disabled 1: Enabled
4	R/W	SYS_DUMMY	0	Enables the SYS dummy load. Default: Disabled 0: Disabled 1: Enabled
3	R/W	BATTOVP_EN	1	Enables battery OVP. Default: Enabled 0: Disabled 1: Enabled
2	R/W	BATT_DUMMY	0	Enables BATT dummy load. Default: Disabled 0: Disabled 1: Enabled
1	R	RESERVED	0	Reserved. Do not change this bit value.
0	R	RESERVED	0	Reserved. Do not change this bit value.

REG12h: Configuration Register 4

The REG12h register controls the charge timer, watchdog timer, and on/off control for charge and source mode operation.

Bits	Access	Bit Name	Default	Description
15	R	RESERVED	0	Reserved. Do not change this bit value.
14	R	RESERVED	0	Reserved. Do not change this bit value.

13	R/W	TMR_EN	1	Enables the charging safety timer (both the linear charger timer and switching charge timer). This bit is reset when the watchdog resets. This bit can be configured via the OTP. Default: Enabled 0: Disabled 1: Enabled
12	R/W	CHG_TMR[1]	1	Sets the CC/CV timer. These bits are reset when the watchdog resets. Default: 20 hours 00: 5 hours 01: 8 hours 10: 12 hours 11: 20 hours
11	R/W	CHG_TMR[0]	1	
10	R/W	TMR2X_EN	1	Controls the charge timer speed duing input voltage, input current, or thermal regulation. This bit is reset when the watchdog resets. Default: 1 0: Timer counts at normal clock rate 1: Timer counts at half-clock rate
9	R/W	WTD_RST	0	Resets the I^2C watchdog timer. This bit returns to 0 after it is reset. It is reset when watchdog resets. Default: 0 0: Normal 1: Reset
8	R/W	WTD[1]	0	Sets the I^2C watchdog timer. These bits are reset when the watchdog resets. These bits can be configured via the OTP. Default: Disabled 00: Disable timer 01: 40s 10: 80s 11: 175s
7	R/W	WTD[0]	0	
6	R/W	DC/DC_EN	1	Enables the DC/DC converter. This bit is reset when the watchdog resets. This bit can be configured via the OTP. Default: Enabled 0: Disabled 1: Enabled
5	R/W	BGATE_EN	1	Enables the BGATE driver. When disabled, the BGATE output stays in a Hi-Z state. This bit is reset when the watchdog resets. This bit can be configured via the OTP. Default: Enabled 0: Disabled 1: Enabled
4	R/W	TERM_EN	1	Enables charge termination. This bit is reset when the watchdog resets. This bit can be configured via the OTP. Default: Enabled 0: Disabled 1: Enabled

3	R/W	SRC_EN	0	Enables source mode configuration. SRC_EN can override the charge enable function. This bit is reset when the watchdog resets. Default: Disabled 0: Disable source mode 1: Enable source mode
2	R/W	REG_RST	0	Resets the register. This bit resets to 0 after the register is reset. This bit is reset when the watchdog resets. Default: 0 0: Keep the current register setting 1: Reset to the default register value and reset safety timer
1	R/W	IINLIM_EN	1	Enables the I_{IN} limit loop. This bit is reset when the watchdog resets. Default: Enabled 0: IIN_LIM disabled 1: IIN_LIM enabled
0	R/W	CHG_EN	1	Configures the charge mode. SRC_EN overrides the CHG_EN enable function. This bit is reset when the watchdog resets. This bit can be configured via the OTP. Default: Charge enabled 0: Charge disabled 1: Charge enabled

REG14h

The REG14h register sets the battery constant fast charge current.

Bits	Access	Bit Name	Default	Description
15:14	R	RESERVED	0	Reserved.
13	R/W	I_{CC}[7]	0	Sets the charge current. These bits are reset when the watchdog resets. These bits can be configured via the OTP. Range: 0A to 6A Default: 2A LSB: 50mA I_{CC} = DEC(Bits[13:6]) x 50 (mA)
12	R/W	I_{CC}[6]	0	
11	R/W	I_{CC}[5]	1	
10	R/W	I_{CC}[4]	0	
9	R/W	I_{CC}[3]	1	
8	R/W	I_{CC}[2]	0	
7	R/W	I_{CC}[1]	0	
6	R/W	I_{CC}[0]	0	
5:0	R	RESERVED	0	Reserved.

REG15h

The REG15h register sets the battery-full regulation voltage.

Bits	Access	Bit Name	Default	Description
15	R	RESERVED	0	Reserved.

14	R/W	V_{BATT_REG}[10]	0	Sets the battery-full voltage. These bits are reset when the watchdog resets. These bits can be configured via the OTP. V_{BATT_REG} (REG15h, bits[14:4]) is the battery-full voltage when the cell voltage range is between 3.4V/cell and 4.67V/cell. Battery-Full Voltage = DEC(Bits[14:4]) x 10 (mV) For example: for a 4-cell battery pack with 4.2V/cell, V_{BATT_REG} = 16.8V, and the battery-full voltage is 16.8V.
13	R/W	V_{BATT_REG}[9]	1	
12	R/W	V_{BATT_REG}[8]	1	
11	R/W	V_{BATT_REG}[7]	0	
10	R/W	V_{BATT_REG}[6]	1	
9	R/W	V_{BATT_REG}[5]	0	
8	R/W	V_{BATT_REG}[4]	0	
7	R/W	V_{BATT_REG}[3]	1	
6	R/W	V_{BATT_REG}[2]	0	
5	R/W	V_{BATT_REG}[1]	0	
4	R/W	V_{BATT_REG}[0]	0	
3:0	R	RESERVED	0	Reserved.

REG16h

The REG16h register indicates the charge status and faults related to BATFET OC and OT conditions.

Bits	Access	Bit Name	Default	Description
15	R	MD_STAT[1]	0	Indicates the DC/DC operation status. INT asserts when the state changes. 00/10: Idle 01/11: Operation
14	R	MD_STAT[0]	0	
13	R	PG_STAT	0	Indicates the power good (PG) status. INT asserts when this bit changes from 0 to 1. 0: V_{IN} not power good 1: V_{IN} power good
12	R	SWITCH_STAT[1]	0	Indicates the DC/DC converter's operation mode. 00: Idle 01: Buck 10: Buck-boost 11: Boost
11	R	SWITCH_STAT[0]	0	
10	R	BATT_MISS_STAT	0	Indicates whether the battery is missing when set to 1. INT asserts when this bit changes from 0 to 1. 0: Normal 1: Battery missing
9	R	RESERVED	0	Reserved.
8	R	CHG_STAT[2]	0	Indicates the charging status. INT asserts when the state changes. 000: No charging 001: Trickle charge 010: Pre-charge 011: CC charge 100: CV charge 101: Charge termination
7	R	CHG_STAT[1]	0	
6	R	CHG_STAT[0]	0	
5	R	VIN_MIN_STAT	0	Indicates whether the IC stays in the V_{IN} loop. INT asserts when the bit changes from 0 to 1. 0: The IC is not in the input voltage limit 1: The IC is in the input voltage limit
4	R	IIN_LIM_STAT	0	Indicates whether the IC stays in the I_{IN} loop. INT asserts when the bit changes from 0 to 1. 0: The IC is not in the input current limit 1: The IC is in the input current limit
3	R	RESERVED	0	Reserved.

2	R	BATFET_OC	0	Indicates whether the discharge current threshold exceeds the current threshold. The device asserts an INT signal if a BATFET over-current (OC) condition occurs. Default: 0 (Normal) 0: Normal operation 1: A BATFET OC condition has occurred
1	R	TS_FAULT	0	Indicates whether a TS over-temperature (OT) fault occurs. INT asserts when a TS OT fault occurs. 0: Normal 1: TS OT
0	R	RESERVED	0	Reserved.

REG17h:

The REG17h register indicates the faults in charge and source mode.

Bits	Access	Bit Name	Default	Description
15	R	VIN_SRC_OV	0	Indicates whether output over-voltage protection (OVP) has occurred in source mode. INT asserts when output OVP occurs. 0: Normal 1: OVP at VIN in source mode.
14	R	VIN_SRC_UV	0	Indicates whether output under-voltage protection (UVP) occurs in source mode. INT asserts when the output UVP occurs. 0: Normal 1: UVP has occurred at VIN in source mode
13	R	VIN_OV	0	Indicates whether input OVP occurs in charging mode. INT asserts when input OVP occurs. 0: Normal 1: Input OVP has occurred in charge mode
12	R	VADP_OV	0	Indicates whether ADP OVP occurs in charging mode. INT asserts when VADP OVP occurs. 0: Normal 1: VADP OVP has occurred
11	R	VSYS_OV	0	Indicates whether system (SYS) OVP occurs in charging mode. INT asserts when SYS OVP occurs. 0: Normal operation 1: System OVP has occurred
10	R	VSYS_UV	0	Indicates whether system UVP occurs in charging mode. INT asserts when the SYS UV occurs. 0: Normal operation 1: System UVP has occurred
9	R	RESERVED	0	Reserved.
8	R	VBATT_OV	0	Indicates whether battery OVP occurs in charging mode. INT asserts when battery OVP occurs. 0: Normal 1: Battery OVP has occurred
7	R	VBATT_LOW	0	Indicates whether there is a low battery voltage in source mode. INT asserts when BATT_LOW occurs. 0: Normal 1: Discharge stop due to BATT_LOW

<table>
<tr><td>6</td><td>R</td><td>WTD_EXP</td><td>0</td><td>Indicates whether the watchdog timer has expired.

0: Normal
1: Watchdog timer expiration has occurred</td></tr>
<tr><td>5</td><td>R</td><td>CHG_TMR_EXP</td><td>0</td><td>Indicates whether the charge safety timer has expired. INT asserts when the timer expires.

0: Normal
1: Charge safety timer expiration has occurred</td></tr>
<tr><td>4</td><td>R</td><td>THERM_SHDN</td><td>0</td><td>Indicates whether thermal shutdown occurs. INT asserts when thermal shutdown occurs.

0: Normal
1: Thermal shutdown</td></tr>
<tr><td>3</td><td>R</td><td>RESERVED</td><td>0</td><td>Reserved.</td></tr>
<tr><td>2</td><td>R</td><td>NTC_FAULT[2]</td><td>0</td><td rowspan="3">Indicates whether an NTC faults has occurred in charge mode or source mode. INT asserts when any fault occurs.

<table><tr><th colspan="2">Charge Mode</th><th colspan="2">Source Mode</th></tr><tr><td>000</td><td>Normal</td><td>000</td><td>Normal</td></tr><tr><td>001</td><td>NTC Cold</td><td>001</td><td>NTC Cold</td></tr><tr><td>010</td><td>NTC Cool</td><td>100</td><td>NTC Hot</td></tr><tr><td>011</td><td>NTC Warm</td><td>111</td><td>NTC Float</td></tr><tr><td>100</td><td>NTC Hot</td><td>-</td><td>-</td></tr><tr><td>111</td><td>NTC Float</td><td>-</td><td>-</td></tr></table></td></tr>
<tr><td>1</td><td>R</td><td>NTC_FAULT[1]</td><td>0</td></tr>
<tr><td>0</td><td>R</td><td>NTC_FAULT[0]</td><td>0</td></tr>
</table>

REG18h

The REG18h register sets INT mask control.

Bits	Access	Bit Name	Default	Description
15	R	RESERVED	0	Reserved.
14	R/W	VSYS_FAULT	0	For any fault that is masked, INT does not assert if that fault occurs. However, the fault bit is still set. These bits are reset when the watchdog timer resets. 0: Masked 1: Not masked
13	R/W	VIN_SRC_FAULT	0	
12	R/W	VIN_OV_FAULT	0	
11	R/W	PG_STAT	0	
10	R/W	BATT_OV_FAULT	0	
9	R/W	BATFET_OC	0	
8	R	RESERVED	0	Reserved.
7	N/A	BATT_LOW_FAULT	0	For any fault that is masked, INT does not assert if that fault occurs. However, the fault bit is still set. These bits are reset when the watchdog timer resets. 0: Masked 1: Not masked
6	R/W	BATT_MISS_STAT	0	
5	R/W	THERM_SHDN	0	
4	R/W	TS_FAULT	0	
3	R/W	NTC_FAULT	0	
2	R/W	CHG_TMR_FAULT	0	
1	R/W	MD_STAT	0	
0	R/W	CHG_STAT	0	

REG19h

The REG19h register sets INT mask control for the input power path.

Bits	Access	Bit Name	Default	Description
15:2	R	RESERVED	0	Reserved.
1	R/W	VIN_MIN_STAT	0	For any fault that is masked, INT does not assert if that fault occurs. However, the fault bit is still set. These bits are reset when the watchdog timer resets. 0: Masked 1: Not masked
0	R/W	IIN_LIM_STAT	0	

REG23h

The REG23h register indicates the ADC result for the input voltage.

Bits	Access	Bit Name	Default	Description
15:10	R	RESERVED	-	Reserved.
9	R	V_{IN_ADC}[9]	-	Indicates the ADC V_{IN} conversion. LSB: 20mV V_{IN_ADC} = DEC(Bits[9:0]) x 20 (mV)
8	R	V_{IN_ADC}[8]	-	
7	R	V_{IN_ADC}[7]	-	
6	R	V_{IN_ADC}[6]	-	
5	R	V_{IN_ADC}[5]	-	
4	R	V_{IN_ADC}[4]	-	
3	R	V_{IN_ADC}[3]	-	
2	R	V_{IN_ADC}[2]	-	
1	R	V_{IN_ADC}[1]	-	
0	R	V_{IN_ADC}[0]	-	

REG24h

The REG24h register indicates the ADC result for the input current.

Bits	Access	Bit Name	Default	Description
15:10	R	RESERVED	-	Reserved.
9	R	I_{IN_ADC}[9]	-	Indicates the ADC I_{IN} conversion. LSB: 6.25mA I_{IN_ADC} = DEC(Bits[9:0]) x 6.25 (mA)
8	R	I_{IN_ADC}[8]	-	
7	R	I_{IN_ADC}[7]	-	
6	R	I_{IN_ADC}[6]	-	
5	R	I_{IN_ADC}[5]	-	
4	R	I_{IN_ADC}[4]	-	
3	R	I_{IN_ADC}[3]	-	
2	R	I_{IN_ADC}[2]	-	
1	R	I_{IN_ADC}[1]	-	
0	R	I_{IN_ADC}[0]	-	

REG25h

The REG25h register indicates the ADC result for the battery voltage per cell.

Bits	Access	Bit Name	Default	Description
15:10	R	RESERVED	-	Reserved.
9	R	V_{BATT_ADC}[9]	-	Indicates the ADC conversion of the battery voltage per Cell. The real battery voltage should be the value read times cell numbers. LSB: 5mV/cell V_{BATT_ADC} = DEC(Bits[9:0]) x 5 (mV/cell)
8	R	V_{BATT_ADC}[8]	-	
7	R	V_{BATT_ADC}[7]	-	
6	R	V_{BATT_ADC}[6]	-	
5	R	V_{BATT_ADC}[5]	-	
4	R	V_{BATT_ADC}[4]	-	
3	R	V_{BATT_ADC}[3]	-	
2	R	V_{BATT_ADC}[2]	-	
1	R	V_{BATT_ADC}[1]	-	
0	R	V_{BATT_ADC}[0]	-	

REG26h

The REG26h register indicates the ADC result for the system voltage.

Bits	Access	Bit Name	Default	Description
15:10	R	RESERVED	-	Reserved.

9	R	V_{SYS_ADC}[9]	-	Indicates the result of the ADC conversion for the system voltage. LSB: 20mV V_{SYS_ADC} = DEC(Bits[9:0]) x 20 (mV)
8	R	V_{SYS_ADC}[8]	-	
7	R	V_{SYS_ADC}[7]	-	
6	R	V_{SYS_ADC}[6]	-	
5	R	V_{SYS_ADC}[5]	-	
4	R	V_{SYS_ADC}[4]	-	
3	R	V_{SYS_ADC}[3]	-	
2	R	V_{SYS_ADC}[2]	-	
1	R	V_{SYS_ADC}[1]	-	
0	R	V_{SYS_ADC}[0]	-	

REG27h

The REG27h register indicates the ADC result for the battery charge current.

Bits	Access	Bit Name	Default	Description
15:10	R	RESERVED	-	Reserved.
9	R	I_{BATT_ADC}[9]	-	Indicates the result of the ADC conversion for the charge current when an external 10mΩ current-sense resistor is connected. LSB: 12.5mA I_{BATT_ADC} = DEC(Bits[9:0]) x 12.5 (mA)
8	R	I_{BATT_ADC}[8]	-	
7	R	I_{BATT_ADC}[7]	-	
6	R	I_{BATT_ADC}[6]	-	
5	R	I_{BATT_ADC}[5]	-	
4	R	I_{BATT_ADC}[4]	-	
3	R	I_{BATT_ADC}[3]	-	
2	R	I_{BATT_ADC}[2]	-	
1	R	I_{BATT_ADC}[1]	-	
0	R	I_{BATT_ADC}[0]	-	

REG28h

The REG28h register indicates the ADC result for the NTC sense ratio.

Bits	Access	Bit Name	Default	Description
15:10	R	RESERVED	-	Reserved.
9	R	NTC_{ADC}[9]	-	Indicates the ADC conversion of the NTC voltage, as a percentage of V_{NTC}. The real battery temperature can be recalculated according to external divider and thermistor datasheet. LSB: 1/1024 NTC_{ADC} = DEC(Bits[9:0]) x 1/1024 x 100%
8	R	NTC_{ADC}[8]	-	
7	R	NTC_{ADC}[7]	-	
6	R	NTC_{ADC}[6]	-	
5	R	NTC_{ADC}[5]	-	
4	R	NTC_{ADC}[4]	-	
3	R	NTC_{ADC}[3]	-	
2	R	NTC_{ADC}[2]	-	
1	R	NTC_{ADC}[1]	-	
0	R	NTC_{ADC}[0]	-	

REG29h

The REG29h register indicates the ADC result for the TS Sense Ratio.

Bits	Access	Bit Name	Default	Description
15:8	R	RESERVED	-	Reserved.
9	R	TS_{ADC}[9]	-	Indicates the ADC conversion of the TS voltage, as a percentage of V_{NTC}. LSB: 1/1024 TS_{ADC} = DEC(Bits[9:0]) x 1/1024 x 100%
8	R	TS_{ADC}[8]	-	
7	R	TS_{ADC}[7]	-	
6	R	TS_{ADC}[6]	-	
5	R	TS_{ADC}[5]	-	
4	R	TS_{ADC}[4]	-	
3	R	TS_{ADC}[3]	-	
2	R	TS_{ADC}[2]	-	
1	R	TS_{ADC}[1]	-	
0	R	TS_{ADC}[0]	-	

REG2Ah

The REG2Ah register indicates the ADC result for the junction temperature.

Bits	Access	Bit Name	Default	Description
15:10	R	RESERVED	-	Reserved.
9	R	TJ_{ADC}[9]	-	Indicates the ADC conversion for the junction temperature. LSB: 1 T_{J_ADC} = 314 - 0.5703 x DEC(Bits[9:0])
8	R	TJ_{ADC}[8]	-	
7	R	TJ_{ADC}[7]	-	
6	R	TJ_{ADC}[6]	-	
5	R	TJ_{ADC}[5]	-	
4	R	TJ_{ADC}[4]	-	
3	R	TJ_{ADC}[3]	-	
2	R	TJ_{ADC}[2]	-	
1	R	TJ_{ADC}[1]	-	
0	R	TJ_{ADC}[0]	-	

REG2Bh

The REG2Bh register indicates the ADC result for the battery discharge current.

Bits	Access	Bit Name	Default	Description
15:8	R	RESERVED	-	Reserved.
9	R	$I_{BATT\_DIS\_ADC}$[9]	-	Indicates the ADC conversion for the battery discharge charge current. LSB: 12.5mA Offset: 900mA $I_{BATT\_DIS\_ADC}$ = DEC(Bits[9:0]) x 12.5 (mA) - 900mA
8	R	$I_{BATT\_DIS\_ADC}$[8]	-	
7	R	$I_{BATT\_DIS\_ADC}$[7]	-	
6	R	$I_{BATT\_DIS\_ADC}$[6]	-	
5	R	$I_{BATT\_DIS\_ADC}$[5]	-	
4	R	$I_{BATT\_DIS\_ADC}$[4]	-	
3	R	$I_{BATT\_DIS\_ADC}$[3]	-	
2	R	$I_{BATT\_DIS\_ADC}$[2]	-	
1	R	$I_{BATT\_DIS\_ADC}$[1]	-	
0	R	$I_{BATT\_DIS\_ADC}$[0]	-	

REG2Ch

The REG2Ch register indicates the ADC result for the input voltage in source mode.

Bits	Access	Bit Name	Default	Description
15:10	R	RESERVED	-	Reserved.
9	R	$V_{IN\_SRC\_ADC}$[9]	-	These bits indicate the ADC V_{IN_SRC} conversion at the IN pin in source mode. LSB: 20mV $V_{IN\_SRC\_ADC}$ = DEC(bits[9:0]) x 20 (mV)
8	R	$V_{IN\_SRC\_ADC}$[8]	-	
7	R	$V_{IN\_SRC\_ADC}$[7]	-	
6	R	$V_{IN\_SRC\_ADC}$[6]	-	
5	R	$V_{IN\_SRC\_ADC}$[5]	-	
4	R	$V_{IN\_SRC\_ADC}$[4]	-	
3	R	$V_{IN\_SRC\_ADC}$[3]	-	
2	R	$V_{IN\_SRC\_ADC}$[2]	-	
1	R	$V_{IN\_SRC\_ADC}$[1]	-	
0	R	$V_{IN\_SRC\_ADC}$[0]	-	

REG2Dh

The REG2Dh register indicates the ADC result for the output current in source mode.

Bits	Access	Bit Name	Default	Description
15:8	R	RESERVED	-	Reserved.

9	R	$I_{IN\_SRC\_ADC}$[9]	-	These bits indicate the ADC I_{IN_SRC} conversion in source mode. LSB: 6.25mA $I_{IN\_SRC\_ADC}$ = DEC(Bits[9:0]) x 6.25 (mA)
8	R	$I_{IN\_SRC\_ADC}$[8]	-	
7	R	$I_{IN\_SRC\_ADC}$[7]	-	
6	R	$I_{IN\_SRC\_ADC}$[6]	-	
5	R	$I_{IN\_SRC\_ADC}$[5]	-	
4	R	$I_{IN\_SRC\_ADC}$[4]	-	
3	R	$I_{IN\_SRC\_ADC}$[3]	-	
2	R	$I_{IN\_SRC\_ADC}$[2]	-	
1	R	$I_{IN\_SRC\_ADC}$[1]	-	
0	R	$I_{IN\_SRC\_ADC}$[0]	-	

APPLICATION INFORMATION

Selecting the Input Capacitor

The input capacitor absorbs the maximum ripple current from the PWM converter. I_{IN} is discontinuous in buck mode. The input capacitor's RMS ripple current (I_{CIN_RMS}) can be calculated with Equation (3):

$$I_{CIN\_RMS} = I_{CHG} x \frac{\sqrt{V_{BATT} x (V_{IN} - V_{BATT})}}{V_{IN}} \quad (3)$$

The worst-case RMS ripple current occurs at a 50% duty cycle. Typically, V_{BATT} is between 10V and 15V for a 4-cell battery configuration, which means the worst-case condition occurs when the V_{IN} is 20V.

Low-ESR ceramic capacitors with X7R or X5R dielectrics are recommended to be the input decoupling capacitor. These capacitors should be placed as close as possible to the IN and PGND pins, and their voltage rating must exceed the normal V_{IN} level. A capacitor with a minimum 35V voltage is recommended for applications up to a 20V V_{IN}. It is recommended to use 10µF x 5pcs capacitors for up to a 3A I_{IN} limit.

Ceramic capacitors show a DC-bias effect that reduces the capacitor's effective capacitances. The effect may lead to a significant capacitance drop, especially at higher input voltages with small capacitor packages. Choose a higher voltage rating or nominal capacitance value to obtain the required value at the relevant operation point.

Selecting the VCC Decoupling Capacitor

VCC is an internal LDO output. Place an external 4.7µF decoupling capacitor between VCC and AGND, and place it as close to these pins as possible.

Selecting the Inductor

The MP2761 can operate in buck mode or boost mode, which means that the inductor current is equal to either the charging current (I_{CHG}) or I_{IN}. The inductor's saturation current should exceed the larger value between I_{IN} and I_{CHG}, plus half the ripple current. The inductor current ripples for buck mode and boost mode can be estimated with Equation (4) and Equation (5), respectively:

$$I_{RIPPLE\_BUCK} = \frac{V_{SYS} x (V_{IN} - V_{SYS})}{V_{IN} x f_{SW} x L} \quad (4)$$

$$I_{RIPPLE\_BOOST} = \frac{V_{IN} x (V_{SYS} - V_{IN})}{V_{SYS} x f_{SW} x L} \quad (5)$$

The inductor's ripple current (I_{RIPPLE}) depends on the input voltage (V_{IN}), the output system voltage (V_{SYS}), the switching frequency (f_{SW}), and the inductance (L).

The inductance in buck mode can be calculated with Equation (6):

$$L = \frac{V_{SYS} x (V_{IN} - V_{SYS})}{I_{RIPPLE\_BUCK} x V_{IN} x f_{SW}} \quad (6)$$

The required inductance in boost mode can be estimated with Equation (7):

$$L = \frac{V_{IN} x (V_{SYS} - V_{IN})}{V_{SYS} x f_{SW} x I_{RIPPLE\_BOOST}} \quad (7)$$

The MP2761 has a configurable switching frequency from 375kHz to 770kHz. Higher switching frequencies mean that smaller-value inductors can be used. The inductor's saturation current should exceed I_{CHG} plus half of the ripple current.

The maximum input ripple current occurs when the duty cycle is 50% (D = 0.5).

For example, the battery charging voltage ranges from 12V to 16V for a 4-cell battery pack. For a 20V adapter voltage, a 12V V_{BATT} gives the maximum inductor ripple current.

Another example is a 3-cell battery with a V_{BATT} range between 9V and 13.2V. For a 20V adapter voltage, a 10V V_{BATT} gives the maximum inductor ripple current.

Generally, the inductor ripple is designed to be between 20% and 40% of the maximum charging current. For practical designs, there is a tradeoff between inductor size and efficiency.

The recommend inductance is 4.7µH for 2 to 4 cells in series.

Selecting the Output Capacitor

The output system capacitor (C_{SYS}) should have a sufficient ripple current rating to absorb the output AC current.

In boost mode, I_{OUT} is discontinuous and dominates the output capacitor's RMS ripple current (I_{CSYS_BOOST}) can be calculated with Equation (8):

$$I_{CSYS\_BOOST} = I_{SYS} x \frac{\sqrt{V_{IN} \times (V_{SYS} - V_{IN})}}{V_{IN}} \quad (8)$$

The worst-case output RMS ripple current occurs at the lowest VBUS input voltage. The V_{SYS} is approximately 8V for the 2-cell battery packs, so the worst-case scenario occurs when the voltage is 5V in source mode. Low-ESR ceramic capacitors with X7R or X5R dielectrics are recommended for the output decoupling capacitor. This capacitor should be placed as close as possible to the IC's SYS and PGND pins.

The capacitor's voltage rating must exceed the normal V_{BATT} level. A capacitor with a minimum 35V voltage rating is recommended for the 4-cell battery configuration.

Current Sense

The MP2761 has current loops to limit the current and improve the current accuracy and loop stability. An external current-sense resistor is required to sense the average current. Figure 18 shows a recommended connection.

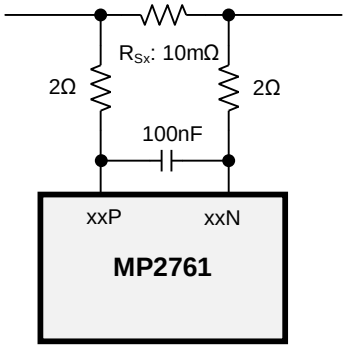


Figure 18: Input or Output Current-Sense Circuit

These current loops are described below:

1. The I_{IN} loop limits the current drawn from the USB port or adapter, and I_{IN} is sensed through the IAP and IAN pins.
2. The battery current loop limits the charge current and discharge current. The battery current is sensed through the SRP and SRN pins.

Selecting the Voltage Divider for NTC Thermistor Temperature

In real-word applications, an external NTC thermistor is placed close to the battery to sense the battery's temperature. The MP2761 measures the battery temperature by monitoring the voltage ratio between the NTC and VNTC pins (see Figure 10 on page 27). Every temperature corresponds to a voltage ratio. The MP2761 has four temperature thresholds to satisfy JEITA requirements.

For a given NTC thermistor, the NTC hot and cold temperature points can be calculated with Equation (9) and Equation (10), respectively:

$$\frac{R_{T2} + R_{NTC\_HOT}}{R_{T1} + R_{T2} + R_{NTC\_HOT}} = \frac{V_{HOT}}{V_{VNTC}} \quad (9)$$

$$\frac{R_{T2} + R_{NTC\_COLD}}{R_{T1} + R_{T2} + R_{NTC\_COLD}} = \frac{V_{COLD}}{V_{VNTC}} \quad (10)$$

Where R_{NTC_HOT} is the thermistor value at the expected hot temperature protection point, and R_{NTC_COLD} is the thermistor value at the expected cold temperature protection point.

By default, V_{HOT} / V_{VNTC}, V_{WARM} / V_{VNTC}, V_{COOL} / V_{VNTC} and V_{COLD} / V_{VNTC} are 23.6%, 33.2%, 65.2% and 74.5%, respectively.

Consider a 103AT NTC thermistor on the battery pack, where the thermistor parameters are $R_{25°C}$ = 10kΩ, β_factor = 3435K. If R_{T1} = 9.845kΩ and R_{T2} = 60Ω, the expected temperature thresholds (T_{HOT} = 60°C, T_{WARM} = 45°C, T_{COOL} = 10°C, and T_{COLD} = 0°C) can be determined.

For simplification, a 10kΩ R_{T1} can be used, and R_{T2} can be replaced with a wire.

Design Example

Table 6 shows a design example following the application guidelines for the specifications below.

Table 6: Design Example

V_{IN}	5V to 20V
V_{BATT_REG}	16.8V
f_{SW}	425kHz
I_{CC}	2A
V_{IN_SRC}	5V to 20V

Figure 20 on page 55 and Figure 21 on page 56 show the detailed application schematics. The typical performance and circuit waveforms are shown in the Typical Performance Characteristics section starting on page 16. For more device applications, refer to the related evaluation board datasheet.

PCB Layout Guidelines

Efficient PCB layout is critical for specified noise, efficiency, and stability requirements. A 4-layer PCB is recommended. For the best results, refer to Figure 19 and follow the guidelines below:

1. Place the output capacitors as close to SYS and PGND as possible. Place a small-sized, 1µF (e.g. 0603) capacitor closer to the SYS and PGND pins than the other 22µF capacitors.
2. Place the input capacitors as close to IN and PGND as possible. Place a small-sized, 1µF (e.g. 0603) capacitor closer to the IN and PGND pins than the other 10µF capacitors.
3. Tie the ground connections (PGND) for the input and output capacitors to the IC ground with a short copper trace connection or PGND plane.
4. Route the connection between SYS/IN and its small-sized 1µF capacitor on the same layer with the IC. The connection to PGND must be on the same layer as the IC. Keep this routing loop as small as possible.
5. Connect AGND to PGND to each decoupling capacitor via a single-point connection.
6. Place the VCC decoupling capacitor and the bootstrap capacitors next to the IC, and keep the trace connections as short as possible.
7. Use a Kelvin connection for the current-sense resistor.
8. Route current-sense wires (IAP and IAN, SRP and SRN) away from switching nodes such as SW1 and SW2.

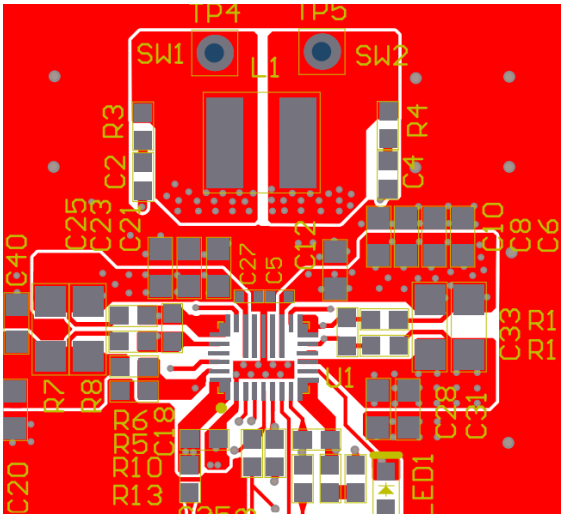


Figure 19: Recommended PCB Layout

TYPICAL APPLICATION CIRCUITS

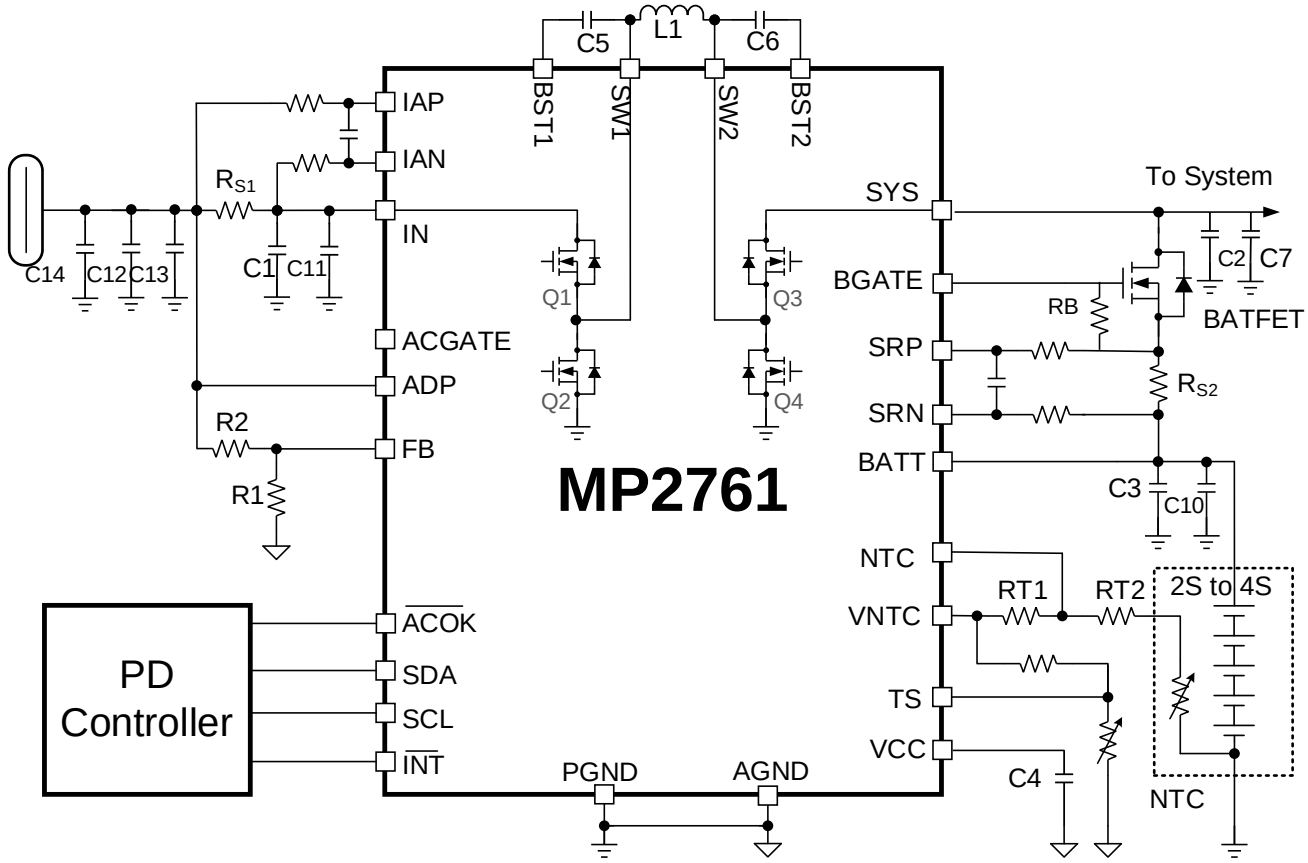


Figure 20: Typical Application Circuit

Table 7: Key BOM for Figure 20

Qty	Ref	Value	Description	Package	Manufacturer
5	C1, C11, C12, C13, C14	10µF	Ceramic capacitor, 35V, X5R	0805	Any
4	C2, C3, C7, C10	22µF	Ceramic capacitor, 35V, X5R	0805	Any
1	C4	4.7µF	Ceramic capacitor, 10V, X5R or X7R	0603	Any
2	C5, C6	100nF	Ceramic capacitor, 25V, X5R or X7R	0603	Any
1	L1	4.7µH	Inductor, 4.7µH, low DCR, I_{SAT} >7.5A	SMD	Any
2	RS1, RS2	10mΩ	Film resistor, 1%	2512	Any
2	RA, RB	5MΩ	Film resistor, 5%	0603	Any
1	BATFET	30V, 5.1mΩ, 20A	N-channel MOSFET (SISA14DN-T1-GE3)	Power PAK 1212-8	Vishay

TYPICAL APPLICATION CIRCUITS *(continued)*

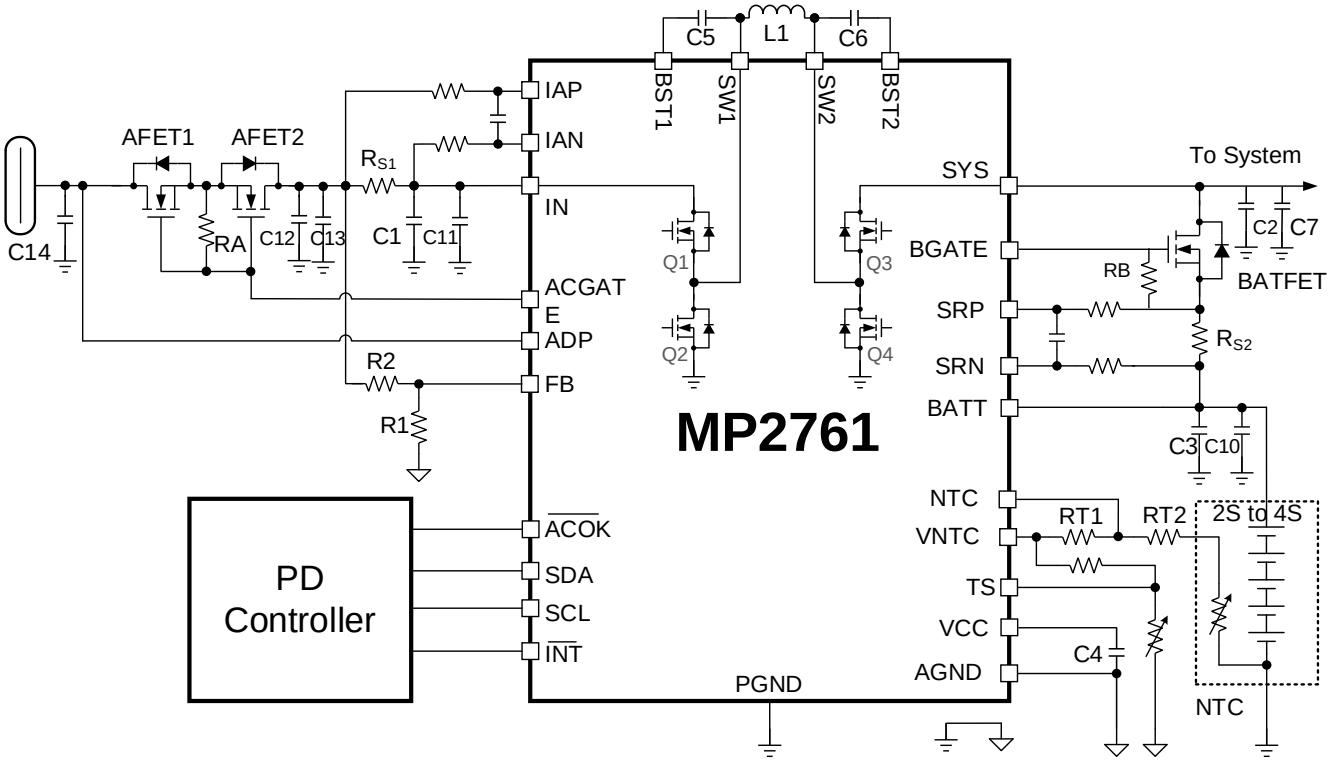


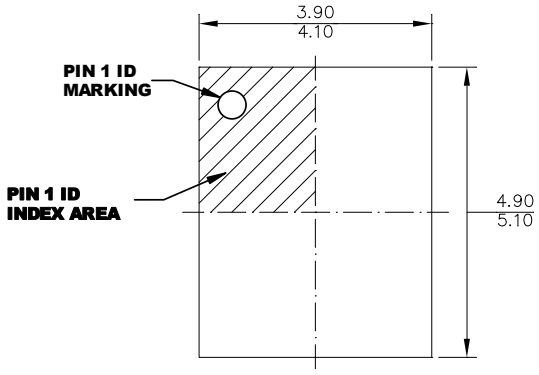
Figure 21: Typical Application Circuit with Input Disconnect Control

Table 8: Key BOM for Figure 21

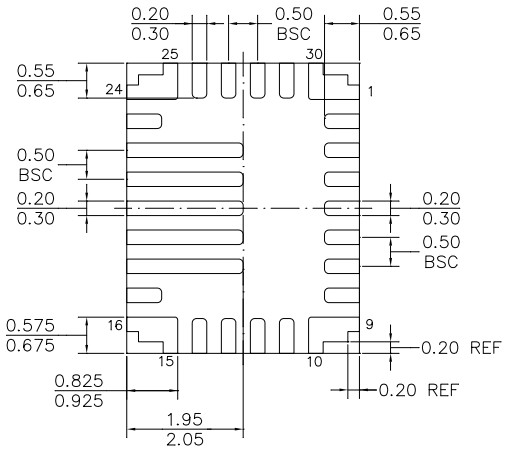
Qty	Ref	Value	Description	Package	Manufacturer
5	C1, C11, C12, C13, C14	10µF	Ceramic capacitor, 35V, X5R	0805	Any
4	C2, C3, C7, C10	22µF	Ceramic capacitor, 35V, X5R	0805	Any
1	C4	4.7µF	Ceramic capacitor, 10V, X5R or X7R	0603	Any
2	C5, C6	100nF	Ceramic capacitor, 25V, X5R or X7R	0603	Any
1	L1	4.7µH	Inductor, 4.7µH, low DCR, I_{SAT} >7.5A	SMD	Any
2	RS1, RS2	10mΩ	Film resistor, 1%	2512	Any
2	RA, RB	5MΩ	Film resistor, 5%	0603	Any
3	AFET1, AFET2, BATFET	5.1mΩ, 30V, 20A	N-channel MOSFET, (SISA14DN-T1-GE3)	Power PAK 1212-8	Vishay

PACKAGE INFORMATION

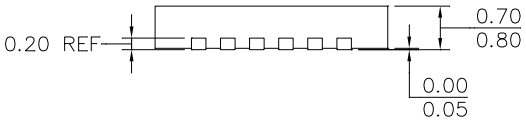
TQFN-30 (4mmx5mm)



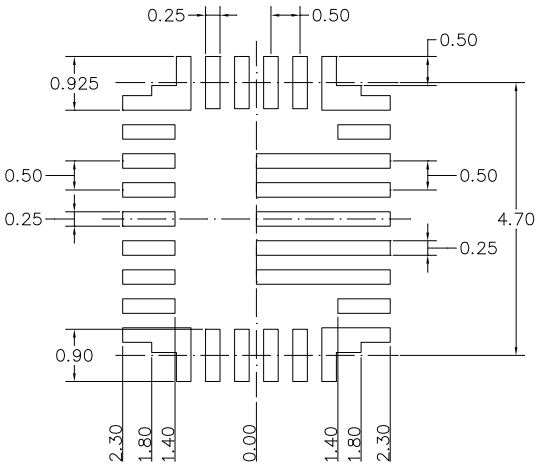
TOP VIEW



BOTTOM VIEW



SIDE VIEW

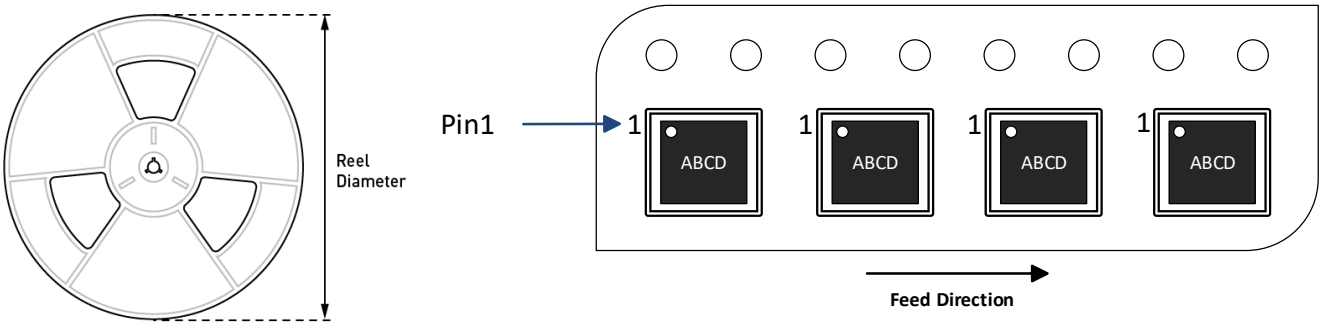


RECOMMENDED LAND PATTERN

NOTE:

1) ALL DIMENSIONS ARE IN MILLIMETERS.
2) LEAD COPLANARITY SHALL BE 0.08 MILLIMETERS MAX.
3) JEDEC REFERENCE IS MO-220.
4) DRAWING IS NOT TO SCALE.

CARRIER INFORMATION



Part Number	Package Description	Quantity/ Reel	Quantity/ Tube	Quantity/ Tray	Reel Diameter	Carrier Tape Width	Carrier Tape Pitch
MP2761GVT-xxxx-Z	TQFN-30 (4mmx5mm)	5000	N/A	N/A	13in	12mm	8mm

REVISION HISTORY

Revision #	Revision Date	Description	Pages Updated
1.0	9/25/2025	Initial Release	-