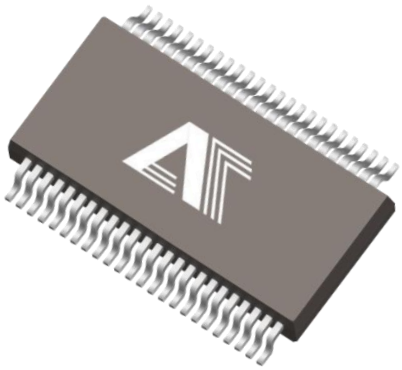
AOTE SEMICONDUCTOR



# LCD control driver circuit

# HT1621B

## Product Data Sheet

AOTE DCC
RELEASE

## ◆ Summary ：

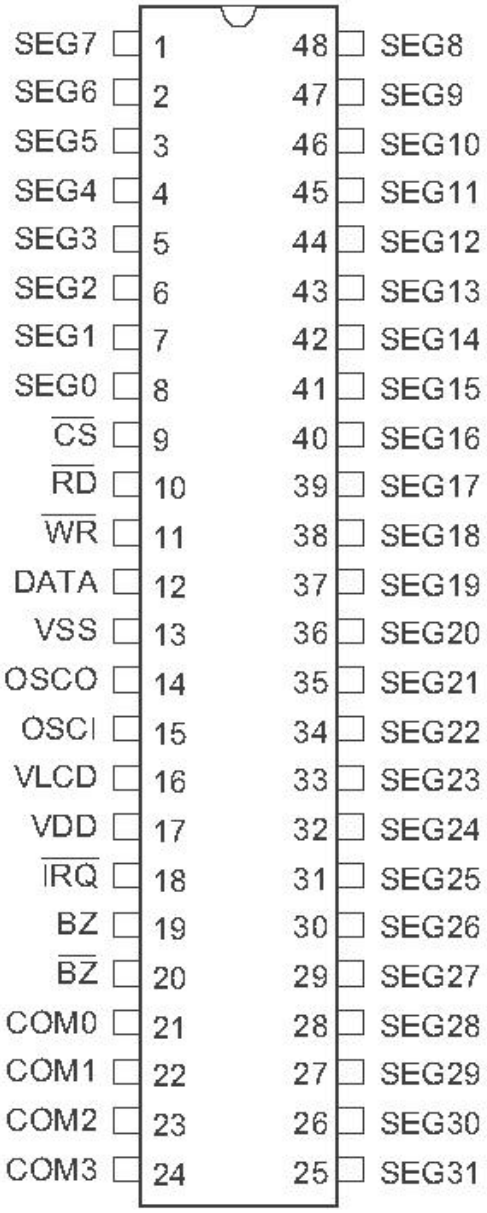
1621B is a peripheral device used to expand the I/O ports of MCU. The display matrix is 32 × 4, which is a 128 dot matrix memory mapped multifunctional LCD driver circuit. The software features of 1621B make it very suitable for application in LCD displays, including LCD modules and display subsystems. The interface application between the main controller and 1621B only requires 3 or 4 ports.

The Power down command can reduce power consumption.

## ◆ Product features

- Working voltage: 2.4V~5.2V
- 256kHz built-in RC oscillation circuit
- External 32.768kHz crystal oscillator or 256kHz clock input
- 1/2 or 1/3 bias, 1/2, 1/3 or 1/4 duty cycle
- Internal Time Base Frequency Source
- Two buzzer frequencies to choose from (2kHz/4kHz)
- The Power down command reduces power consumption
- Internal Time Base and WDT Watchdog Circuit
- Overflow output of Time base/WDT
- There are 8 types of Time Base/WDT clocks available
- 32x4 LCD driver
- 32x4 bit display RAM
- 3-terminal serial interface
- Internal LCD driver frequency
- Software Settings
- Data mode and command mode instructions
- Automatic accumulation of R/W addresses
- Three data access modes
- Use VLCD terminals to regulate LCD voltage, VLCD
- The voltage must be less than or equal to the VDD voltage

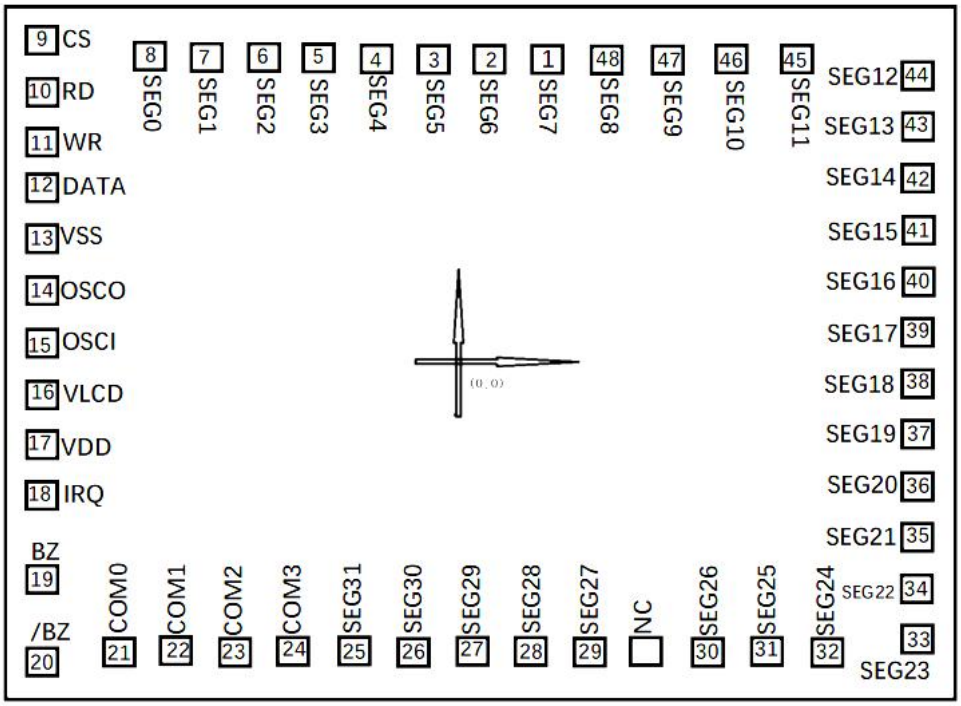
## ◆ Pin arrangement diagram




**HT1621B**

**SSOP-48-300mil**

## ◆ PAD diagram

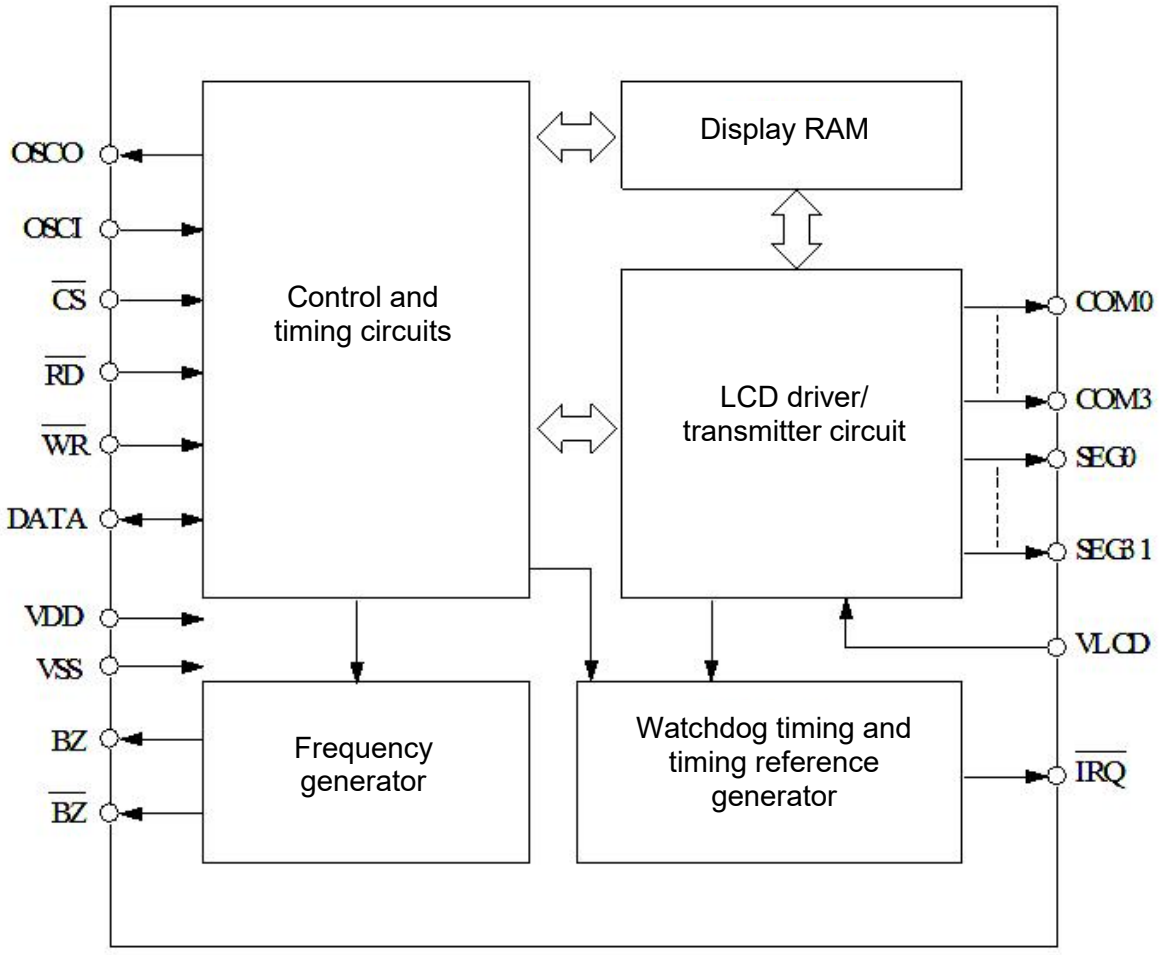



**Chip area: 1.56 * 1.27 mm2, chip substrate connection: VDD**

## ◆ Pin description

| Serial number | Name | I/O | Functional Description |
|---|---|---|---|
| 9 | ¬ CS | I | Chip selection signal input terminal (with pull-up resistor). When logic high-level data and commands cannot be read or written, the serial interface circuit is reset. But if it is a logic low level, data and commands can be transmitted between the controller and 1621B。 |
| 10 | ¬ RD | I | READ clock input terminal (with pull-up resistor). The data in RAM is output to the DATA line at the falling edge of the signal, and the main controller can latch this data at the next rising edge. |
| 11 | ¬ WR | I | WRITE clock input terminal (with pull-up resistor). At the rising edge of the signal, the data on the DATA line is latched to 1621B. |
| 12 | DATA | I/O | Serial data input/output terminal (with pull-up resistor). |
| 13 | VSS | _ | Grounding terminal |
| 15 | OSCI | I | The OSCI and OSCO terminals are connected to a 32.768kHz crystal oscillator for generating the system clock. If an external clock is used, connect it to the OSCI terminal. But if an on-chip RC oscillator circuit is used, the OSCI and OSCO terminals will be suspended. |
| 14 | OSCO | O | |
| 16 | VLCD | I | LCD voltage input terminal |
| 17 | VDD | _ | power supply voltage |
| 18 | ¬ IRQ | O | Time base or WDT overflow flag, N-tube open leak output |
| 19,20 | ¬ BZ,BZ | O | 2kHz or 4kHz buzzing frequency output |
| 21~24 | COM0~COM3 | O | LCD common terminal output |
| 1~8<br>25~48 | SEG7~SEG0<br>SEG31~SEG8 | O | LCD segment output |

## ◆ Functional Block Diagram




## ◆ Functional Description

Display Storage - RAM Structure

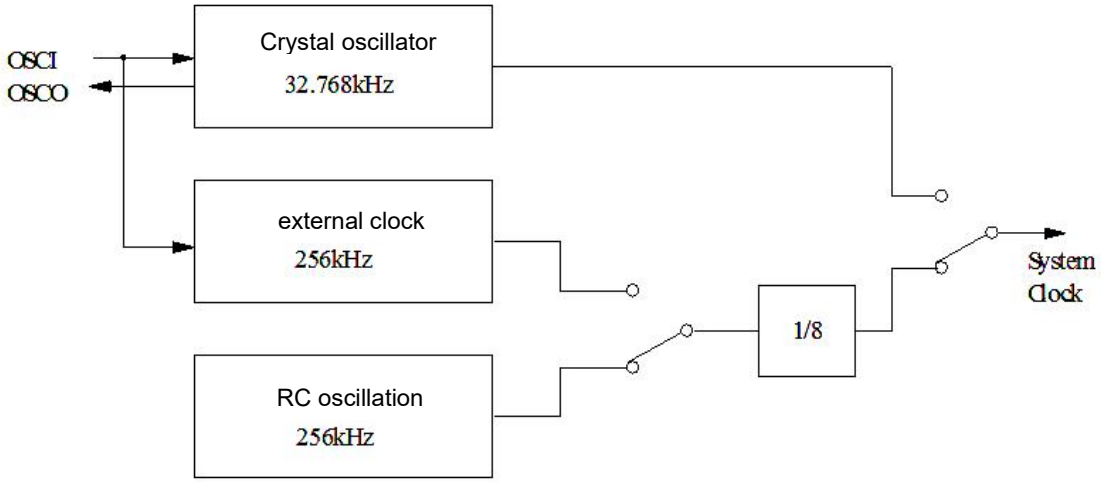
The static display memory (RAM) has a structure of 32×4 bits and stores the displayed data. The content of RAM is directly mapped to the content of the LCD driver. Store data in RAM using read, write, and read modify write commands. The process of mapping the content from RAM to LCD is shown in the following table:

| | COM3 | COM2 | COM1 | COM0 | |
|---|---|---|---|---|---|
| SEG0 | | | | 0 | Address 6-digit (A5，A4...A0) |
| SEG1 | | | | 1 | |
| SEG2 | | | | 2 | |
| SEG3 | | | | 3 | |
| ⋮ | | | | ⋮ | |
| SEG31 | | | | 31 | |
| | D3 | D2 | D1 | D0 | Data\Addr |

## ◆ System oscillator

The clock of HT1621B is used to generate the clock frequency of Timebase/WDT, LCD driver clock, and buzzer frequency. This clock comes from an on-chip 256kHz RC oscillator, an external 32.768kHz crystal oscillator, or an external 256kHz clock set by S/W. The setting of system oscillation is shown in the following figure. After executing the SYSDIS command, the system clock stops and the LCD bias generator will also stop working. This command is only applicable to on-chip RC oscillation or external crystal oscillator. Once the system clock stops, the LCD display will darken and the timing reference/WDT will also lose its function.

The LCD OFF command is used to turn off the LCD bias generator. After the LCD OFF command turns off the LCD bias generator, execute the SYSDIS command to reduce power consumption, similar to the Power down command. But if an external system clock is connected, the SYSDIS command cannot turn off oscillation or enter Power down mode. The crystal oscillator can be connected to a frequency of 32kHz outside the OSI port. In this case, the system will not be able to enter Power down mode, similar to an external 256kHz clock. When the system is powered on, HT1621B is in SYSDIS state.




System oscillation setting

## ◆ Time base and WDT timing

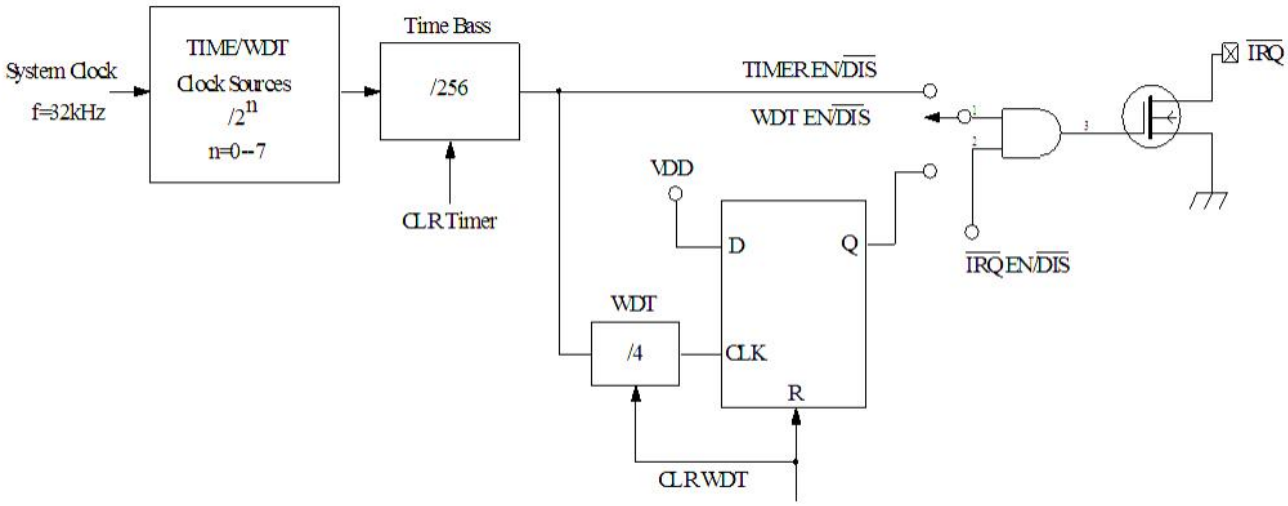
The Time base generator is composed of an 8-level up counter that generates accurate timing. WDT consists of an 8-level Time base generator and a 2-level up counter, which can cause the main controller or subsystem to stop working in abnormal situations (unknown or unwanted jumps, execution errors, etc.). WDT pause, a WDT pause flag will be set. The output of the Time base generator and the output of the WDT pause flag can be output to the ¬ IRQ terminal using commands. There are a total of 8 frequencies that can serve as sources for Time base generators and WDT clocks. The frequency is calculated according to the following formula: $fWDT=32kHz/2^n$, where n ranges from 0 to 7. The 32kHz in the formula represents the frequency of the system, which can be a 32.768kHz crystal oscillator, on-chip oscillation (256kHz), or external oscillation (256kHz).

If an on-chip 256kHz RC oscillator or an external 256kHz clock is selected as the system clock, the system clock is pre-set to 32kHz by a 3-level frequency divider. In this way, both the Time base generator and WDT are related to commands. When using the same 8-level counter, be careful when using commands related to the Time base generator and WDT. For example, calling the WDT DIS command is invalid for the time base generator, while WDT EN is not only applicable to the Time base generator but can also activate the WDT pause flag output (the WDT pause flag is connected to the ¬ IRQ port). After executing the TIMER EN command, WDT is no longer connected to the ¬ IRQ port, and the clock output is connected to the ¬ IRQ port. Executing the CLR WDT command can reset WDT to

zero, and the contents of the Time base generator are reset by the CLRWDT or CLR TIMER command. The CLR WDT or CLR TIMER commands are executed before the WDT EN or TIMER EN commands, respectively. Before executing the ¬ IRQ EN command, the CLR WDT or CLR TIMER command should be executed first. The CLR TIMER command must be executed before transitioning from WDT mode to Time base mode. Once the WDT pause mode occurs, the ¬ IRQ terminal will maintain a logic low level until the CLR WDT or ¬ IRQ DIS command is executed. After the IRQ output is invalid, the IRQ pin will be in a suspended state. By executing the ¬ IRQ EN or ¬ IRQ DIS command, the ¬ IRQ output is in a valid or invalid state.

The ¬ IRQ EN command can output the pause flag of Time base or WDT to the ¬ IRQ port. The clock and WDT settings are as follows. In the case of on-chip RC oscillation or crystal oscillator, the Power down mode will reduce power loss until the oscillation is turned on or off through the corresponding system command. Time base/WDT does not work in Power down mode.

On the other hand, if an external clock is selected as the system clock, the SYS DIS command is invalid and the Power down mode will not be executed. After selecting an external clock, HT1621B will continue to operate until the system is powered off or the external clock is removed. After the system is powered on, ¬ IRQ is disabled.




Timing and WDT settings

The buzzer output has a simple buzzer circuit inside HT1621B. The buzzer oscillator can provide a pair of buzzer driving signals BZ and BZ to generate a buzzer signal. Executing the TONE4k and TONE2k commands allows for the selection of two types of buzzer outputs. The TONE4k and TONE2k commands set the buzzing frequency to 4k and 2k, respectively. The buzzing output can be turned on or off through the TONE ON or TONE OFF command. The buzzer output terminals BZ and BZ are a pair of inverted driving outputs used to drive the piezoelectric buzzer.

| Name | Command code | function |
|---|---|---|
| Beep off | 0000-1000-X | Turn off buzzer output |
| 4k buzzing | 010X-XXXX-X | Turn on the buzzer output, the buzzer frequency is 4kHz |
| 2k buzzing | 011X-XXXX-X | Turn on the buzzer output, the buzzer frequency is 2kHz |

## ◆ LCD driver

HT1621B is a 128 (32 × 4) dot matrix LCD driver. The S/W setting can drive 1/2 or 1/3 bias, 2, 3 or 4 COM end LCD displays, making HT1621B suitable for various LCD displays. The LCD driver clock is generated from the system clock, and regardless of whether the system clock comes from the 32.768kHz

crystal oscillator frequency, on-chip RC oscillator frequency, or external frequency, the frequency of the LCD driver clock is always 256Hz. The corresponding commands for the LCD are shown in the table below.

| Name | Command code | function |
|---|---|---|
| LCD OFF | 10000000010X | Turn off LCD output |
| LCD ON | 10000000011X | Turn on LCD output |
| BIAS&COM | 1000010abXcX | C=0:1/2 bias<br>c=1：1/3 bias ab=00：2COMS<br>ab=01：3COMS<br>ab=10：4COMS |

The 100 in bold indicates the command mode ID. If consecutive commands are sent, the command mode ID (except for the first command) will be ignored. The LCDOFF command turns off the LCD display by interrupting the LCD bias generator, while the LCDON command turns on the LCD display by starting the LCD bias generator. BIAS and COM commands are commands related to LCD displays, and HT1621B can drive many types of LCD displays through this command.

## ◆ Command format

HT1621B can be set through S/W. There are two modes for setting HT1621B and transmitting LCD display data commands, namely command mode and data mode. The setting of HT1621B is called command mode, with an ID of 100, consisting of system setting command, system frequency selection command, LCD structure command, buzzer frequency selection command, and operation command. The data mode includes read, write, and read-write transformation operations. The following table shows the data mode IDs and command mode IDs:

| Conditions | Pattern | ID |
|---|---|---|
| read | data | 110 |
| write | data | 101 |
| The transition between reading and writing | data | 101 |
| command | command | 100 |

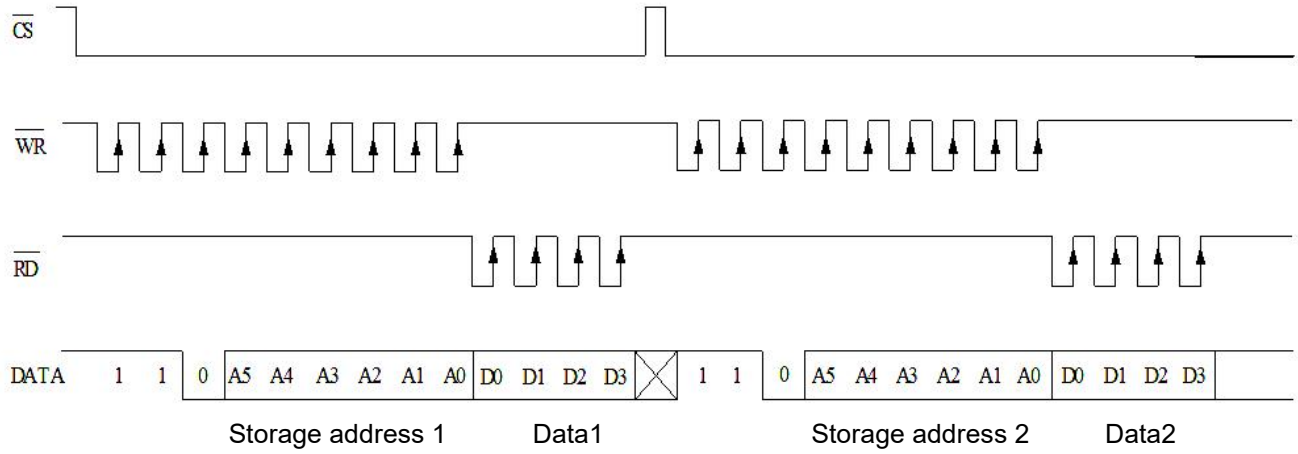
The mode command appears before data and command transmission. If there are consecutive instructions, command mode ID100 can be ignored. When the system operates in discontinuous command or discontinuous address data mode, the CS end should be set to 1, and the previous operating mode will be reset. Once the CS end is 0, a new working mode ID will appear.

## ◆ Interface

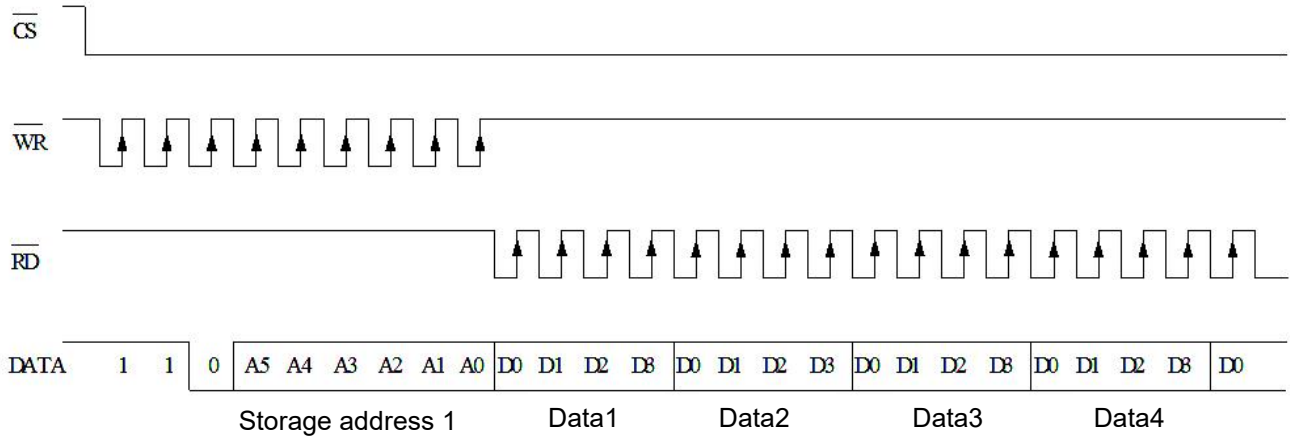
HT1621B has 4 wires that require interfaces. Initialize the serial interface circuit of CS and terminate the communication terminal between the main controller and HT1621B. When CS is 1, data and commands between the main controller and 1621B are disabled and initialized. Before the command mode and mode transition occur, a high-level pulse is required to initialize the serial interface of HT1621B. The data line is a serial input/output line. Reading and writing data or writing commands must be done through a data cable. The RD line is the READ clock input. The data in RAM is read out at the falling edge of the ¬ RD signal, and the read data will be displayed on the DATA line. The main controller reads the correct data between the rising edge and the next falling edge of the READ signal. The WR line is the WRITE clock input. The data, addresses, and commands on the data line are all read to HT1621B on the rising edge of the ¬ WR signal. The IRQ line is used as the interface between the main controller and HT1621B. The IRQ pin is used as a timer output or WDT overflow flag output, set by S/W. The main controller executes the time reference or WDT function through the IRQ pin connected to HT1621B.

## ◆ Sequence diagram

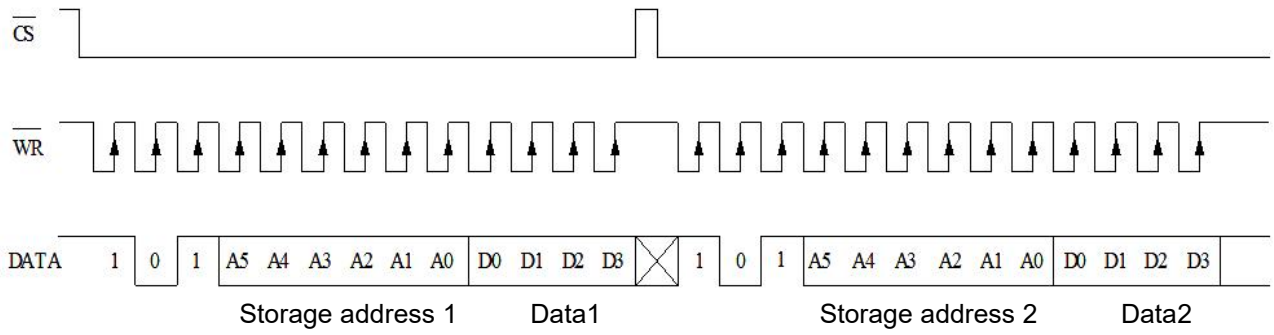
**Read mode (command code: 110)**



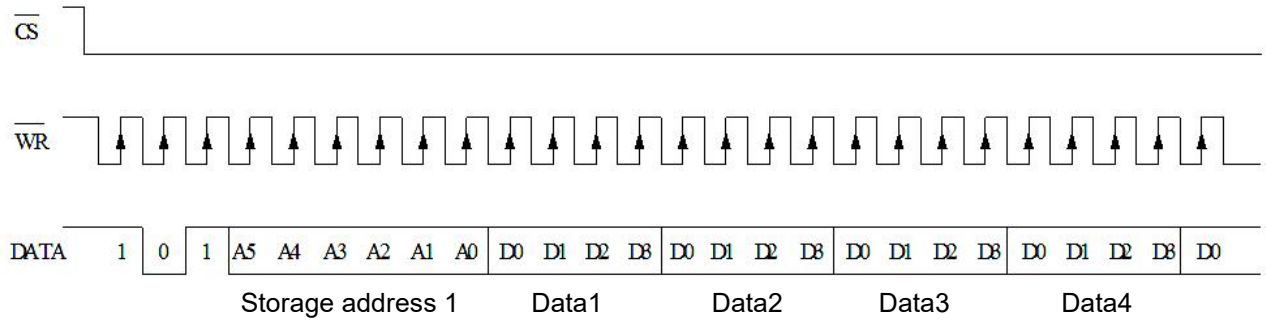

**Read mode (continuous address read)**



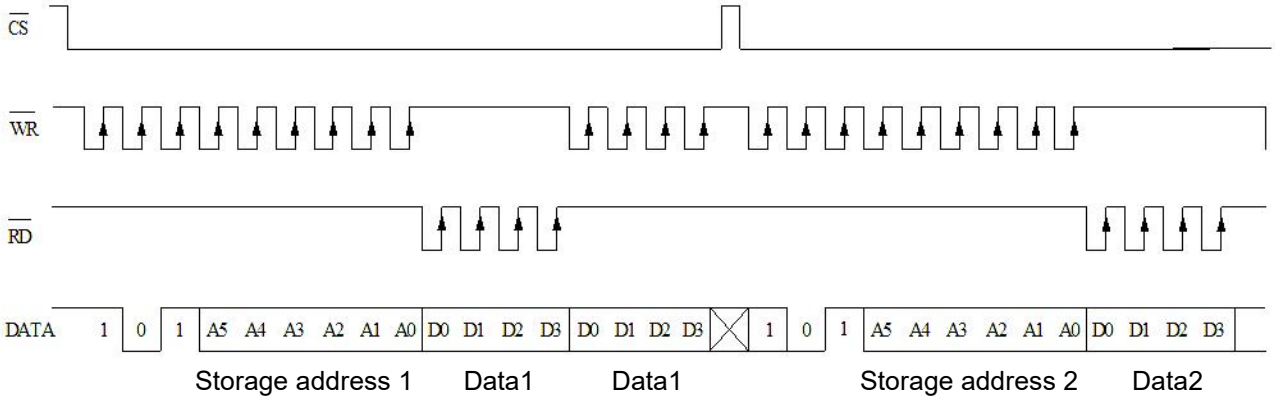

**Write mode (command code: 101)**



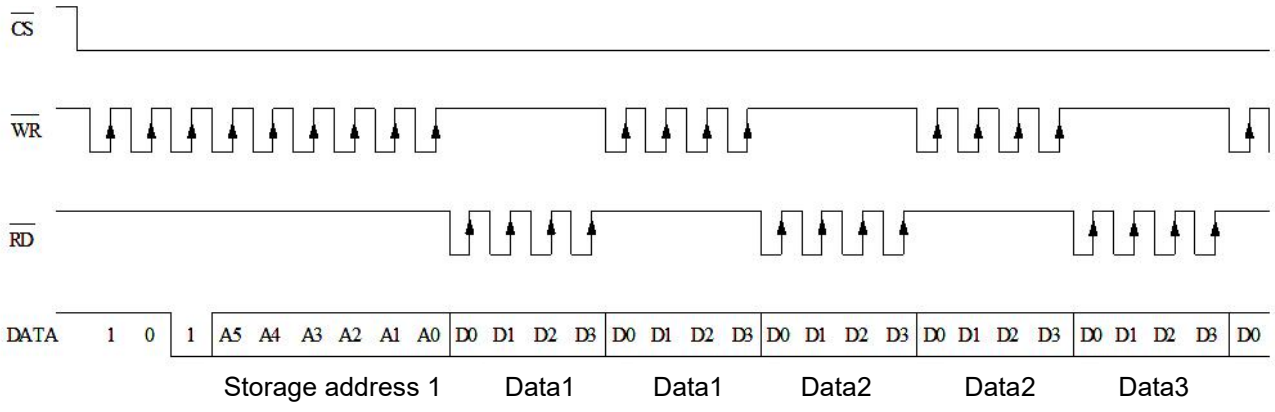
**Write mode (continuous address writing)**



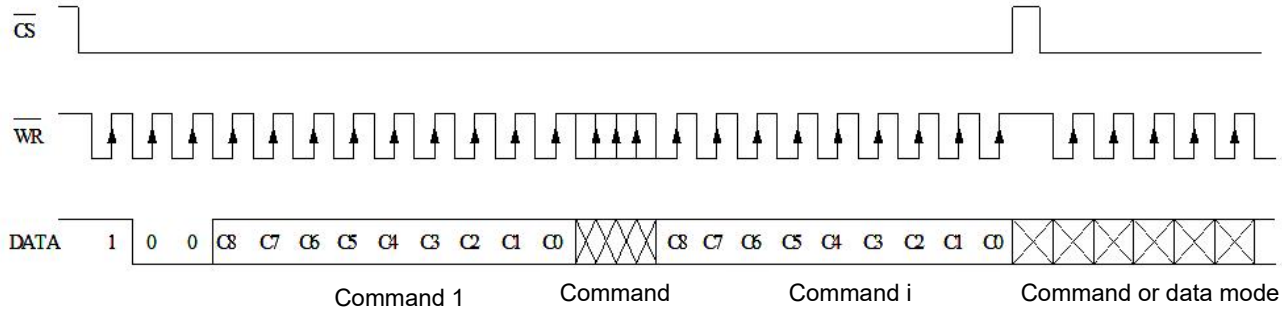

**Read/Write Change Mode (Command Code: 101)**



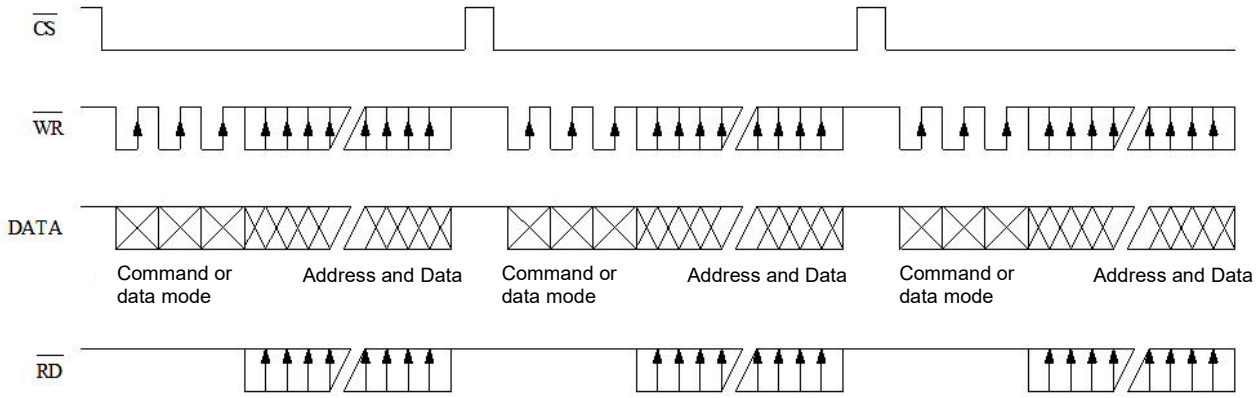

**Read/Write Change Mode (Continuous Address Storage)**



**Command mode (command code: 100)**




**Mode (Data and Command Mode)**



## ◆ Command table

| Name | ,D | Command code | D/C | function | Reset |
|---|---|---|---|---|---|
| READ | 110 | A5A4A3A2A1A0D0D1D2D3 | D | Read data from RAM | |
| WR,TE | 101 | A5A4A3A2A1A0D0D1D2D3 | D | Write data to RAM | |
| READ-MOD,FY-WR,TE | 101 | A5A4A3A2A1A0D0D1D2D3 | D | Read and write data from RAM | |
| SYSD,S | 100 | 0000-0000-X | C | Turn off the system clock and LCD bias generator | YES |
| SYSEN | 100 | 0000-0001-X | C | Open the system clock | |
| LCDOFF | 100 | 0000-0010-X | C | Turn off the LCD bias generator | YES |
| LCDON | 100 | 0000-0011-X | C | Open LCD bias generator | |
| T,MERSD,S | 100 | 0000-0100-X | C | Disable Timebase output | |
| WDTD,S | 100 | 0000-0101-X | C | Prohibit WDT pause flag output | |
| T,MEREN | 100 | 0000-0110-X | C | Allow Timebase output | |
| WDTEN | 100 | 0000-0111-X | C | Allow WDT to pause flag output | |
| TONEOFF | 100 | 0000-1000-X | C | Turn off buzzer output | YES |
| TONEON | 100 | 0000-1001-X | C | Turn on buzzer output | |
| CLRT,MER | 100 | 0000-11XX-X | C | Clear the contents of the Timebase generator | |
| CLRWDT | 100 | 0000-111X-X | C | Clear the contents of WDT | |
| XTAL32k | 100 | 0001-01XX-X | C | System clock, crystal oscillator | |
| RC256k | 100 | 0001-10XX-X | C | System clock, on-chip RC oscillation | YES |
| EXT256k | 100 | 0001-11XX-X | C | External clock | |
| B,AS1/2 | 100 | 0010-abX0-X | C | LCD1/2offset setting ab=00：2COMS<br>ab=01：3COMS<br>ab=10：4COMS | |
| B,AS1/3 | 100 | 0010-abX1-X | C | LCD1/3offset setting ab=00：2COMS<br>ab=01：3COMS<br>ab=10：4COMS | |
| TONE4k | 100 | 010X-XXXX-X | C | Beep frequency output：4kHZ | |
| TONE2k | 100 | 011X-XXXX-X | C | Beep frequency output出：2kHZ | |
| ,RQD,S | 100 | 100X-0XXX-X | C | Prohibited, RQ output | YES |
| ,RQEN | 100 | 100X-1XXX-X | C | Allow, RQ output | |
| F1 | 100 | 101X-X000-X | C | TImebase/WDT clock output: 1HZ WDT pause flag: 4s | |
| F2 | 100 | 101X-X001-X | C | Timebase/WDT clock output: 2HZWDT pause flag: 2s | |
| F4 | 100 | 101X-X010-X | C | Timebase/WDT clock output: 4HZ WDT pause flag: 1s | |
| F8 | 100 | 101X-X011-X | C | Time base/WDT clock output: 8HZ WDT pause flag: 1/2s | |
| F16 | 100 | 101X-X100-X | C | Timebase/WDT clock output: 16HZWDT pause flag: 1/4s | |
| F32 | 100 | 101X-X101-X | C | Timebase/WDT clock output: 32HZWDT pause flag: 1/8s | |
| F64 | 100 | 101X-X110-X | C | Timebase/WDT clock output: 64HZWDT pause flag: 1/16s | |
| F128 | 100 | 101X-X111-X | C | Timebase/WDT clock output: 128HZWDT pause flag: 1/32s | YES |
| TEST | 100 | 1110-0000-X | C | test mode | |
| NORMAL | 100 | 1110-0011-X | C | Normal Mode | YES |

Note: A5~A0: RAM address D3-D0: RAM data D/C: Data/Command Mode

## ◆ Limiting parameters

| Characteristics | Symbol | Limit value | Unit |
|---|---|---|---|
| power supply voltage | $V_{DD}$ | -0.3 ~ 5.5 | V |
| input voltage | $V_{IN}$ | $V_{SS}$-0.3 ~ $V_{DD}$+0.3 | V |
| Storage temperature | $T_{STG}$ | -50 ~ +125 | ℃ |
| Operating temperature | $T_{OTG}$ | -25 ~ +75 | ℃ |

## ◆ Electrical parameters

DC parameters

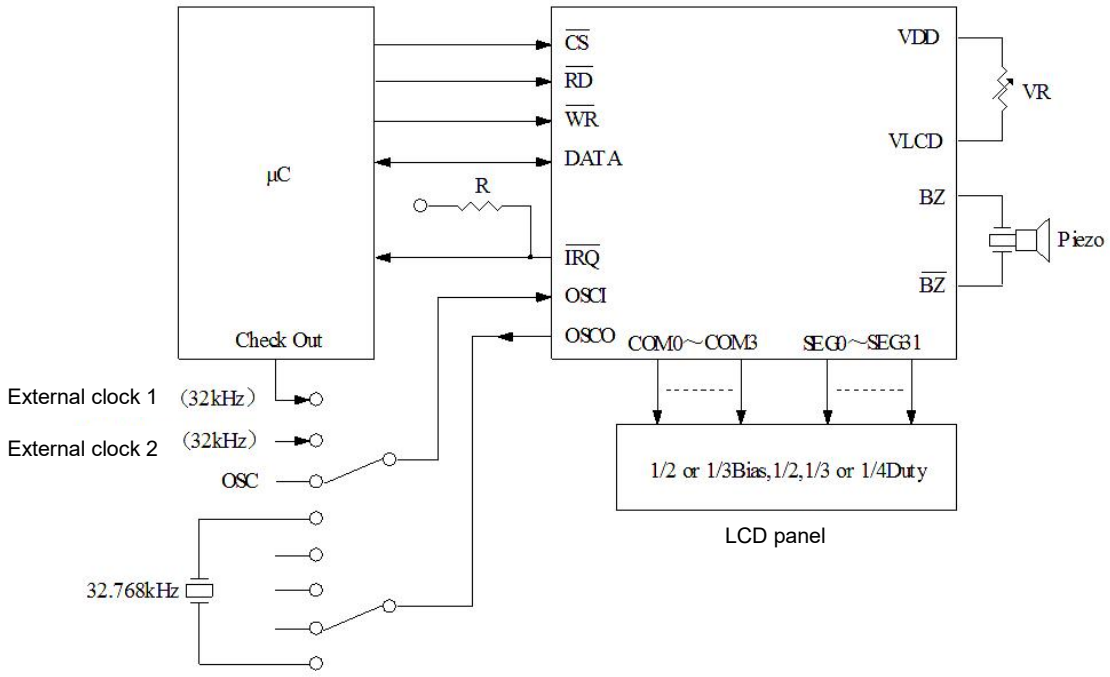
| Name | Symbol | Min | Typ | Max | Unit | Test conditions | |
|---|---|---|---|---|---|---|---|
| | | | | | | Vdd | Conditions |
| Working voltage | VDD | 2.4 | - | 5.2 | V | - | - |
| operating current | IDD1 | - | 150 | 300 | μA | 3V | No load/LCD open on-chip RC oscillation |
| | | | 300 | 600 | | 5V | |
| operating current | IDD2 | - | 60 | 120 | μA | 3V | No load/LCD, open crystal oscillator |
| | | | 120 | 240 | | 5V | |
| operating current | IDD3 | - | 100 | 200 | μA | 3V | No load/LCD, turn off external clock |
| | | - | 200 | 400 | | 5V | |
| standby current | ISTB | - | 0.1 | 5 | μA | 3V | no-load power shutdown mode |
| | | - | 0.3 | 10 | | 5V | |
| Input low voltage | VIL | 0 | - | 0.6 | V | 3V | DATA,¬ WR,¬ CS,¬ RD |
| | | 0 | | 1.0 | | 5V | |
| Input high voltage | VIH | 2.4 | - | 3.0 | V | 3V | DATA,¬ WR,¬ CS,¬ RD |
| | | 4.0 | - | 5.0 | | 5V | |
| DATA,BZ,¬ BZ,¬ IRQ | IOL1 | 0.5 | 1.2 | - | mA | 3V | VOL=0.3V |
| | | 1.3 | 2.6 | - | | 5V | VOL=0.5V |
| DATA,BZ,¬ BZ | IOH1 | -0.4 | -0.8 | - | mA | 3V | VOH=2.7V |
| | | -0.9 | -1.8 | - | | 5V | VOH=4.5V |
| LCD Common terminal current injection | IOL2 | 80 | 150 | - | μA | 3V | VOL=0.3V |
| | | 150 | 250 | - | | 5V | VOL=0.5V |
| LCD Public terminal pulling current | IOH2 | -80 | -120 | | μA | 3V | VOH=2.7V |
| | | -120 | -200 | - | | 5V | VOH=4.5V |
| LCDSEG End irrigation current | IOL3 | 60 | 120 | | μA | 3V | VOL=0.3V |
| | | 120 | 200 | | | 5V | VOL=0.5V |
| LCDSEG End irrigation current | IOH3 | -40 | -70 | - | μA | 3V | VOH=2.7V |
| | | -70 | -100 | | | 5V | VOH=4.5V |
| pull-up resistor | RPH | 40 | 80 | 150 | kΩ | 3V | DATA,¬ WR,¬ CS,¬ RD |
| | | 30 | 60 | 100 | | 5V | |

## ◆ Electrical parameters

AC parameters

| Name | Symbol | Min | Typ | Max | Unit | Test conditions | |
|---|---|---|---|---|---|---|---|
| | | | | | | Vdd | Conditions |
| System clock | fSYS1 | - | 256 | - | kHz | 3V | On-chip RC oscillation |
| | | - | 256 | - | | 5V | |
| System clock | fSYS2 | - | 32.768 | - | kHz | 3V | Crystal oscillator |
| | | | 32.768 | | | 5V | |
| System clock | fSYS3 | - | 256 | - | kHz | 3V | External clock |
| | | - | 256 | - | | 5V | |
| LCD frequency | fLCD1 | - | fSYS1/ 1024 | - | Hz | - | On-chip RC oscillation |
| | | - | fSYS2/128 | - | | | Crystal oscillator |
| | | | fSYS3/ 1024 | | | | External clock |
| LCD Public end cycle | tCOM | - | n/fLCD | - | sec | - | N: Number of public terminals |
| Serial data clock (¬ WR end) | FCLK1 | - | - | 150 | kHz | 3V | Duty cycle 50% |
| | | | | 300 | | 5V | |
| Serial data clock (RD end) | FCLK2 | - | - | 75 | kHz | 3V | Duty cycle 50% |
| | | | | 150 | | 5V | |
| Serial interface reset pulse width | tCS | - | 250 | - | ns | - | ¬ CS |
| WR, RD input pulse width | tCLK | 3.34 | - | - | μs | 3V | Writing mode |
| | | 6.67 | - | - | | | Reading mode |
| | | 1.67 | - | - | μs | 5V | Writing mode |
| | | 3.34 | - | - | | | Reading mode |
| Rise/Fall Time Serial Data Time Width | tr ， tf | - | 120 | - | ns | 3V | - |
| | | | | | | 5V | |
| Data to WR, Setting time for RD width | tsu | | 120 | | ns | 3V | |
| | | | | | | 5V | |
| Data to ¬ WR, Retention time of RD width | th | - | 120 | - | ns | 3V | - |
| | | | | | | 5V | |
| From CS to WR, Setting time for RD width | tsu1 | | 100 | | ns | 3V | |
| | | | | | | 5V | |
| From CS to WR, Retention time of RD width | th1 | | 100 | | ns | 3V | |
| | | | | | | 5V | |

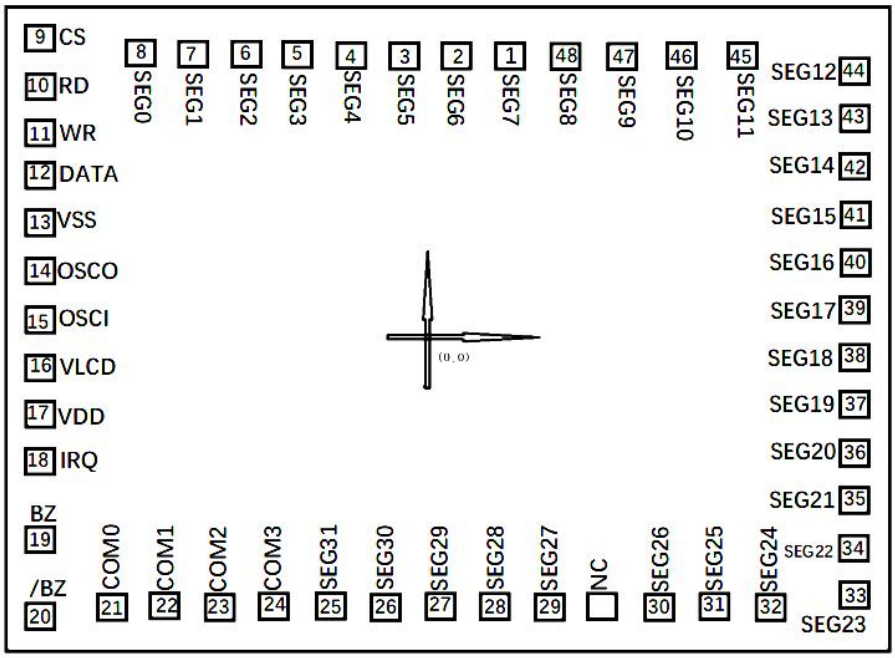
## ◆ Reference application route




*This circuit is for reference only.

VLCD power supply must be less than or equal to VDD voltage.

## ◆ Schematic diagram of pressure welding point




Chip area: 1.56 * 1.27 mm2, chip substrate connection: VDD

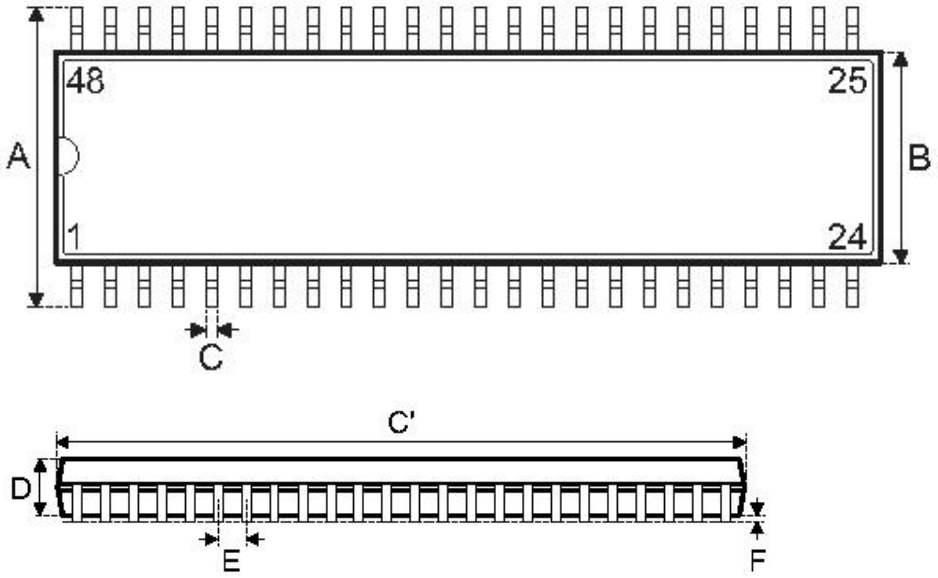
## ◆ Coordinates of chip solder joints

**Chip center point coordinates: (0,0) (required to be 0,0)**

| Serial number | Name | X-coordinate | Y-coordinate | Serial number | Name | X-coordinate | Y-coordinate |
|---|---|---|---|---|---|---|---|
| 1 | SEG7 | 185.7 | 548 | 25 | SEG31 | -182.3 | -548 |
| 2 | SEG6 | 93.7 | 548 | 26 | SEG30 | -90.3 | -548 |
| 3 | SEG5 | 1.7 | 548 | 27 | SEG29 | 1.7 | -548 |
| 4 | SEG4 | -90.3 | 548 | 28 | SEG28 | 93.7 | -548 |
| 5 | SEG3 | -182.3 | 548 | 29 | SEG27 | 185.7 | -548 |
| 6 | SEG2 | -274.3 | 548 | NC | SEG28(NC) | 277.7 | -548 |
| 7 | SEG1 | -366.3 | 548 | 30 | SEG26 | 369.7 | -548 |
| 8 | SEG0 | -458.3 | 548 | 31 | SEG25 | 461.7 | -548 |
| 9 | CSB | -692.7 | 569.4 | 32 | SEG24 | 553.7 | -548 |
| 10 | RDB | -692.7 | 477.4 | 33 | SEG23 | 692.8 | -506 |
| 11 | WRB | -692.7 | 385.4 | 34 | SEG22 | 692.8 | -414 |
| 12 | DATA | -692.7 | 265.8 | 35 | SEG21 | 692.8 | -322 |
| 13 | VSS | -692.7 | 153.4 | 36 | SEG20 | 692.8 | -230 |
| 14 | OSCO | -692.7 | 61.4 | 37 | SEG19 | 692.8 | -138 |
| 15 | OSCI | -692.7 | -30.6 | 38 | SEG18 | 692.8 | -46 |
| 16 | VLCD | -692.7 | -122.6 | 39 | SEG17 | 692.8 | 46 |
| 17 | VDD | -692.7 | -216.3 | 40 | SEG16 | 692.8 | 138 |
| 18 | IRQB | -692.7 | -310 | 41 | SEG15 | 692.8 | 230 |
| 19 | BZ | -692.7 | -429.6 | 42 | SEG14 | 692.8 | 322 |
| 20 | BZB | -692.7 | -553.6 | 43 | SEG13 | 692.8 | 414 |
| 21 | COM0 | -550.3 | -548 | 44 | SEG12 | 692.8 | 506 |
| 22 | COM1 | -458.3 | -548 | 45 | SEG11 | 553.7 | 548 |
| 23 | COM2 | -366.3 | -548 | 46 | SEG10 | 461.7 | 548 |
| 24 | COM3 | -274.3 | -548 | 47 | SEG9 | 369.7 | 548 |
| | | | | 48 | SEG8 | 277.7 | 548 |

Note: Pads marked with "NC" are suspended

## ◆ Encapsulated Information




| Symbol | Dimensions in inch | | |
|---|---|---|---|
| | Min. | Nom. | Max. |
| A | - | 0.472 BSC | - |
| B | - | 0.394 BSC | - |
| C | - | 0.472 BSC | - |
| D | - | 0.394 BSC | - |
| E | - | 0.032 BSC | - |
| F | 0.012 | 0.015 | 0.018 |
| G | 0.053 | 0.055 | 0.057 |
| H | - | - | 0.063 |
| I | 0.002 | - | 0.006 |
| J | 0.018 | 0.024 | 0.030 |
| K | 0.004 | - | 0.008 |
| α | 0° | - | 7° |

| Symbol | Dimensions in inch | | |
|---|---|---|---|
| | Min. | Nom. | Max. |
| A | - | 12.00 BSC | - |
| B | - | 10.00 BSC | - |
| C | - | 12.00 BSC | - |
| D | - | 10.00 BSC | - |
| E | - | 0.80 BSC | - |
| F | 0.30 | 0.37 | 0.45 |
| G | 1.35 | 1.40 | 1.45 |
| H | - | - | 1.60 |
| I | 0.05 | - | 0.15 |
| J | 0.45 | 0.60 | 0.75 |
| K | 0.09 | - | 0.20 |
| α | 0° | - | 7° |

## ◆ Attention

- AOTE implements dynamic technical updates. Specifications are subject to change. Refer to the official website for the latest version.
- Users must strictly adhere to specified conditions. Failures caused by misuse (overload, high temperature, incompatible circuits) are excluded from warranty.
- Contact technical support for customized validation in critical applications (medical devices, industrial control).
- This document is valid until December 31, 2026. Updates will be notified on the official website.
- For further clarification on technical specifications or application solutions, please contact us through official channels: