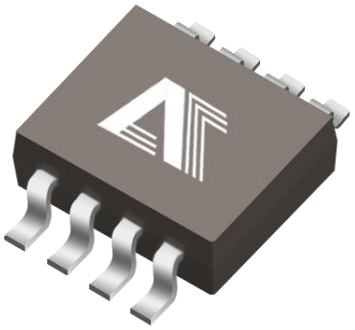
AOTE
SEMICONDUCTOR



# Real time clock (RTC)

# DS1302Z

## Product Data Sheet

AOTE DCC
RELEASE

## ◆ Summary ：

The DS1302Z trickle charging timing circuit includes a real-time clock/calendar and 31 bytes of static RAM, which communicates with the microprocessor through a simple serial interface. This real-time clock/calendar provides information on year, month, day, hour, minute, and second. It automatically adjusts at the end of months with less than 31 days, and also corrects for leap years. Due to the presence of an AM/PM indicator, the clock can operate in either 12 hour or 24-hour format.

In addition to the timing function, it also has the following features: dual pin main power supply and backup power supply, programmable trickle charger VCC1, and a 31 byte register. Widely used in product fields such as telephone, fax, portable instruments, and battery powered instruments. DS1302Z adopts SOP8 packaging.

## ◆ Product features

- Real time clock calculates year, month, day, hour, minute, second, and week until the year 2100, and has leap year adjustment function.
- 31x8 bit general-purpose temporary storage RAM.
- Serial input/output minimizes the number of pins.
- Operating within a wide voltage range of 2.0V to 5.5V.
- The operating current is less than 300mA at 2.0V.
- There are single byte or multi byte (burst mode) data transfer methods for reading and writing clock or RAM data
- 8-pin DIP package or optional 8-pin surface mount S0P package.
- Simple 3-wire interface.
- Compatible with TTL (VCC=5V).
- Civilian temperature range: -40 ℃ to+85 ℃.

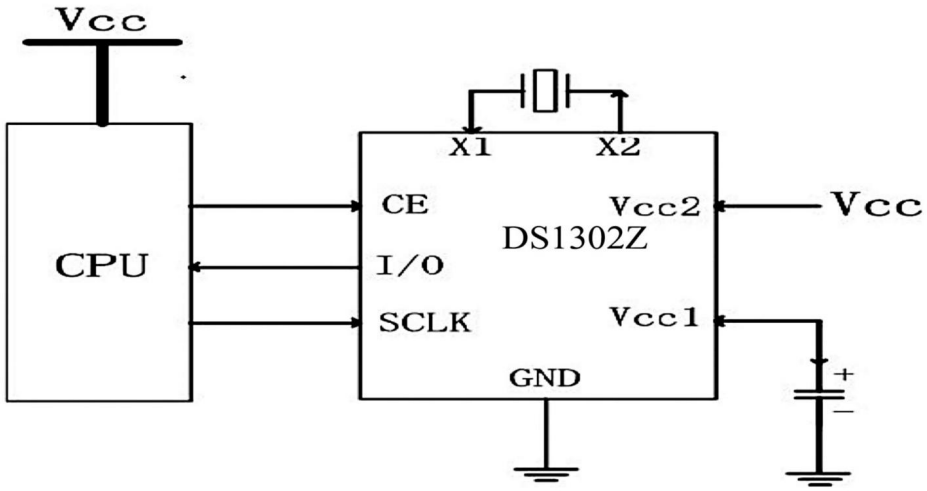
## ◆ Applications

- Telephone
- Fax
- Portable instrument
- Instrumentation and meters

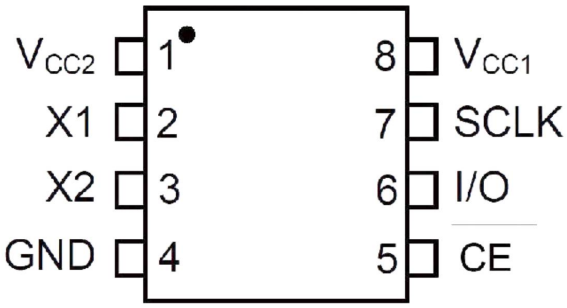
## ◆ Product ordering information

| Product Name | Encapsulation | Packaging | Packaging Quantity |
|---|---|---|---|
| DS1302Z | SOP-8 | Tube packaging | 100 pieces/tube<br>2500 pieces/plate |

- **Typical application diagram**



## ◆ Pin Function Definition




| Pin number | Pin name | I/O | Description |
|---|---|---|---|
| 1 | VCC2 | P | The main power supply pin in the dual power supply configuration, VCC1, is connected to the backup power supply and maintains time and date data in the event of a main power failure. DS1302Z operates on the larger of VCC1 and VCC2. When VCC2 is 0.2V higher than VCC1, VCC2 supplies power to DS1302Z; When VCC1 is higher than VCC2, VCC1 supplies power to DS1302Z. |
| 2 | X1 | I | The main power supply pin in the dual power supply configuration, VCC1, is connected to the backup power supply and maintains time and date data in the event of a main power failure. DS1302Z operates on the larger of VCC1 and VCC2. When VCC2 is 0.2V higher than VCC1, VCC2 supplies power to DS1302Z; When VCC1 is higher than VCC2, VCC1 supplies power to DS1302Z. |
| 3 | X2 | O | |
| 4 | GND | P | power ground |
| 5 | CE | I | Input. The CE signal must maintain a high level during reading and writing, and there is a 40k Ω (typical value) pull-down resistor connected to ground inside this pin. |
| 6 | I/O | I/O | Input/push-pull output. The I/O pin is a bidirectional data pin of a three wire interface, which has a 40k Ω (typical value) pull-down resistor connected to ground inside. |
| 7 | SLCK | I | Input. SCLK is used to synchronize data actions on the serial interface, and this pin has a 40k Ω (typical value) pull-down resistor connected to ground. |
| 8 | VCC1 | P | Low power operation in single power and battery operating systems and low-power backup batteries, in systems using trickle charging, this pin is connected to a rechargeable energy source. UL certification ensures the avoidance of reverse charging current when using lithium batteries. |

## ◆ Oscillating circuit

DS1302Z uses an external 32.768kHz crystal, and does not require any external resistors or capacitors to operate the oscillation circuit. Table 1 provides detailed parameters of several external crystals, while Figure 1 shows a functional schematic of the oscillation circuit. If using crystals of specified specifications, the startup time is usually less than 1 second.

**Table 1 Detailed Explanation of Crystal Oscillators**

| Parameter | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| Nominal frequency | f0 | - | 32.768 | - | kHz |
| Resonant resistor | ESR | - | 45 | - | k Ω |
| load capacitance | CL | - | 6 | - | pF |

◆ **Figure 1 Internal functional block diagram**

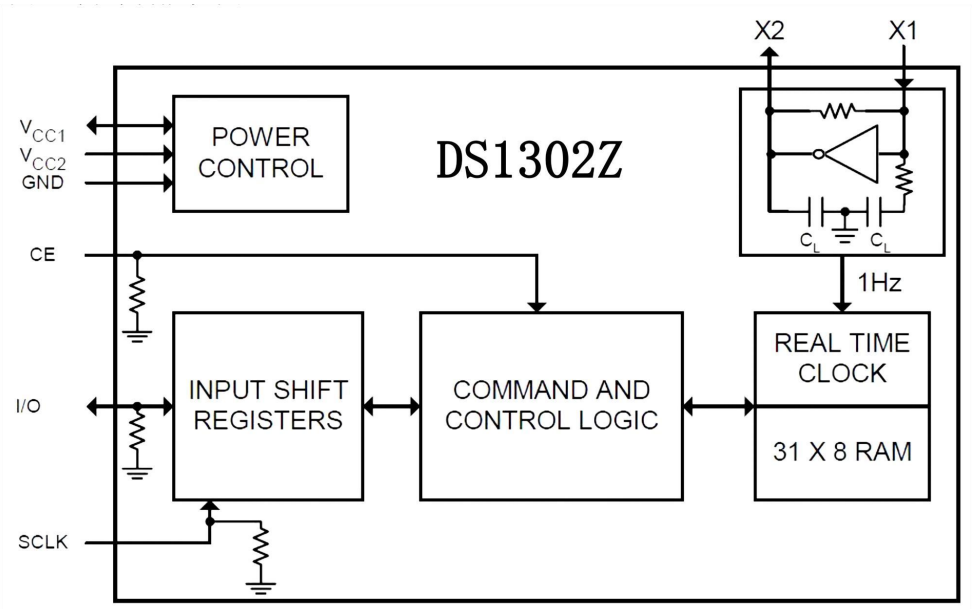
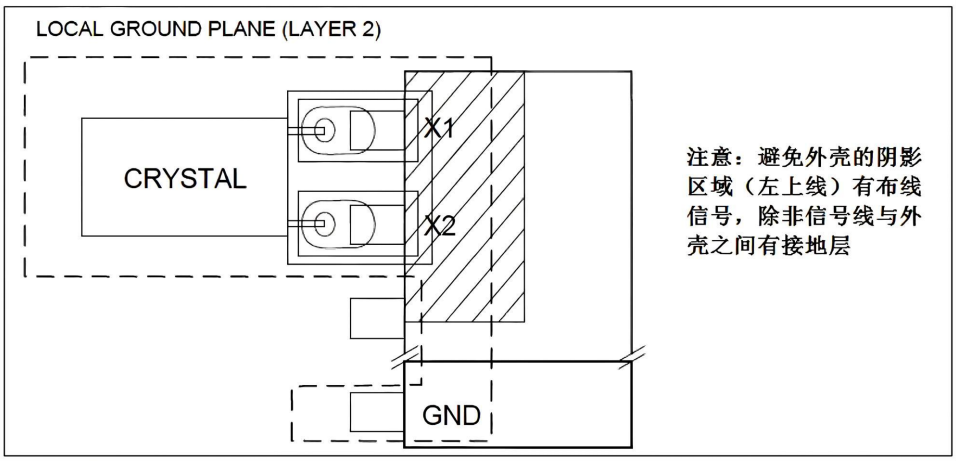



Figure 1 shows the main elements of a serial timer: shift register, control logic, oscillator, real-time clock, and RAM.

**Clock accuracy**

The accuracy of a clock depends on the precision of the crystal oscillator and the accuracy of the matching between the capacitive load of the oscillation circuit and the capacitive load calibrated by the crystal oscillator. To improve the accuracy of travel time, a set of 10pF-33pF load compensation capacitors should be installed externally at the crystal oscillator end, and the specific capacitance value depends on the application layout and crystal oscillator. In addition, the frequency drift of the crystal oscillator caused by temperature changes can increase errors, and the coupling of peripheral circuit noise and oscillation circuit may lead to faster clock operation. Figure 2 shows a typical printed circuit board layout that isolates crystal and oscillator noise.

◆ **Figure 2 Typical layout of crystal oscillator printed circuit board**



### command word

Figure 3 shows the command word, which initiates each data transfer, and MSB (bit 7) must be logic 1. If it is 0, writing to DS1302Z is prohibited. Bit 6 is designated as clock/calendar data at logic 0 and as RAM data at logic 1. Bits 1 to 5 represent the designated registers for input and output, with LSB (bit 0) being a write operation (output) at logic 0 and a read operation (input) at logic 1. Command words starting with LSB (bit 0) are always input.

◆ **Figure 3 Address/Command Word**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| 1 | RAM / $\overline{CK}$ | A4 | A3 | A2 | A1 | A0 | RD / $\overline{WR}$ |

### CE and Clock Control

All data transmission starts driving CE input high. CE input implements two functions. Firstly, CE enables control logic that allows reading and writing of shift registers for address/command sequences; Secondly, the CE signal provides a termination method for single byte and multi byte CE data transmission.

A clock cycle is a series of rising edges accompanied by falling edges. To input data, the rising edge of the clock must be valid, and the falling edge must output data bits. If the CE input is low, all data transmission is terminated and the I/O port is in a high impedance state. Figure 4 shows data transmission, which must be logic 0 until VCC is greater than 2.0V when powered on. Similarly, when CE changes to logic 1 state, SCLK must be logic 0.

### Data input

After inputting the command word for 8 SCLK cycles, the rising edge data bytes of the next 8 SCLK cycles are inputted. If this happens accidentally, the excess SCLK cycles will be ignored and data input will start with bit 0.

### Data output

After inputting the read command word for 8 SCLK cycles, the falling edge of the following 8 SCLK cycles outputs one data byte. Note that the transmission of the first data bit occurs at the first falling edge after the command byte is written, and CE remains high. If this happens accidentally, the excess SCLK cycle will resend the data byte. This operation allows for continuous pulse train mode reading capability, and the VO pin is set to three states at each rising edge of SCLK, with data output starting from bit 0.

### Pulse train mode

By addressing the 31 (decimal) storage unit (address/command bits 1 to 5 are logic 1), the burst mode can specify clock/calendar or RAM registers. As mentioned earlier, bit 6 specifies clock or RAM, and bit 0 specifies read and write. The storage units 9 to 31 of the clock/calendar register and the storage unit 31 of the RAM register have no data storage capacity, and read and write in burst mode start from bit 0 of address 0. When writing clock registers in burst mode, the first 8 registers must write the data to be sent in sequence. However, when writing RAM in burst mode, it is not necessary to write all 31 bytes of data to be sent. Regardless of whether all 31 bytes are written or not, each written byte will be sent to RAM.

## Clock/Calendar

Reading appropriate register bytes can obtain time and calendar information. Table 3 illustrates the RTC registers, where writing appropriate register bytes can set or initialize time and calendar. The contents of the time and calendar registers are in binary encoded decimal (BCD) format. The day of the week register increases at midnight, and the corresponding values for the days of the week can be defined by the user, but must be continuous. (For example, if 1 represents Sunday, then 2 represents Monday, etc.) Illegal time and date inputs result in undefined operations. When reading and writing clock and date registers, the second (user) cache is used to prevent errors during internal register updates. When reading clock and date registers, synchronize the rising edge user cache with internal registers in CE. Whenever the second register is written, the countdown circuit is reset. Write transmission occurs at the falling edge of CE to avoid flipping issues. Once the countdown circuit is reset, the remaining time and date registers must be written within one second. DS1302Z can operate in two modes: 12 hour mode and 24-hour mode. Bit 7 of the hour register is defined as the hour mode selection bit. When it is high, it is in the 12 hour mode. In the 12 hour mode, bit 5 is the morning/afternoon bit and the high level is in the afternoon; In 24-hour mode, position 5 is the second hour position (20:00-23:00). Once there is a change on 12/24, the hourly data must be reinitialized.

## Clock pause flag

Bit 7 of the second register is defined as the clock pause flag. When it is set to 1, the clock oscillator pauses and DS1302Z enters a low-power standby mode with a leakage current of less than 100nA. When this is set to 0, the clock starts and the initial power on state is undefined.

## Write protection position

Bit 7 of the control register is a write protect bit, and the first 7 bits (bits 0 to 6) are forced to be 0 and always read as 0 during reading. Before any write operation to the clock or RAM, bit 7 must be 0. When it is high, the write protection bit prohibits any register write operations, and the initial power on state is undefined. Therefore, the WP bit should be cleared before attempting to write the device.

## Trickle charging register

This register controls the trickle charging characteristics of DS1302Z, and the simplified structural diagram in Figure 5 shows the basic components of the trickle charger. The trickle charging selection (TCS) bit (bit 4 to bit 7) controls the selection of the trickle charger. To prevent accidental activation, only the 1010 mode can enable the trickle charger, and all other modes will disable the trickle charger. When DS1302Z is powered on, the trickle charger is disabled, and the diode selection (DS) bit (bit 2 and bit 3) selects whether one or two diodes are connected between VCC2 and VCC1. If DS is 01, one diode, 10 is 2 diodes. If DS is 00 or 11, regardless of TCS, the trickle charger is prohibited; RS bit (bit 0 and bit 1) selects the resistor connected between VCC2 and VCC1. Table 2 shows the selection of resistors and diodes for RS and DS.

| TCS BIT7 | TCS BIT6 | TCS BIT5 | TCS BIT4 | TCS BIT3 | TCS BIT2 | TCS BIT1 | TCS BIT0 | FUNCTION |
|---|---|---|---|---|---|---|---|---|
| × | × | × | × | × | × | 0 | 0 | Disabled |
| × | × | × | × | 0 | 0 | × | × | Disabled |
| × | × | × | × | 1 | 1 | × | × | Disabled |
| 1 | 0 | 1 | 0 | 0 | 1 | 0 | 1 | 1 Diode, 2kΩ |
| 1 | 0 | 1 | 0 | 0 | 1 | 1 | 0 | 1 Diode, 4kΩ |
| 1 | 0 | 1 | 0 | 0 | 1 | 1 | 1 | 1 Diode, 8kΩ |
| 1 | 0 | 1 | 0 | 1 | 0 | 0 | 1 | 2 Diode, 2kΩ |
| 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 2 Diode, 4kΩ |
| 1 | 0 | 1 | 0 | 1 | 0 | 1 | 1 | 2 Diode, 8kΩ |
| 0 | 1 | 0 | 1 | 1 | 1 | 0 | 0 | Initial power-on state |

Table 2 Selection of trickle charging resistors and diodes

The selection of resistors and diodes is determined by the user based on the maximum current required for charging the battery or supercapacitor. The maximum charging current can be calculated as shown in the following example.
Assuming a 5V system power supply is applied to VCC2 and a supercapacitor is connected to VCC1.
Assuming that the trickle charger is enabled and VCC2 and VCC1 have a diode and resistor R1, the maximum current IMAX is calculated as follows:
IMAX=(5.0V - diode voltage drop)/R1 ≈ (5.0V-0.7V)/2k Ω≈ 2.2mA
When charging a supercapacitor, the voltage drop between VCC2 and VCC1 increases, resulting in an increase in charging current.

### Clock/Calendar Pulse Train Mode

The clock/calendar command byte specifies the burst mode operation. In this mode, the first eight clock/calendar registers must read and write continuously from bit 0 of address 0 (see Table 3). If the write protection position is high when specified as the write clock/calendar burst mode, none of the eight clock/calendar registers (including control registers) will transfer data. The trickle charger is not readable or writable in burst mode. At the beginning of the clock pulse train reading, the current time is transferred to another set of memory; When the clock continues to run, it will read back time information from these second registers. This eliminates the need for updating the main register and re reading the register in case of a read.

### RAM

Static RAM is addressed continuously in the RAM address space with 31x8 bytes.

### RAM pulse train mode

The RAM command byte defines the burst mode operation, in which the 31RAM register can continuously read and write from bit 0 of address O (see Table 3).

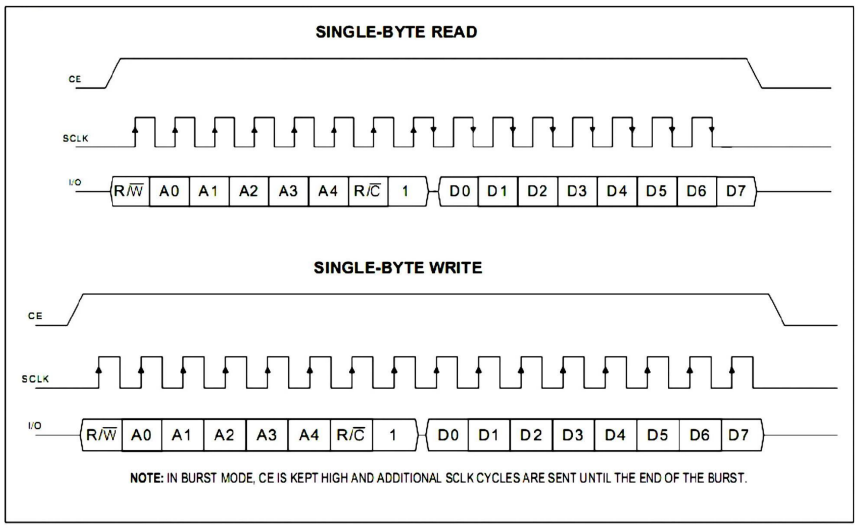
### Register Summary

Table 3 shows a summary of register data formats.

### Crystal oscillator selection

A 32.768kHz crystal oscillator can be directly connected to DS1302Z through pins 2 and 3 (X1, X2). To improve the accuracy of travel time, a set of 10pF-33pF load compensation capacitors should be installed externally at the crystal oscillator end, and the specific capacitance value depends on the application layout and crystal oscillator.

## ◆ Figure 4 Data Transmission Summary



## ◆ Table 3 Register Address/Definition

**RTC**

| READ | WRITE | TCS BIT7 | TCS BIT6 | TCS BIT5 | TCS BIT4 | TCS BIT3 | TCS BIT2 | TCS BIT1 | TCS BIT0 | FUNCTION |
|---|---|---|---|---|---|---|---|---|---|---|
| 81h | 80h | CH | 10 Seconds | | | Seconds | | | | 00-59 |
| 83h | 82h | | 10 Minutes | | | Minutes | | | | 00-59 |
| 85h | 84h | 12/<u>24</u> | 0 | 10<br><u>AM</u>/PM | Hour | Hour | | | | 1-12/-23 |
| 87h | 86h | 0 | 0 | 10 Date | | Date | | | | 1-31 |
| 89h | 88h | 0 | 0 | 0 | 10 Month | Month | | | | 1-12 |
| 8Bh | 8Ah | 0 | 0 | 0 | 0 | 0 | Day | | | 1-7 |
| 8Dh | 8Ch | 10 YEAR | | | | Year | | | | 00-99 |
| 8Fh | 8Eh | WP | 0 | 0 | 0 | 0 | 0 | 0 | 0 | _ |
| 91h | 90h | TCS | TCS | TCS | TCS | DS | DS | RS | RS | _ |

**Clock pulse train**

| | |
|---|---|
| BFh | BEh |

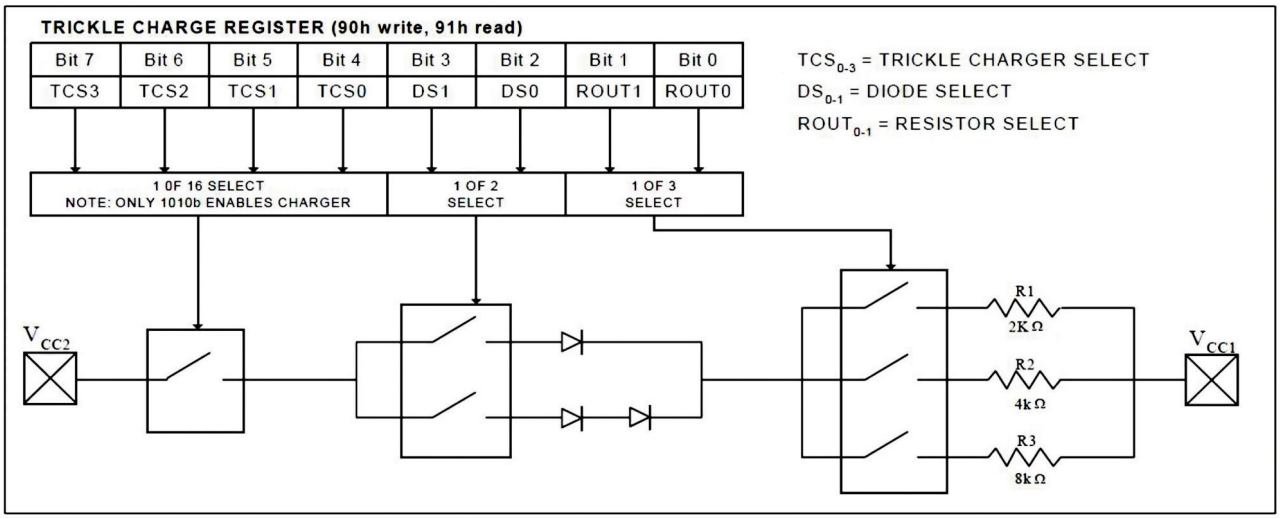
**RAM**

| | | | |
|---|---|---|---|
| C1h | C0h | | 00-FFh |
| C3h | C2h | | 00-FFh |
| C5h | C4h | | 00-FFh |
| | | | |
| FDh | FCh | | 00-FFh |

**RAM pulse train**

| | |
|---|---|
| FFh | FEh |

## ◆ Figure 5 Programmable trickle charger




## ◆ Limiting parameters

| Parameter | Identification | value |
|---|---|---|
| The voltage range between any pin and ground | | -0.5~7.0V |
| Working temperature range, civilian grade | Tj_Min/Max | -40~85℃ |
| Storage temperature range | Ta_Min/Max | -55^125℃ |
| Lead temperature (welding, 10s) | T_lead | 260℃ |

Exceeding the stress listed in the absolute maximum rated value table will cause permanent damage to the device. These are only rated values and do not include functional operations that are in or outside the operating range specified in the manual. Long term exposure to the absolute maximum rated value will affect the reliability of the device.

## ◆ Recommended DC working conditions(TA=0 ℃ -+80 ℃) (Note 1)

| Parameter | Symbol | | Status | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|---|
| power supply voltage VCC1,VCC2 | VCC1 VCC2 | | (note2，10) | 2.0 | 3.3 | 5.5 | V |
| Logic 1 Input | VIH | | (note2) | 2.0 | | VCC+0.3 | V |
| Logic 0 input | VIL | VCC=2.0V | (note2) | -0.3 | | +0.3 | V |
| | | VCC=5V | | -0.3 | | +0.8 | |

## ◆ DC electrical characteristics(TA=0 ℃ -+80 ℃) (Note 1)

| Parameter | Symbol | | Test conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|---|
| Input leakage current | ILI | | ( note5，13) | | | 500 | uA |
| I/0 leakage current | ILO | | (note5，13) | | | 500 | |
| Logic 1 output (IOH=-0.4mA) | VOH | VCC=2.0V | (note2) | 1.6 | | | V |
| Logic 1 output (IOH=-1.0mA) | | VCC=5.0V | | 2.4 | | | V |
| Logic0 output (IOH=+1.5mA) | VOL | VCC=2.0V | (note2) | | | 0.4 | V |
| Logic0 output (IOH=+0.4mA) | | VCC=5.0V | | | | 0.4 | V |
| Dynamic power supply current (oscillator enabled) | ICC1A | VCC=2.0V | CH=0 (note4，11) | | | 0.4 | mA |
| | | VCC=5.0V | | | | 1.2 | |
| Chronoamperometry (oscillator enabled) | ICC1T | VCC=2.0V | CH=0 (note3，11，13) | | | 0.3 | uA |
| | | VCC=5.0V | | | | 1 | |
| quiescent current (Oscillators prohibited) | ICC1S | VCC=2.0V | CH=1 (note9，11，13) | | | 100 | nA |
| | | VCC=5.0V | | | | 100 | |
| | | IND | | | | 200 | |
| Dynamic power supply current (oscillator enabled)) | ICC2A | VCC=2.0V | CH=0 (note4，12) | | | 0.425 | mA |
| | | VCC=5.0V | | | | 1.28 | |
| Chronoamperometry (oscillator enable)) | ICC2T | VCC=2.0V | CH=0 (note3，12) | | | 25.3 | uA |
| | | VCC=5.0V | | | | 81 | |
| quiescent current (Oscillators prohibited) | ICC2S | VCC=2.0V | CH=1 (note9，12) | | | 25 | uA |
| | | VCC=5.0V | | | | 80 | |
| Trickle charging resistor | R1 | | | | 2 | | kΩ |
| | R2 | | | | 4 | | |
| | R3 | | | | 8 | | |
| Voltage drop of trickle charging diode | VTG | | | | 0.7 | | V |

## ◆ AC electrical characteristics(TA=0 ℃ -+80 ℃) (Note 1)

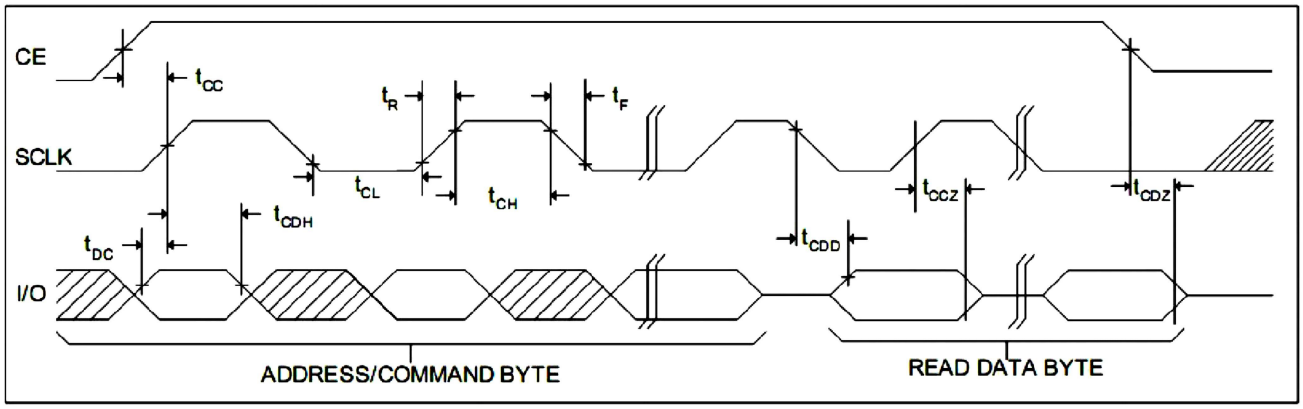
| Parameter | Symbol | | Test conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|---|
| Data to CLK Set up | TDC | VCC=2.0V | (note6) | 200 | | | ns |
| | | VCC=5.0V | | 50 | | | |
| CLK to Data Hold | TCDH | VCC=2.0V | (note6) | 280 | | | ns |
| | | VCC=5.0V | | 70 | | | |
| CLK to Data Delay | TCDD | VCC=2.0V | (note6) | | | 800 | ns |
| | | VCC=5.0V | | | | 200 | |
| CLK Low Time | TCL | VCC=2.0V | (note6, 7, 8) | 1000 | | | ns |
| | | VCC=5.0V | | 250 | | | |
| CLK High Time | TCH | VCC=2.0V | (note6) | 1000 | | | ns |
| | | VCC=5.0V | | 250 | | | |
| CLK Frequency | TCLK | VCC=5.0V | (note6) | | | 0.5 | MHz |
| | | IND | | DC | | 2.0 | |
| CLK Rise and Fall | TR | VCC=2.0V | | | | 2000 | ns |
| | TF | VCC=5.0V | | | | 500 | |
| CE to CLK Setup | TCC | VCC=2.0V | (note6) | 4 | | | ns |
| | | VCC=5.0V | | 1 | | | |
| CLK to CE Hold | TCCH | VCC=2.0V | (note6) | 240 | | | ns |
| | | VCC=5.0V | | 60 | | | |
| CE Inactive Time | TCWH | VCC=2.0V | (note6) | 4 | | | ns |
| | | VCC=5.0V | | 1 | | | |
| CE to I/0 High Impedance | TCDZ | VCC=2.0V | (note6) | | | 280 | ns |
| | | VCC=5.0V | | | | 70 | |
| SCLK to I/0 High Impedance | TCCZ | VCC=2.0V | (note6) | | | 280 | ns |
| | | VCC=5.0V | | | | 70 | |

Note 1: The limit of -20 ℃ is designed to ensure that production testing has not been conducted
Note 2: All voltages are referenced to ground
Note 3: ICCIT and ICC2T are opened by IO, and CE and SCLK are specified as 0
Note 4: ICC1A and ICC2A are opened by VO, CE is specified high, SCLK=2MHz when VCC=5V; SCLK=500KHz,VCC=2.0V.
Note 5: CE, SCLK, and I/O all have 40k Ω pull-down resistors connected to ground
Note 6: When measured at VIH=2.0V or VIL=0.8V, the maximum rise and fall time is 10ns
Note 7: Measured at VOH=2.4V or VOL=0.4V
Note 8: Load capacitance=50pF
Note 9: ICC1S and ICC2S are specified by CE, VO, SCLK
Note 10: VCC=VCC2, when VCC2>VCC1+0.2V; VCC=VCC1, When VCC1>VCC2
Note 11: VCC2=0V
Note 12: VCC1=0V
Note 13: When the typical value is+25 ℃

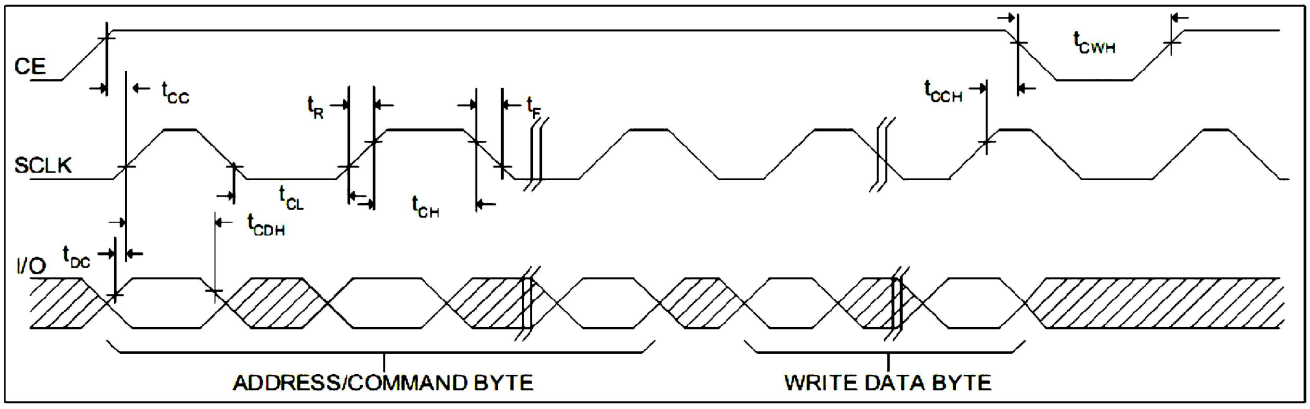
## ◆ Capacitor (TA=+25 ℃)

| Parameter | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| Input capacitor | CI | | 10 | | pF |
| I/O capacitor | CI/O | | 15 | | pF |

## ◆ Figure 6 Timing diagram: Read data transmission

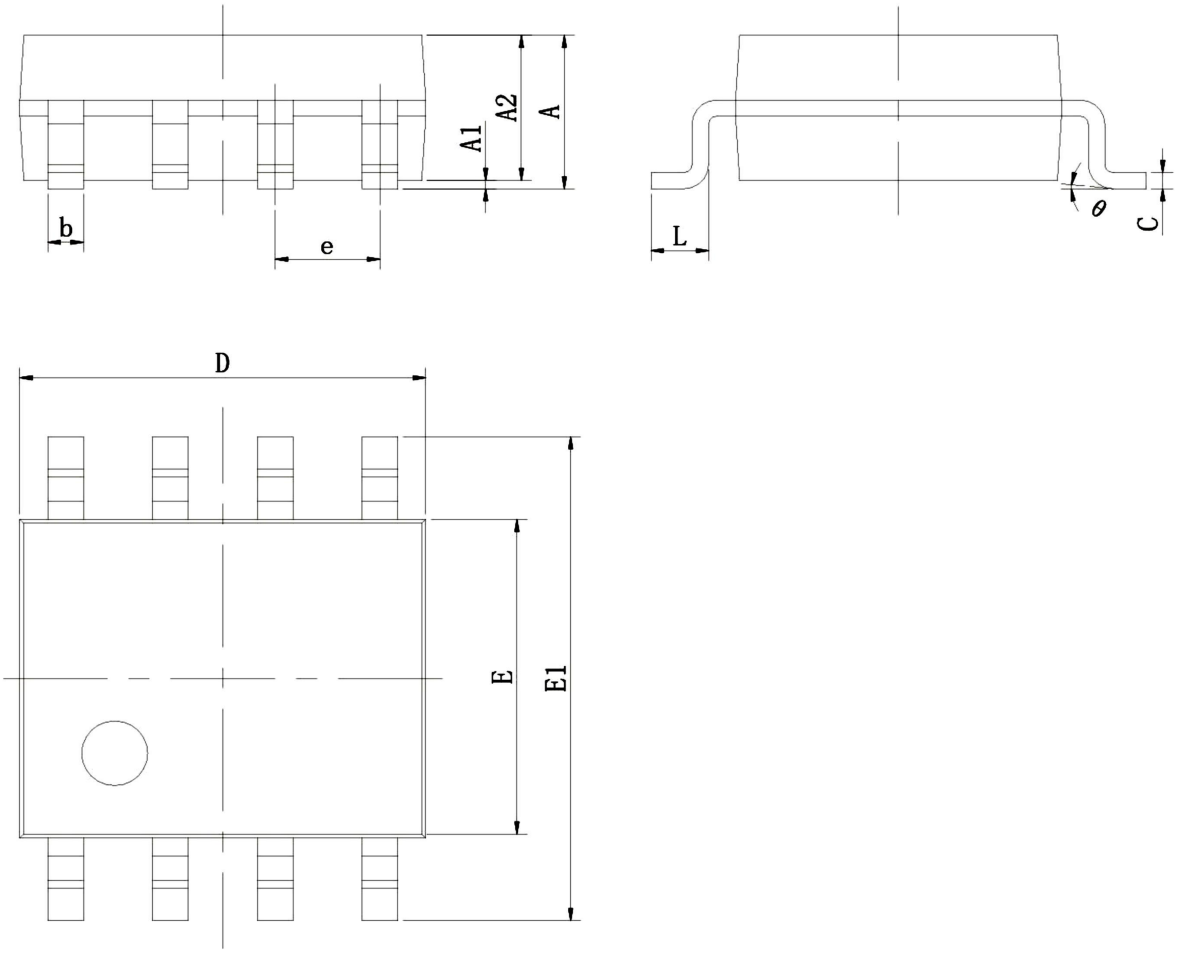



## ◆ Figure 7 Timing diagram: Writing data transmission



## ◆ Package size diagram

**SOP8**




| Symbol | Dimensions In Millimeters | | Dimensions In Inches | |
|---|---|---|---|---|
| | Min | Max | Min | Max |
| A | 1.350 | 1.800 | 0.053 | 0.071 |
| A1 | 0.010 | 0.250 | 0.003 | 0.010 |
| A2 | 1.250 | 1.550 | 0.053 | 0.061 |
| b | 0.300 | 0.510 | 0.011 | 0.020 |
| c | 0.170 | 0.250 | 0.006 | 0.010 |
| D | 4.700 | 5.100 | 0.185 | 0.201 |
| E | 3.800 | 4.000 | 0.150 | 0.157 |
| E1 | 5.800 | 6.300 | 0.228 | 0.244 |
| e | 1.270 (BSC) | | 0.050 (BSC) | |
| L | 0.400 | 1.270 | 0.016 | 0.050 |
| θ | 0° | 8° | 0° | 8° |

## ◆ Attention

- AOTE implements dynamic technical updates. Specifications are subject to change. Refer to the official website for the latest version.
- Users must strictly adhere to specified conditions. Failures caused by misuse (overload, high temperature, incompatible circuits) are excluded from warranty.
- Contact technical support for customized validation in critical applications (medical devices, industrial control).
- This document is valid until December 31, 2026. Updates will be notified on the official website.
- For further clarification on technical specifications or application solutions, please contact us through official channels: