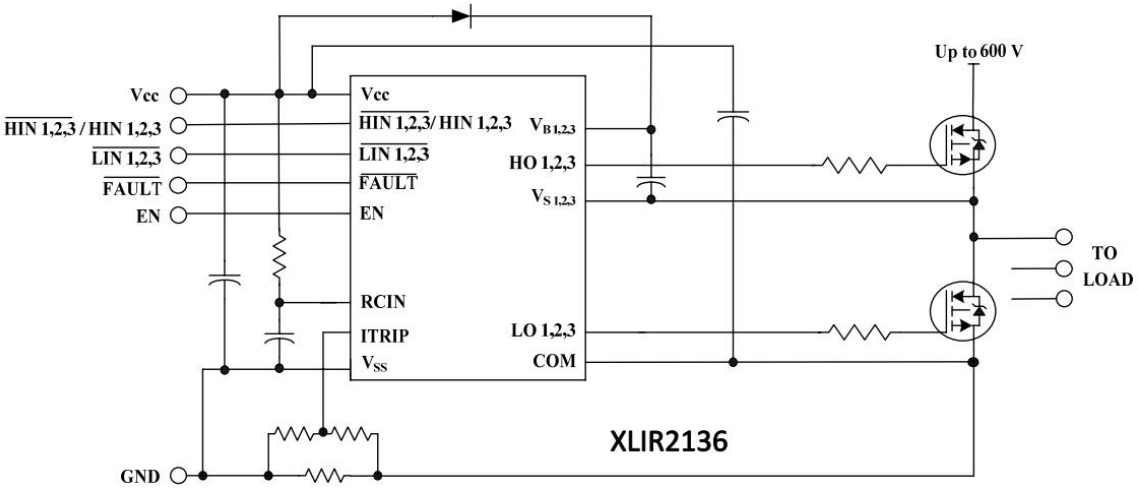
1. DESCRIPTION

The XLIR2136 are high voltage, high speed power MOSFET and IGBT drivers with three independent high and low side referenced output channels for 3-phase applications. Proprietary HVIC technology enables ruggedized monolithic construction. Logic inputs are compatible with CMOS or LSTTL outputs, down to 3.3 V logic. A current trip function which terminates all six outputs can be derived from an external current sense resistor. An enable function is available to terminate all six outputs simultaneously. An open-drain FAULT signal is provided to indicate that an overcurrent or undervoltage shutdown has occurred. Overcurrent fault conditions are cleared automatically after a delay programmed externally via an RC network connected to the RCIN input. The output drivers feature a high pulse current buffer stage designed for minimum driver cross-conduction. Propagation delays are matched to simplify use in high frequency applications. The floating channels can be used to drive N-channel power MOSFETs or IGBTs in the high side configuration which operates up to 600 **V.**

2. FEATURES

- Floating channel designed for bootstrap operation
- Fully operational to +600 V
- Tolerant to negative transient voltage, dV/dt immune
- Undervoltage lockout for all channels
- Over-current shutdown turns off all six drivers
- Independent 3 half-bridge drivers
- Matched propagation delay for all channels
- Cross-conduction prevention logic
- Low side output out of phase with inputs. High side outputs out of phase
- 3.3 V logic compatible
- Lower di/dt gate drive for better noise immunity
- Externally programmable delay for automatic fault clear
- All parts are LEAD-FREE

3. TYPICAL CONNECTION



(Refer to LeadAssignments for correctpin configuration). Thisdiagram shows electricalconnections only. Pleaserefer to our ApplicationNotes and Design Tips forproper circuit boardlayout.

4. ABSOLUTE MAXIMUM RATINGS

Absolute Maximum Ratings indicate sustained limits beyond which damage to the device may occur. All voltage parameters are absolute voltages referenced to COM. The thermal resistance and power dissipation ratings are measured under board mounted and still air conditions.

Symbol	Definition		Min	Max	Units
V_S	High side offset voltage		$V_{B\,1,2,3}$ - 25	$V_{B\,1,2,3}$ + 0.3	V
V_B	High side floating supply voltage		-0.3	625	
V_{HO}	High side floating output voltage		$V_{S\,1,2,3}$- 0.3	$V_{B\,1,2,3}$ + 0.3	
V_{CC}	Low side and logic fixed supply voltage		-0.3	25	
V_{SS}	Logic ground		V_{CC} - 25	V_{CC} + 0.3	
$V_{LO1,2,3}$	Low side output voltage		-0.3	V_{CC} + 0.3	
V_{IN}	Input voltage LIN, HIN, ITRIP, EN		V_{SS} -0.3	Lower of (V_{SS} + 15) or V_{CC} + 0.3)	
V_{RCIN}	RCIN input voltage		V_{SS} -0.3	V_{CC} + 0.3	
V_{FLT}	$\overline{\text{FAULT}}$ output voltage		V_{SS} -0.3	V_{CC} + 0.3	
dV/dt	Allowable offset voltage slew rate		—	50	V/ns
P_D	Package power dissipation @ $T_A \leq$ +25 °C	(28 lead DIP)	—	1.5	W
		(28 lead SOP)	—	1.6	
Rth_{JA}	Thermal resistance, junction to ambient	(28 lead DIP)	—	83	°C/W
		(28 lead SOP)	—	78	
T_J	Junction temperature		—	150	°C
T_S	Storage temperature		-55	150	
T_L	Lead temperature (soldering, 10 seconds)		—	300	

5. RECOMMENDED OPERATING CONDITIONS

The input/output logic-timing diagram is shown in Fig. 1. For proper operation the device should be used within the recommended conditions. All voltage parameters are absolute referenced to COM. The V_S offset ratings are tested with all supplies biased at a 15 V differential.

Symbol	Definition	Min	Max	Units
$V_{B1,2,3}$	High side floating supply voltage	$V_{S1,2,3}$ +10	$V_{S1,2,3}$ + 20	V
$V_{S\,1,2,3}$	High side floating supply offset voltage	Note 1	600	
$V_{HO\,1,2,3}$	High side output voltage	$V_{S1,2,3}$	$V_{B1,2,3}$	
$V_{LO1,2,3}$	Low side output voltage	0	V_{CC}	
V_{CC}	Low side and logic fixed supply voltage	10	20	
V_{SS}	Logic ground	-5	5	
V_{FLT}	$\overline{\text{FAULT}}$ output voltage	V_{SS}	V_{CC}	
V_{RCIN}	RCIN input voltage	V_{SS}	V_{CC}	

Note 1: Logic operational for VS of (COM - 5 V) to (COM + 600 V). Logic state held for VS of (COM - 5 V) to (COM – VBS).
Note 2: All input pins and the ITRIP and EN pins are internally clamped with a 5.2 V zener diode.

RECOMMENDED OPERATING CONDITIONS - (Continued)

Absolute Maximum Ratings indicate sustained limits beyond which damage to the device may occur. All voltage parameters are absolute voltages referenced to COM. The thermal resistance and power dissipation ratings are measured under board mounted and still air conditions.

Symbol	Definition	Min	Max	Units
V_{ITRIP}	ITRIP input voltage	V_{SS}	V_{SS} + 5	V
V_{IN}	Logic input voltage $\overline{LIN}$, $\overline{HIN}$	V_{SS}	V_{SS} + 5	
T_A	Ambient temperature	-40	105	℃

6. STATIC ELECTRICAL CHARACTERISTICS

V_{BIAS} (V_{CC},$V_{BS1,2,3}$) = 15 V unless otherwise specified. The V_{IN}, V_{TH}, and I_{IN} parameters are referenced to V_{SS} and are applicable to all six channels ($\overline{HIN1,2,3}$ and $\overline{LIN1,2,3}$). The V_O and I_O parameters are referenced to COM and $V_{S1,2,3}$ and are applicable to the respective output leads: HO1,2,3 and LO1,2,3.

Symbol	Definition	Min	Typ	Max	Units	Test Conditions
V_{IH}	Logic 0 input voltage $\overline{LIN1,2,3}$, $\overline{HIN1,2,3}$	3.0	—	—	V	
	Logic 0 input voltage $\overline{LIN1,2,3}$, $\overline{HIN1,2,3}$	2.5	—	—		
V_{IL}	Logic 1 input Voltage $\overline{LIN1,2,3}$, $\overline{HIN1,2,3}$	—	—	0.8		
	Logic 0 input voltage $\overline{LIN1,2,3}$, $\overline{HIN1,2,3}$					
$V_{EN,TH+}$	Enable positive going threshold	—	—	3		
$V_{EN,TH-}$	Enable negative going threshold	0.8	—	—		
$V_{IT,TH+}$	ITRIP positive going threshold	0.37	0.46	0.55		
$V_{IT,HYS}$	ITRIP input hysteresis	—	0.07	—		
$V_{RCIN,TH+}$	RCIN positive going threshold	—	8	—		
$V_{RCIN,HYS}$	RCIN input hysteresis	—	3	—		
V_{OH}	High level output voltage, V_{BIAS} - V_O	—	0.9	1.4		I_O = 20 mA
V_{OL}	Low level output voltage, V_O	—	0.4	0.6		
V_{CCUV+} V_{BSUV+}	V_{CC} and V_{BS} supply undervoltage positive going threshold	8.0	8.9	9.8		

STATIC ELECTRICAL CHARACTERISTICS - (Continued)

V_{BIAS} (V_{CC},$V_{BS1,2,3}$) = 15 V unless otherwise specified. The V_{IN}, V_{TH}, and I_{IN} parameters are referenced to V_{SS} and are applicable to all six channels ($\overline{HIN1,2,3}$ and $\overline{LIN1,2,3}$). The V_O and I_O parameters are referenced to COM and $V_{S1,2,3}$ and are applicable to the respective output leads: HO1,2,3 and LO1,2,3.

Symbol	Definition	Min	Typ	Max	Units	Test Conditions
V_{CCUV-} V_{BSUV-}	V_{CC} and V_{BS} supply undervoltage negative going threshold	7.4	8.2	9.0	V	
V_{CCUVH} V_{BSUVH}	V_{CC} and V_{BS} supply undervoltage lockout hysteresis	0.3	0.7	—		
I_{LK}	Offset supply leakage current	—	—	50	µA	$V_{B1,2,3}$ = $V_{S1,2,3}$ = 600 V
I_{QBS}	Quiescent V_{BS} supply current	—	70	120		V_{IN} = 0 V or 5 V
I_{QCC}	Quiescent V_{CC} supply current	—	1.6	2.3	mA	
$V_{IN,CLAMP}$	Input clamp voltage (HIN, LIN, ITRIP and EN)	4.9	5.2	5.5	V	I_{IN} =100 µA
I_{LIN+}	Input bias current (LOUT = HI)	—	200	300	µA	V_{LIN} = 5 V
I_{LIN-}	Input bias current (LOUT = LO)	—	100	220		V_{LIN} = 0 V
I_{HIN+}	Input bias current (HOUT = HI)	—	200	300		V_{HIN} = 5 V
I_{HIN-}	Input bias current (HOUT = LO)	—	100	220		V_{HIN} = 0 V
I_{ITRIP+}	"High" ITRIP input bias current	—	30	100		V_{ITRIP} = 5 V
I_{ITRIP-}	"Low" ITRIP input bias current	—	0	1		V_{ITRIP} = 0 V
I_{EN+}	"High" ENABLE input bias current	—	30	100		V_{ENABLE} = 5 V
I_{EN-}	"Low" ENABLE input bias current	—	0	1		V_{ENABLE} =0 V
I_{RCIN}	RCIN input bias current	—	0	1		Vrcin= 0 V or 15 V
I_{O+}	Output high short circuit pulsed current	120	200	—	mA	V_O =0 V, PW ≤ 10 µs
I_{O-}	Output low short circuit pulsed current	250	350	—		V_O =15 V, PW ≤ 10 µs
R_{on_RCIN}	RCIN low on resistance	—	50	100	Ω	
R_{on_FAULT}	FAULT low on resistance	—	50	100		

7. DYNAMIC ELECTRICAL CHARACTERISTICS

V_{CC} = V_{BS} = V_{BIAS} = 15 V, $V_{S1,2,3}$ = V_{SS} = COM, T_A = 25 °C and CL = 1000 pF unless otherwise specified.

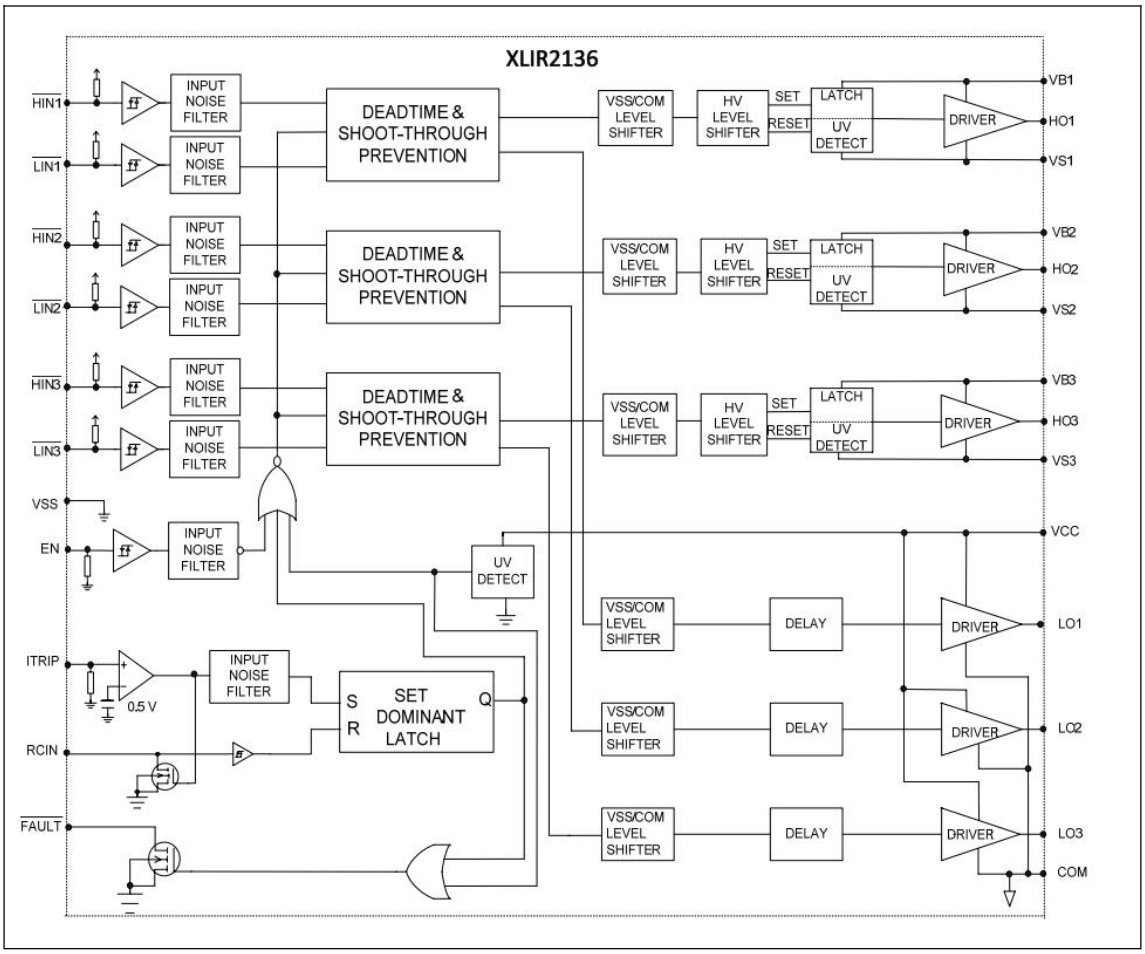
Symbol	Definition	Min	Typ	Max	Units	Test Conditions
t_{on}	Turn-on propagation delay	300	425	550	ns	V_{IN} = 0 V & 5 V
t_{off}	Turn-off propagation delay	250	400	550		
t_r	Turn-on rise time	—	125	190		
t_f	Turn-off fall time	—	50	75		
t_{EN}	ENABLE low to output shutdown propagation delay	300	450	600		V_{IN}, V_{EN} = 0 V or 5 V
t_{ITRIP}	ITRIP to output shutdown propagation delay	500	750	1000		VITRIP = 5 V
t_{bl}	ITRIP blanking time	100	150	—		V_{IN} = 0 V or 5 V V_{ITRIP} = 5 V
t_{FLT}	ITRIP to $\overline{\text{FAULT}}$ propagation delay	400	600	800		
t_{FILIN}	Input filter time (HIN, LIN)	100	200	—		V_{IN} = 0 V & 5 V
t_{FLTCLR}	FAULT clear time RCIN: R = 2 MΩ, C = 1 nF	1.3	1.65	2	ms	V_{IN} = 0 V or 5 V V_{ITRIP} = 0 V
DT	Deadtime	220	290	360	ns	V_{IN} = 0 V & 5 V
MT	Matching delay ON and OFF	—	40	75		External dead time >400 ns
MDT	Matching delay, max (t_{on} , t_{off}) – min (t_{on} , t_{off}), (t_{on} , t_{off} are applicable to all 3 channels)	—	25	70		
PM	Output pulse width matching (pwin-pwout) (Fig.2)	—	40	75		

Note: For high side PWM, HIN pulse width must be ≥ 1 µs.

VCC	VBS	ITRIP	ENABLE	FAULT	LO1,2,3	HO1,2,3
<UVCC	X	X	X	0 (note 1)	0	0
15 V	<UVBS	0 V	5 V	high imp	LIN1,2,3	0
15 V	15 V	0 V	5 V	high imp	LIN1,2,3	HIN1,2,3
15 V	15 V	>VITRIP	5 V	0 (note 2)	0	0
15 V	15 V	0 V	0 V	high imp	0	0

Note 1: A shoot-through prevention logic prevents LO1,2,3 and HO1,2,3 for each channel from turning on simultaneously.
Note 2: UVCC is not latched, when V_{CC} > UV_{CC}, FAULT returns to high impedance.
Note 3: When ITRIP < V_{ITRIP} , FAULT returns to high-impedance after RCIN pin becomes greater than 8 V (@ V_{CC} = 15 V).

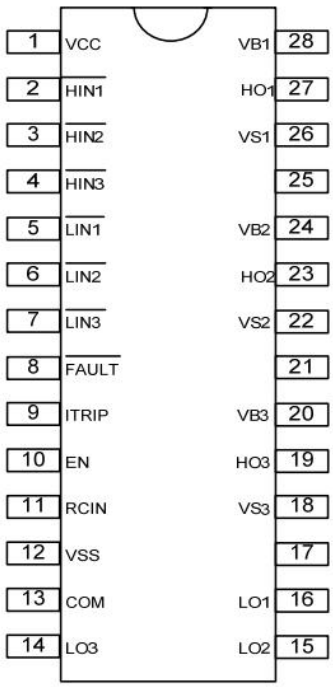
8. FUNCTIONAL BLOCK DIAGRAM



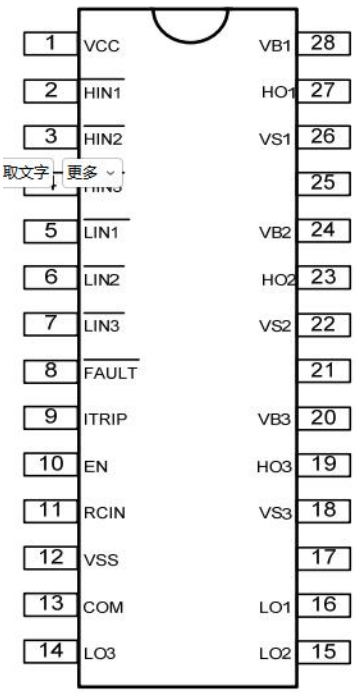
Symbol	Description
V_{CC}	Low side and logic fixed supply
V_{SS}	Logic ground
$\overline{HIN1,2,3}$	Logic inputs for high side gate driver outputs (HO1,2,3), out of phase
$\overline{LIN1,2,3}$	Logic input for low side gate driver outputs (LO1,2,3), out of phase
FAULT	Indicates over-current (ITRIP) or low-side undervoltage lockout has occurred. Negative logic, open- drain output
EN	Logic input to enable I/O functionality. I/O logic functions when ENABLE is high (i.e., positive logic) No effect on FAULT and not latched
ITRIP	Analog input for overcurrent shutdown. When active, ITRIP shuts down outputs and activates FAULT and RCIN low. When ITRIP becomes inactive, FAULT stays active low for an externally set time T_{FLTCLR}, then automatically becomes inactive (open-drain high impedance).
RCIN	External RC network input used to define FAULT CLEAR delay, T_{FLTCLR}, approximately equal to R*C. When RCIN>8 V, the FAULT pin goes back into open-drain high-impedance
COM	Low side gate drivers return
$V_{B1,2,3}$	High side floating supply
HO1,2,3	High side gate driver outputs
$V_{S1,2,3}$	High voltage floating supply return
LO1,2,3	Low side gate driver outputs

Note: All input pins and the ITRIP pin are internally clamped with a 5.2 V zener diode.

9. LEAD ASSIGNMENTS



28 Lead DIP



28 Lead SOP

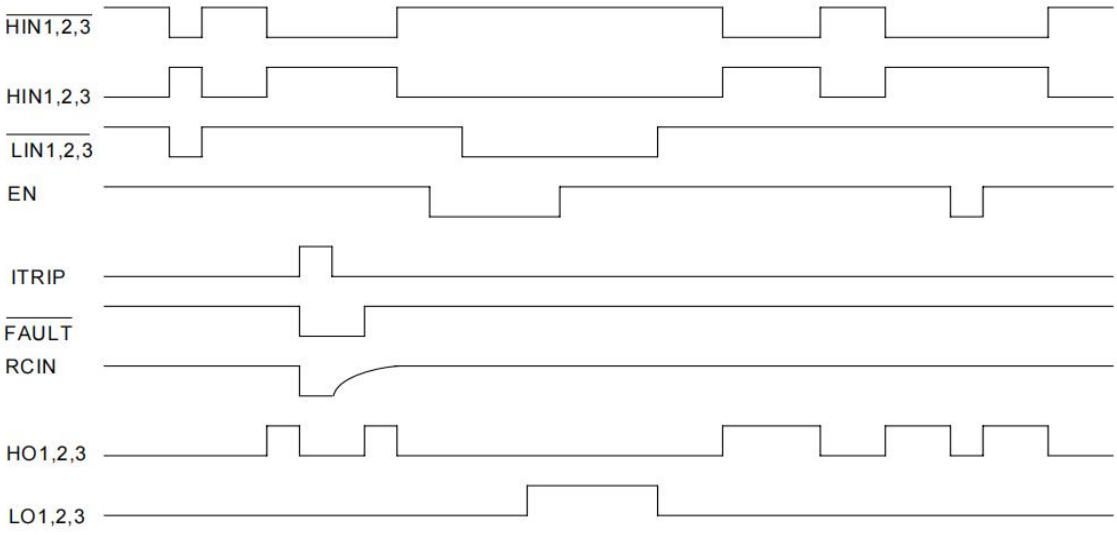


Fig. 1. Input/Output Timing Diagram

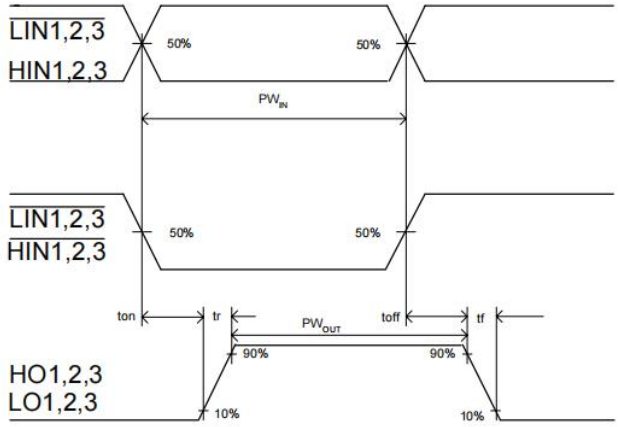


Fig. 2. Switching Time Waveforms

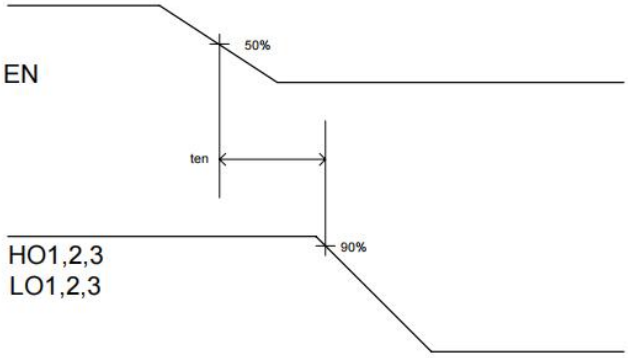


Fig. 3. Output Enable Timing Waveform

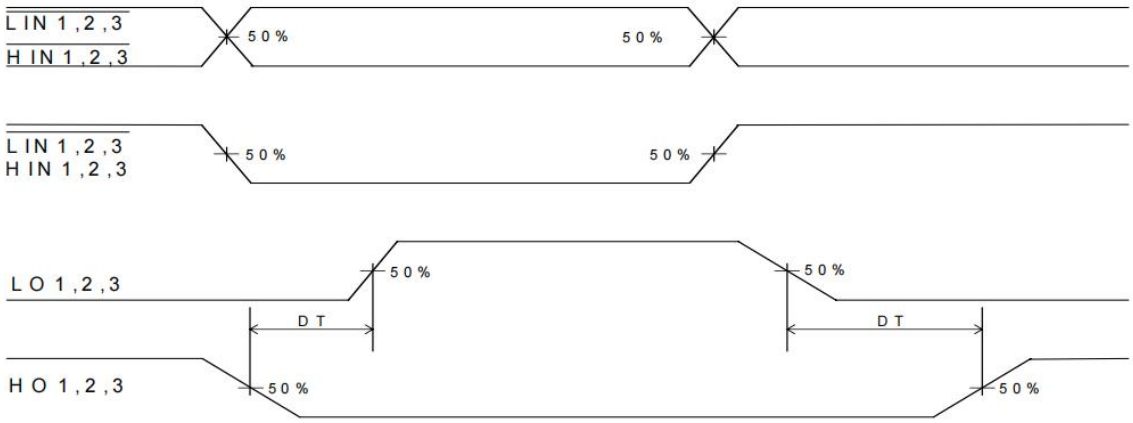


Fig. 4. Internal Deadtime Timing Waveforms

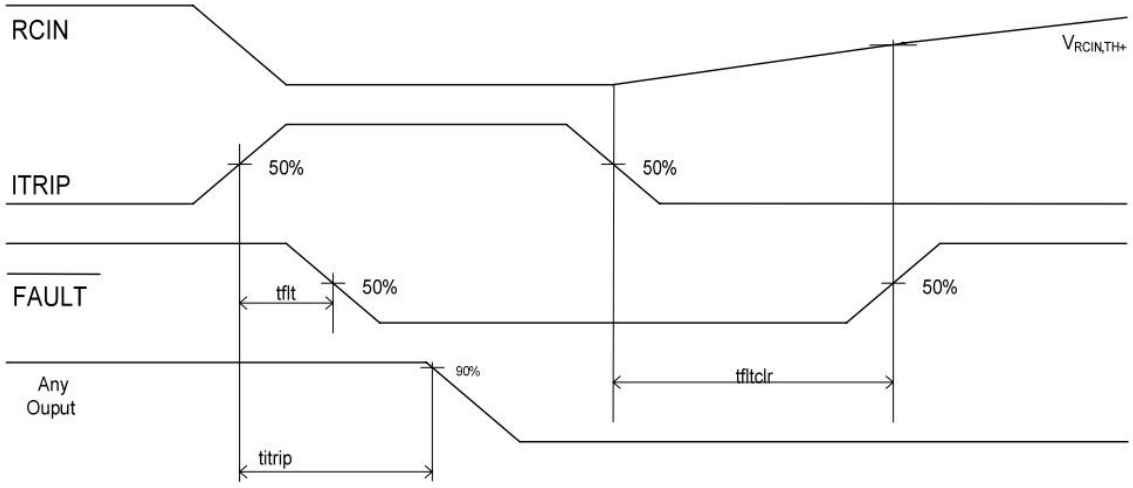


Fig. 5. ITRIP/RCIN Timing Waveforms

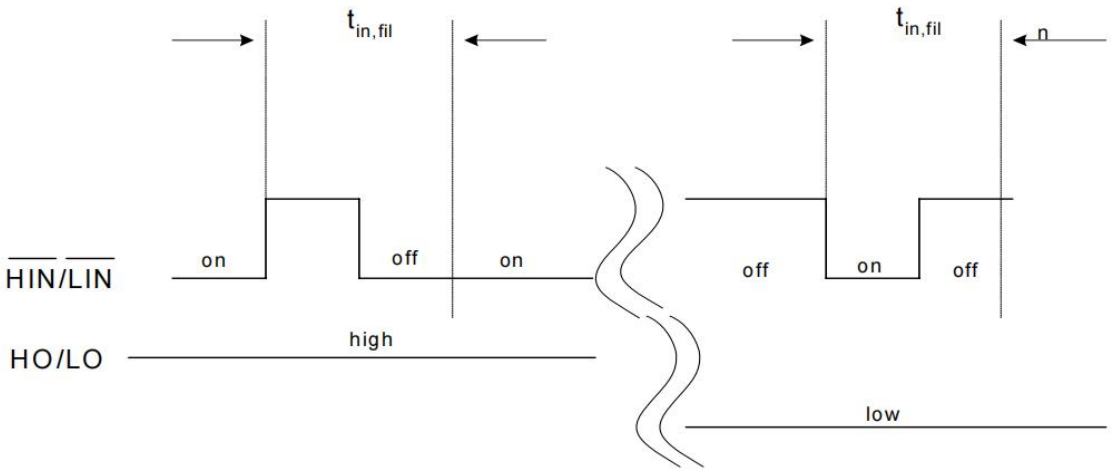


Fig. 6. Input Filter Function

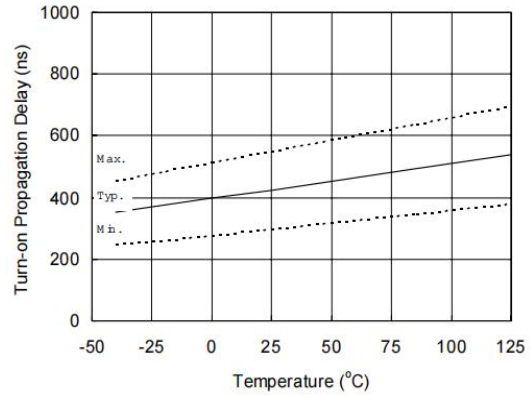


Figure 6A. Turn-on Propagation Delay vs. Temperature

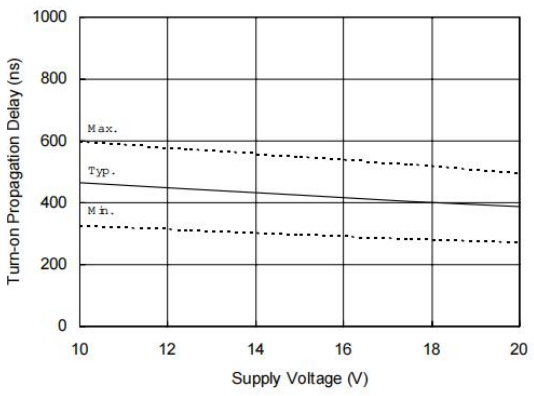


Figure 6B. Turn-on Propagation Delay vs. Supply Voltage

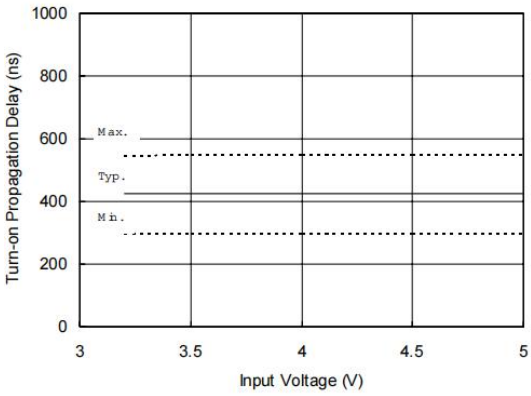


Figure 6C. Turn-on Propagation Delay vs. Input Voltage

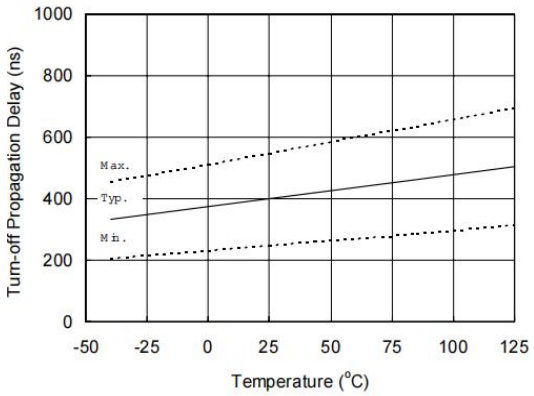


Figure 7A. Turn-off Propagation Delay vs. Temperature

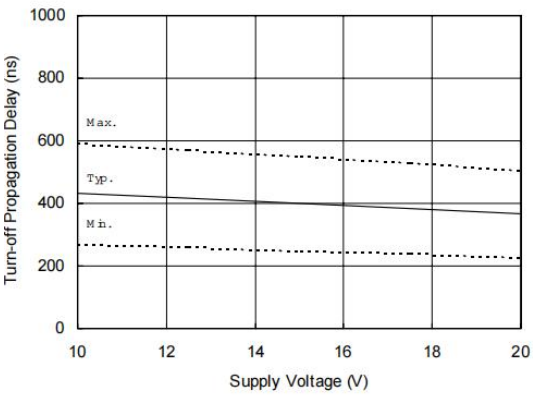


Figure 7B. Turn-off Propagation Delay vs. Supply Voltage

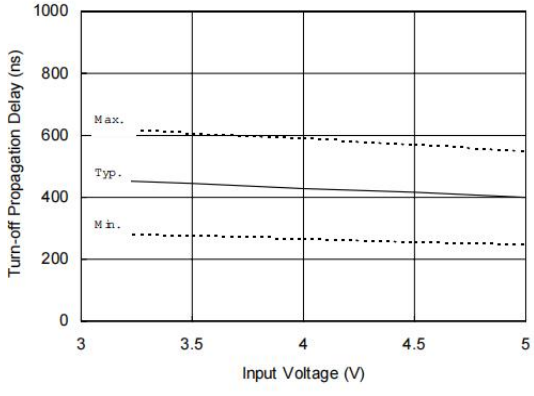


Figure 7C. Turn-off Propagation Delay vs. Input Voltage

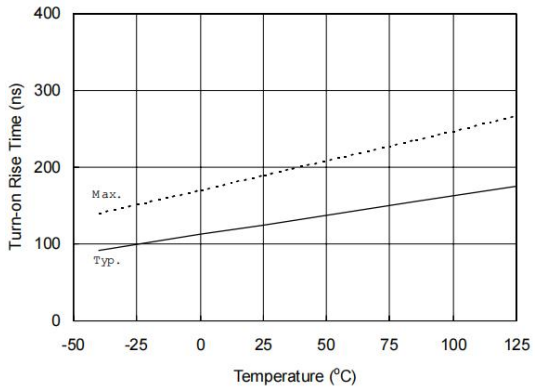


Figure 8A. Turn-on Rise Time vs. Temperature

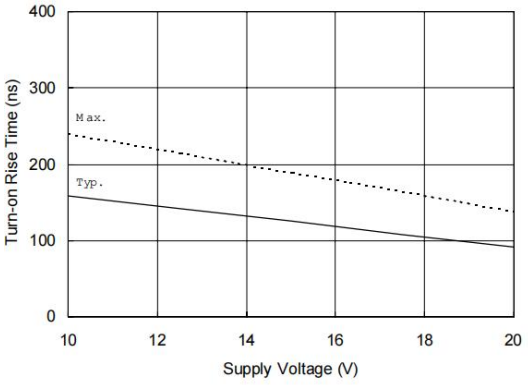


Figure 8B. Turn-on Rise Time vs. Supply Voltage

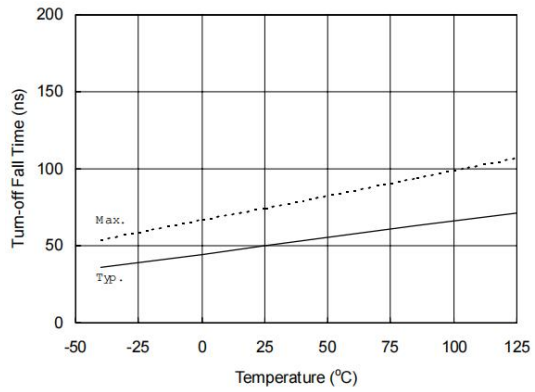


Figure 9A. Turn-off Fall Time vs. Temperature

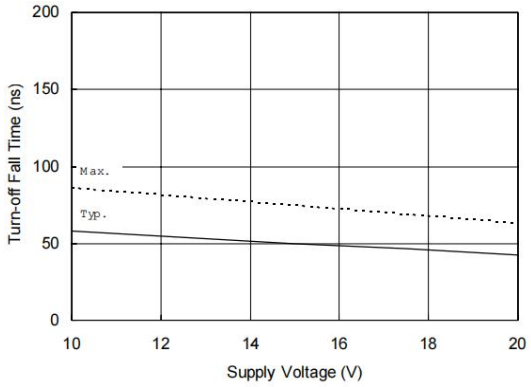


Figure 9B. Turn-off Fall Time vs. Supply Voltage

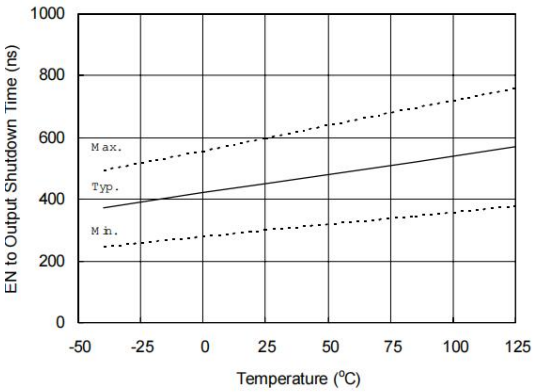


Figure 10A. EN to Output Shutdown Time vs. Temperature

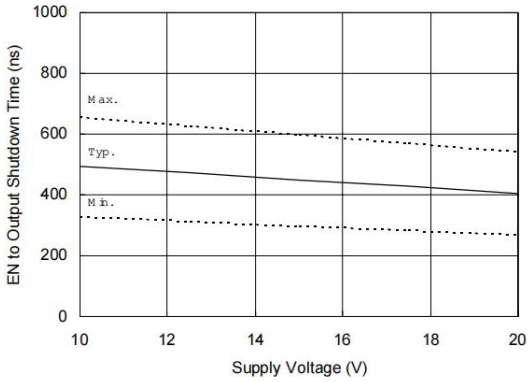


Figure 10B. EN to Output Shutdown Time vs. Supply Voltage

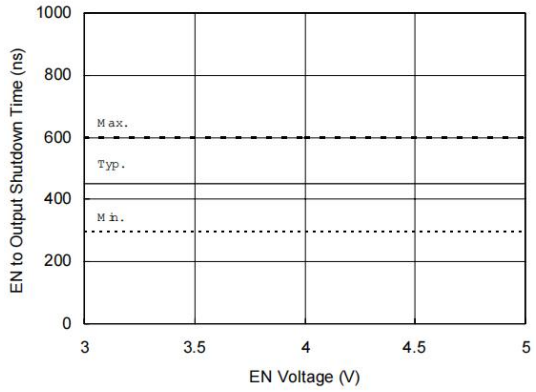


Figure 10C. EN to Output Shutdown Time vs. EN Voltage

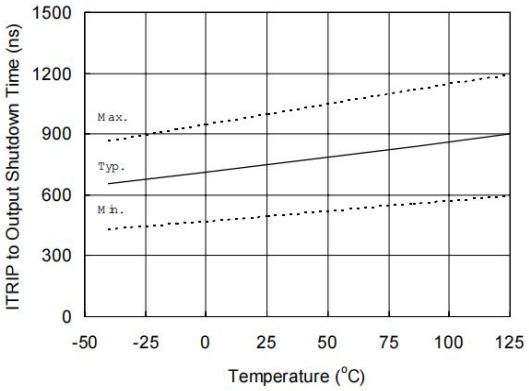


Figure 11A. ITRIP to Output Shutdown Time vs. Temperature

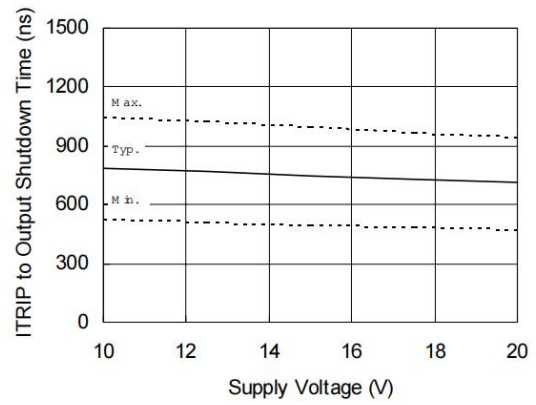


Figure 11B. ITRIP to Output Shutdown Time vs. Supply Voltage

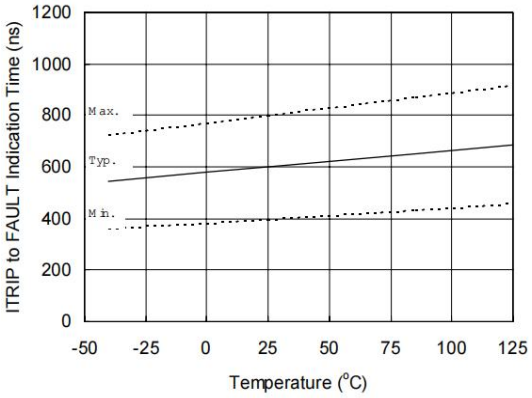


Figure 12A. ITRIP to FAULT Indication Time vs. Temperature

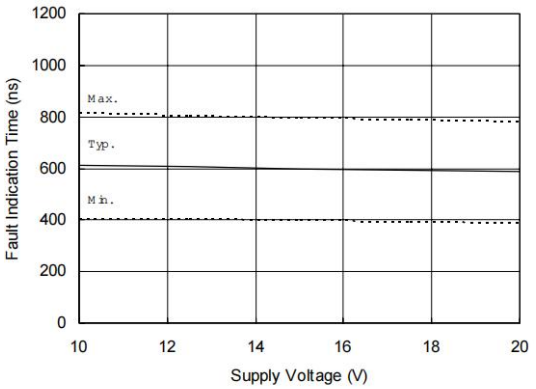


Figure 12B. ITRIP to FAULT Indication Time vs. Supply Voltage

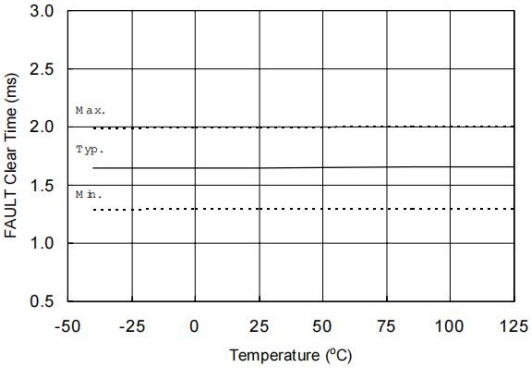


Fig13A. FAULT Clear Time vs. Temperature

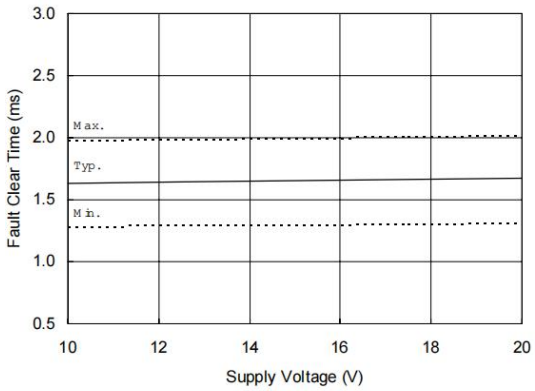


Figure 13B. FAULT Clear Time vs. Supply Voltage

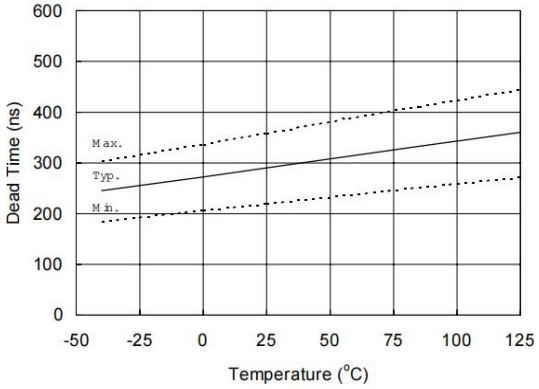


Figure 14A. Dead Time vs. Temperature

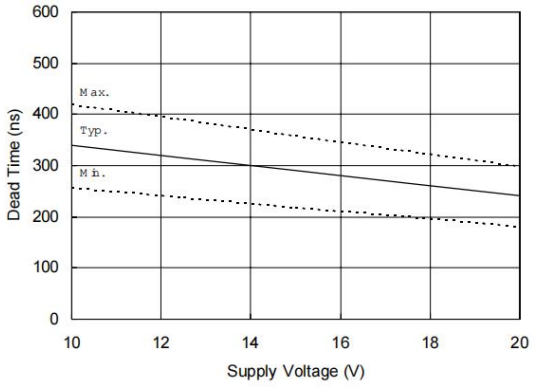


Figure 14B. Dead Time Time vs. Supply Voltage

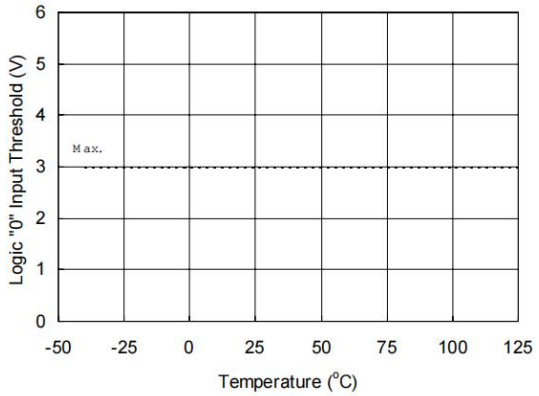


Figure 15A. Logic "0" Input Threshold vs. Temperature

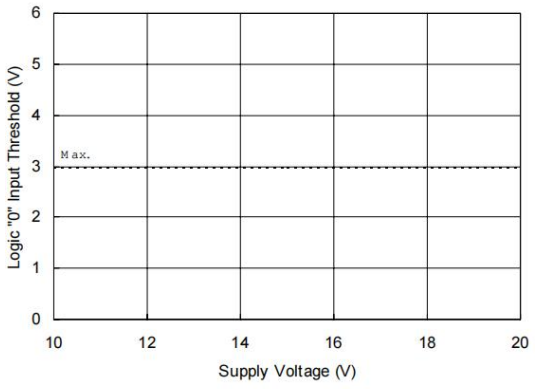


Figure 15B. Logic "0" Input Threshold vs. Supply Voltage

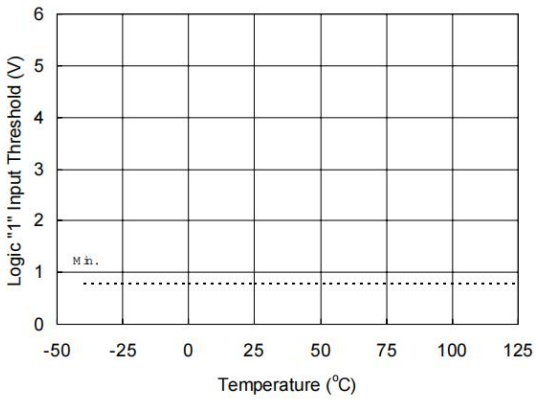


Figure 16A. Logic "1" Input Threshold vs. Temperature

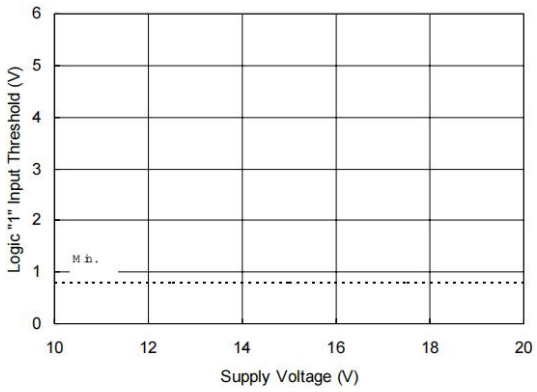


Figure 16B. Logic "1" Input Threshold vs. Supply Voltage

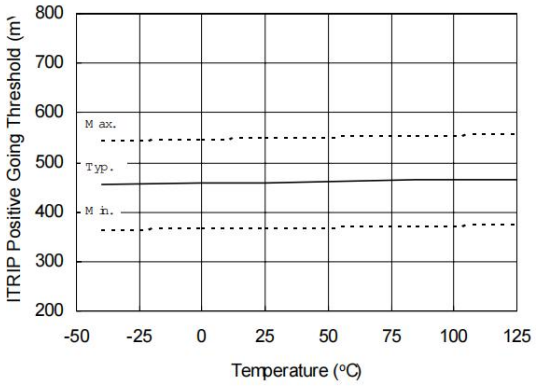


Figure 17A. ITRIP Positive Going Threshold vs. Temperature

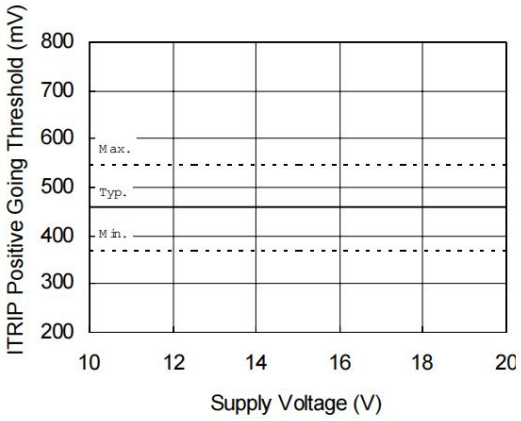


Figure 17B. ITRIP Positive Going Threshold vs. Supply Voltage

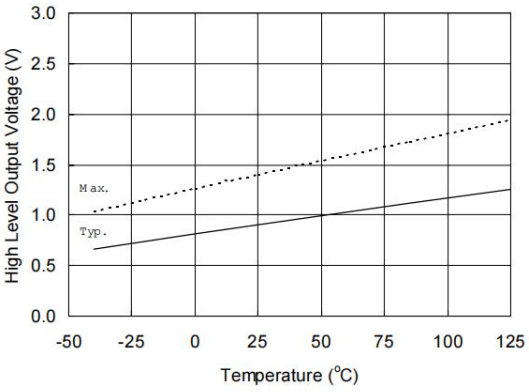


Figure 18A. High Level Output vs. Temperature

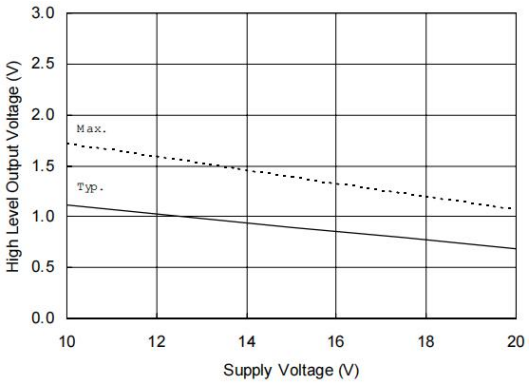


Figure 18B. High Level Output vs. Supply Voltage

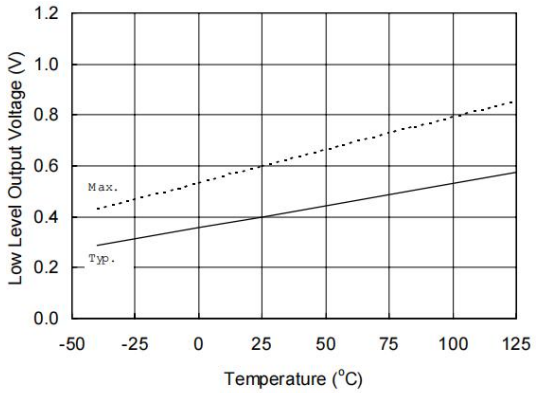


Figure 19A. Low Level Output vs. Temperature

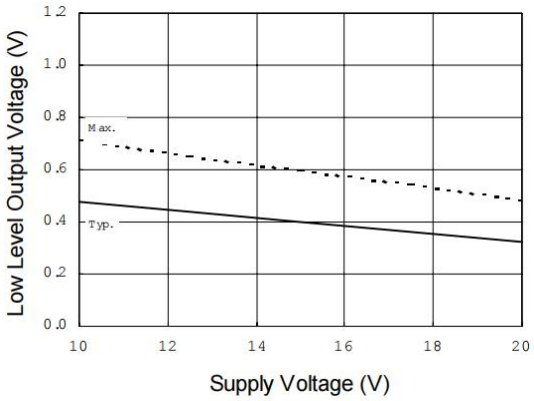


Figure 19B. Low Level Output vs. Supply Voltage

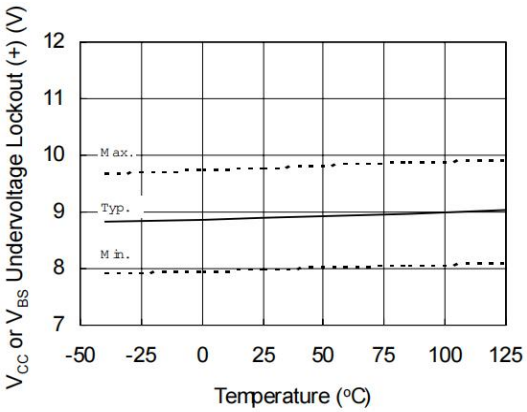


Figure 20. V_{CC} or V_{BS} Undervoltage (+) vs. Temperature

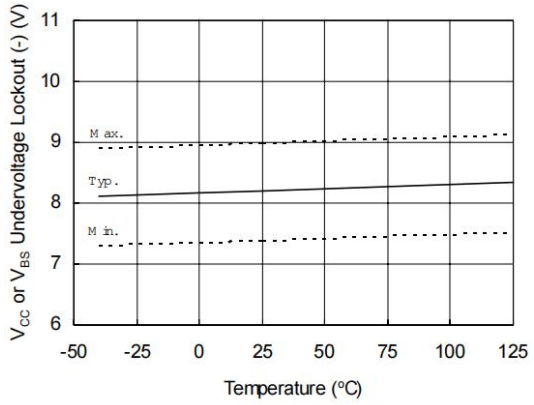


Figure 21. V_{CC} or VBS Undervoltage (-) vs. Temperature

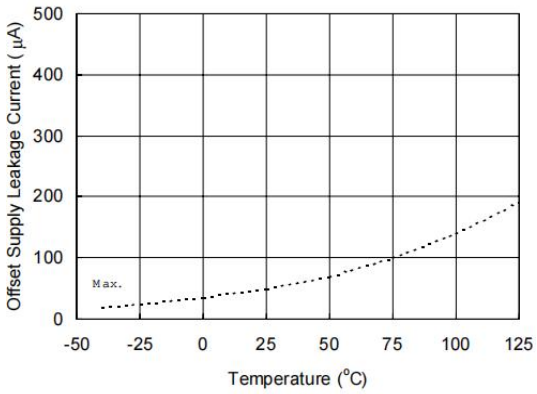


Figure 22A. Offset Supply Leakage Current vs. Temperature

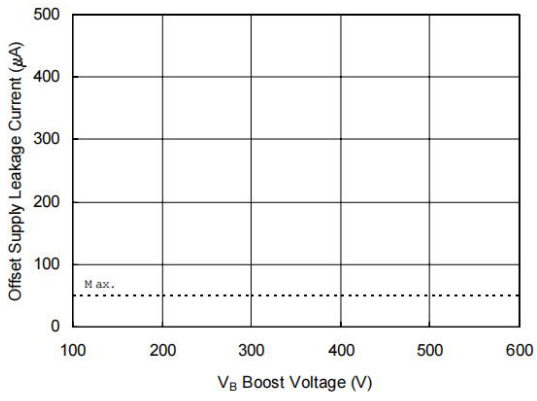


Figure 22B. Offset Supply Leakage Current vs. V_B Boost Voltage

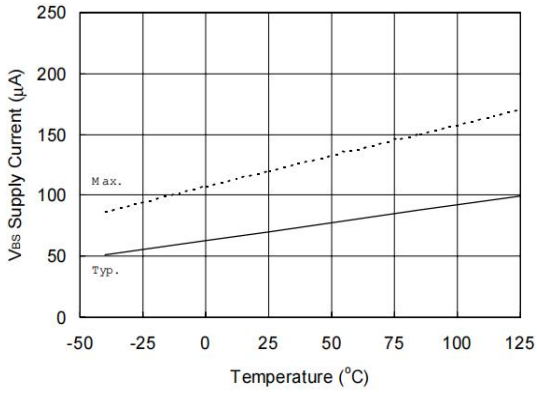


Figure 23A. V_{BS} Supply Current vs. Temperature

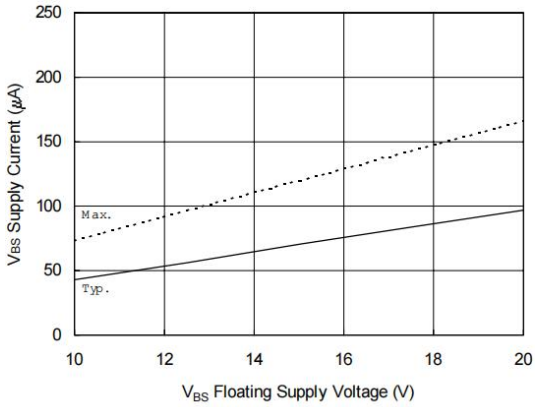


Figure 23B. V_{BS} Supply Current vs. VBS Floating Supply Voltage

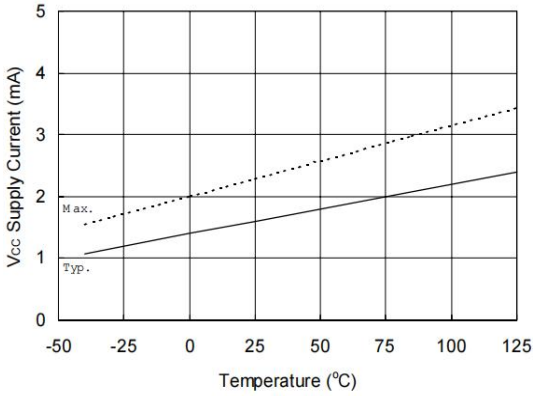


Figure 24A. V_{CC} Supply Current vs. Temperature

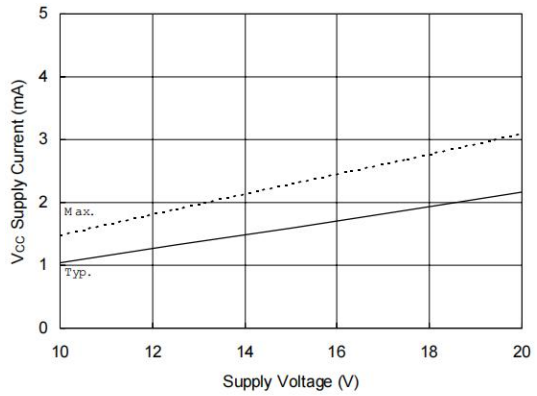


Figure 24B. V_{CC} Supply Current vs. V_{CC} Supply Voltage

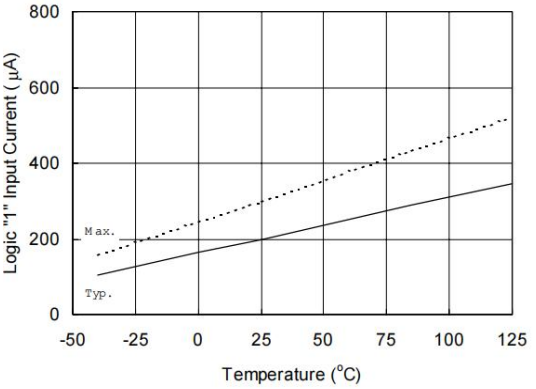


Figure 25A. Logic "1" Input Current vs. Temperature

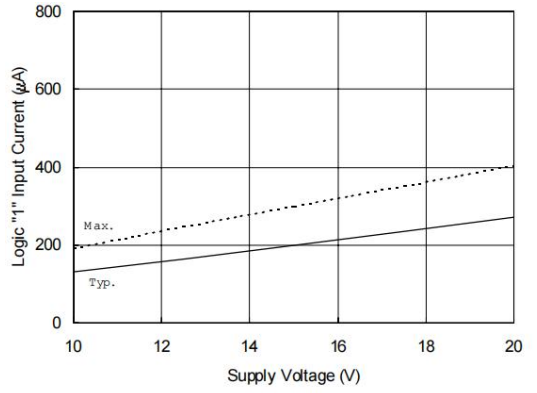


Figure 25B. Logic "1" Input Current vs. Supply Voltage

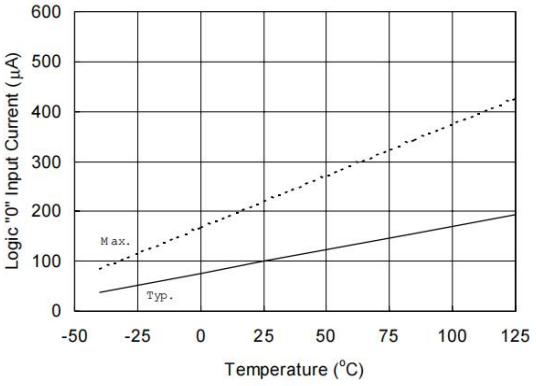


Figure 26A. Logic "0" Input Current vs. Temperature

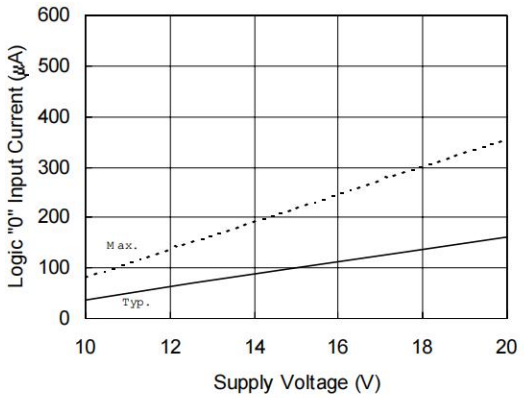


Figure 26B. Logic "0" Input Current vs. Supply Voltage

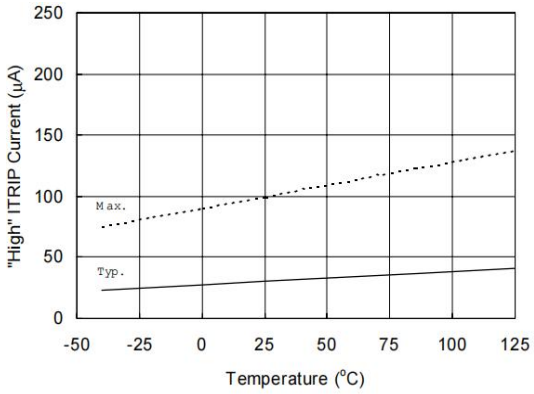


Figure 27A. "High" ITRIP Current vs. Temperature

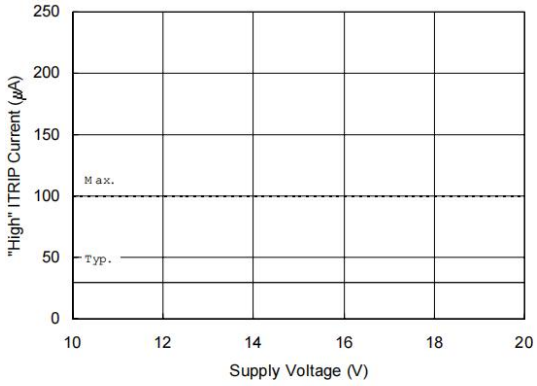


Figure 27B. "High" ITRIP Current vs. Supply Voltage

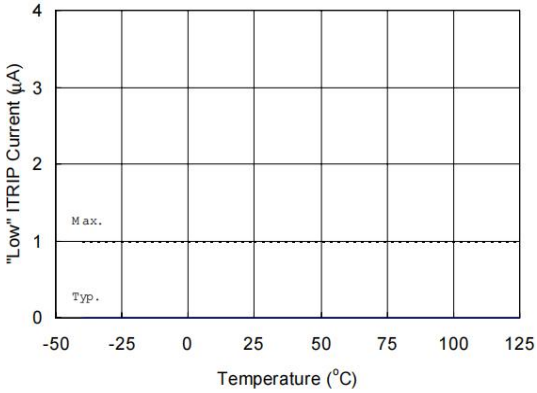


Figure 28A. "Low" ITRIP Current vs. Temperature

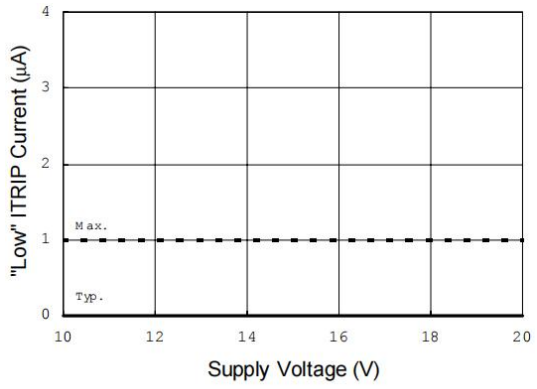


Figure 28B. "Low" ITRIP Current vs. Supply Voltage

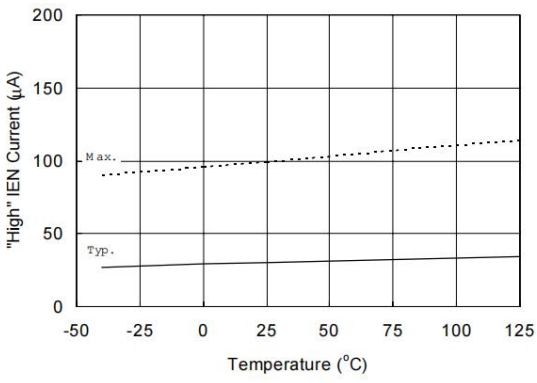


Figure 29A. "High" IEN Current vs. Temperature

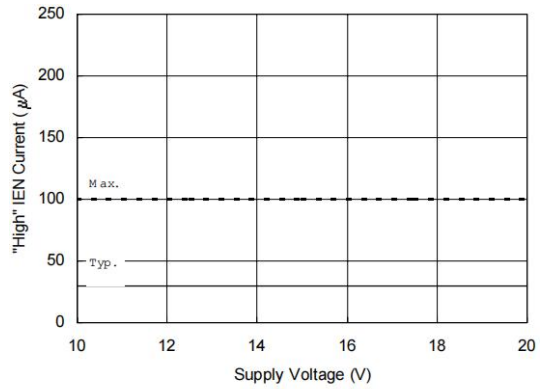


Figure 29B. "High" IEN Current vs. Supply Voltage

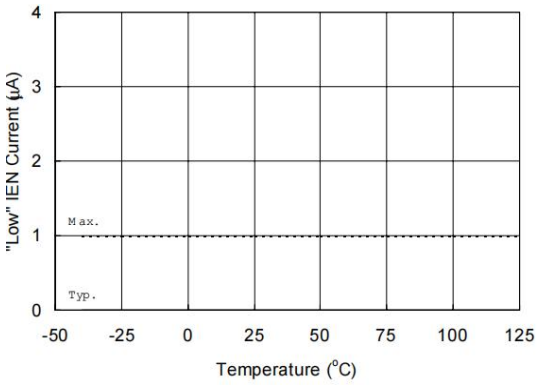


Figure 30A. "Low" IEN Current vs. Temperature

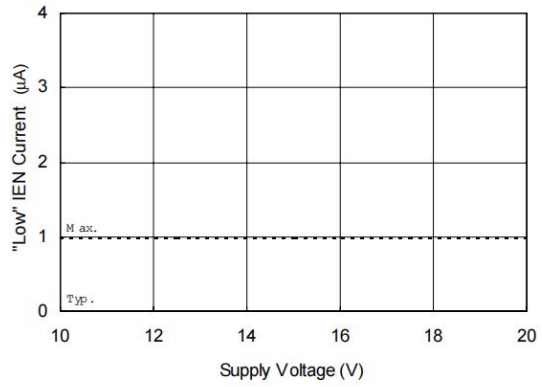


Figure 30B. "Low" IEN Current vs. Supply Voltage

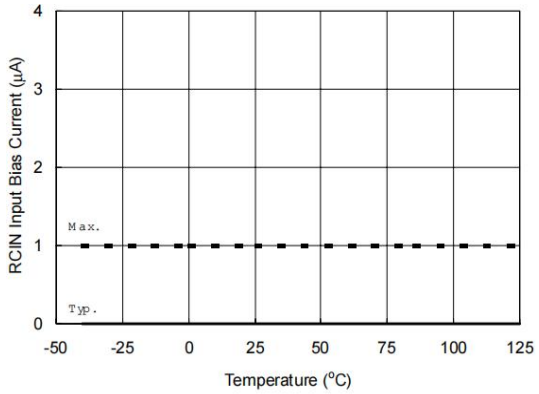


Figure 31A. RCIN Input Bias Current vs. Temperature

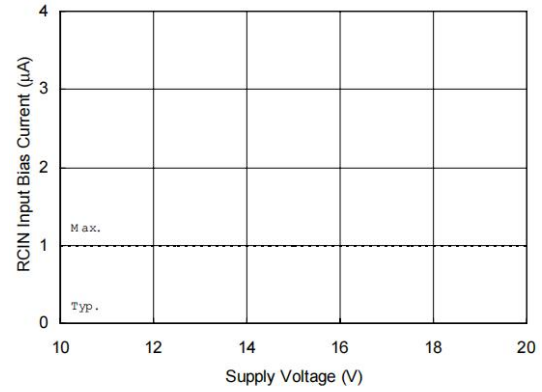


Figure 31B. RCIN Input Bias Current vs. Supply Voltage

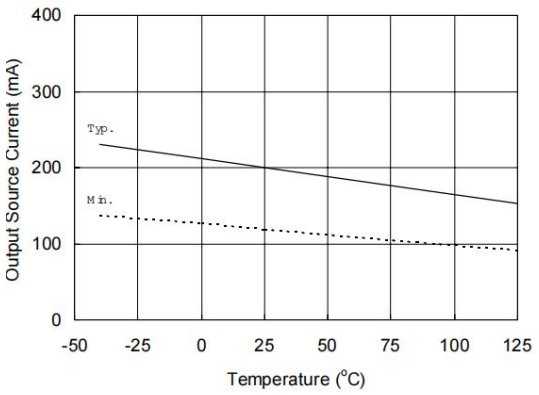


Figure 32A. Output Source Current vs. Temperature

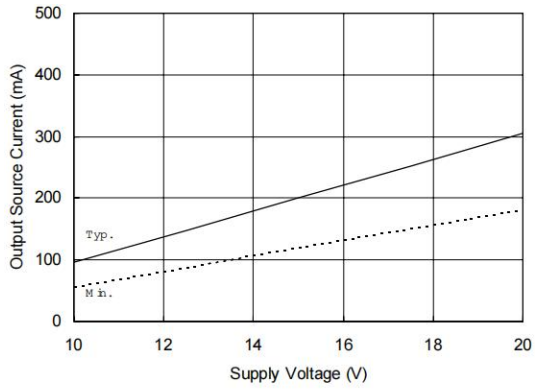


Figure 32B. Output Source Current vs. Supply Voltage

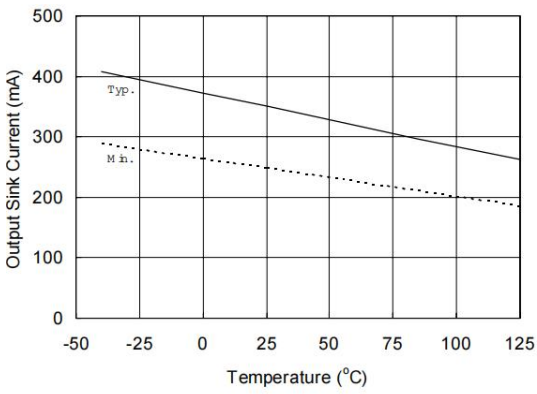


Figure 33A. Output Sink Current vs. Temperature

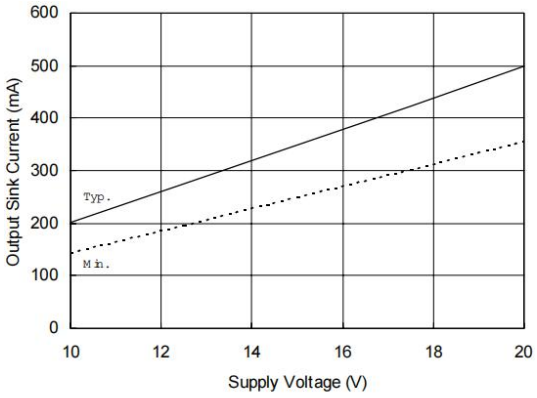


Figure 33B. Output Sink Current vs. Supply Voltage

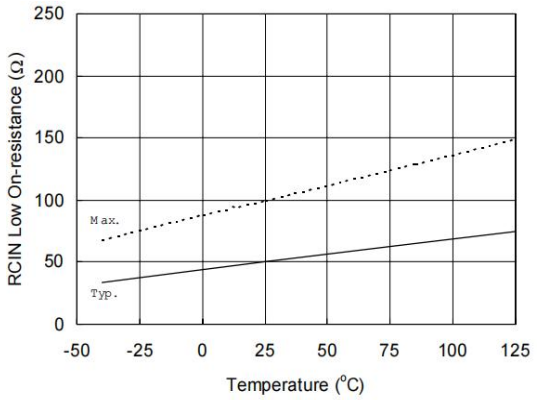


Figure 34A. RCIN Low On-resistance vs. Temperature

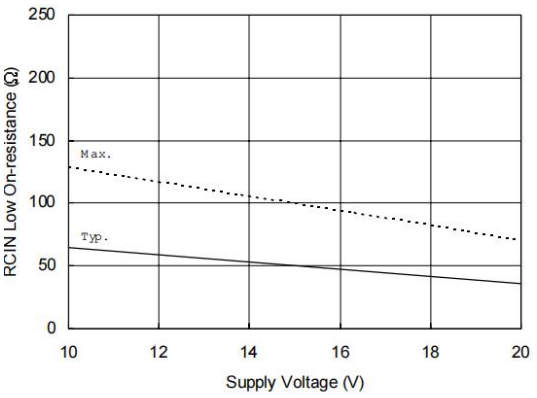


Figure 34B. RCIN Low On-resistance vs. Supply Voltage

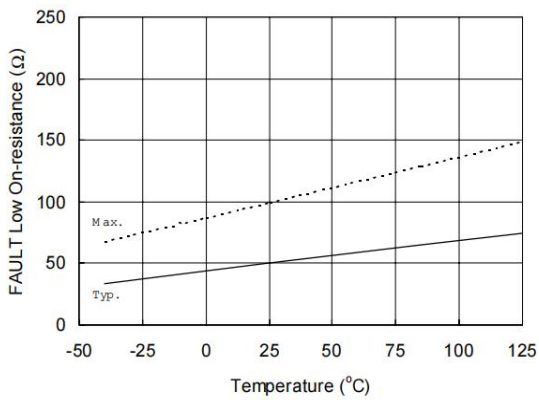


Figure 35A. FAULT Low On-resistance vs. Temperature

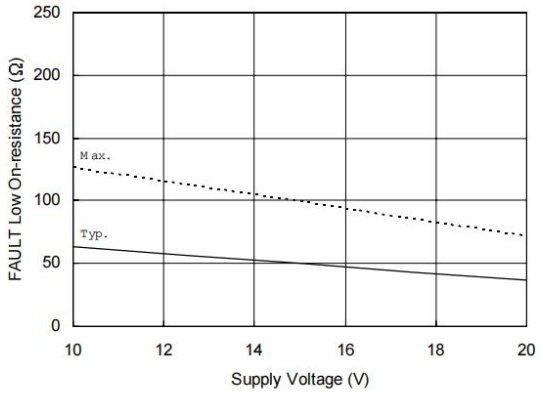


Figure 35B. FAULT Low On-resistance vs. Supply Voltage

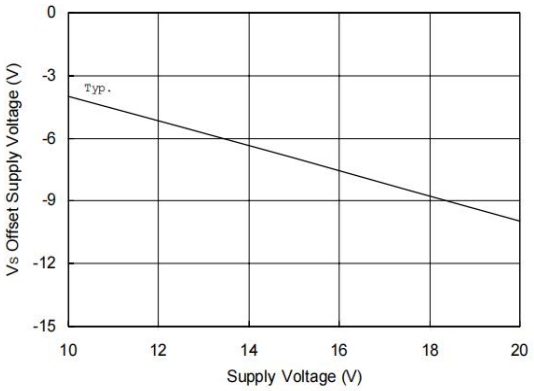


Figure 36. Maximum V_S Negative Offset vs. V_{BS} Supply Voltage

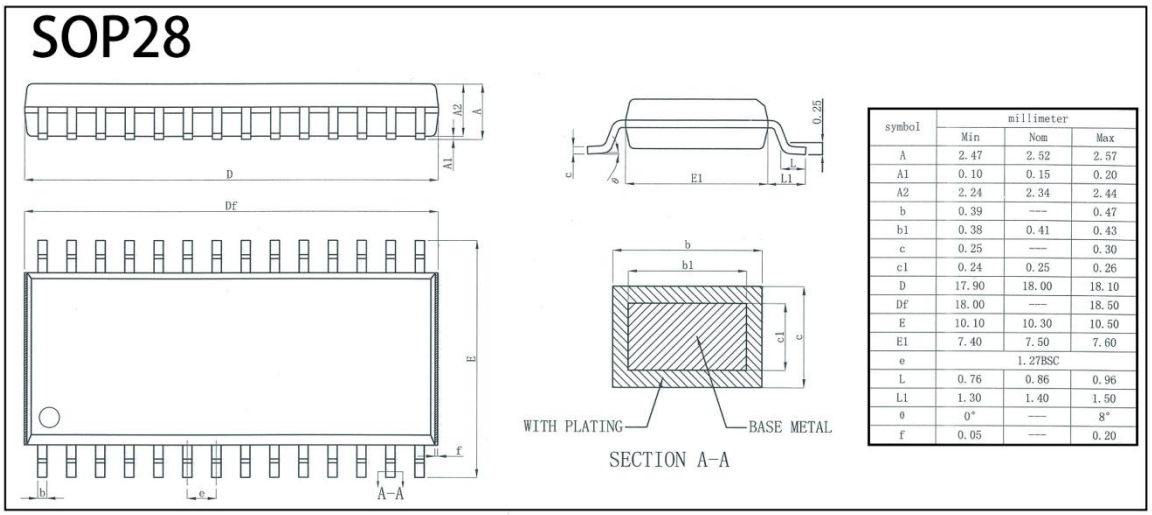
10. ORDERING INFORMATION

Ordering Information

Part Number	Device Making	Package type	Body size (mm)	Temperate (°C)	MSL	Transpo Rt	Package Quantit
XLIR2136STRPBF	XL2136ST	SOP28	18.25*7.50	-40 to +105	MSL3	T&R	1000
XLIR2136PBF	XL2136PBF	DIP28	37.01*13.84	-40 to +105	MSL3	Tube 13	260

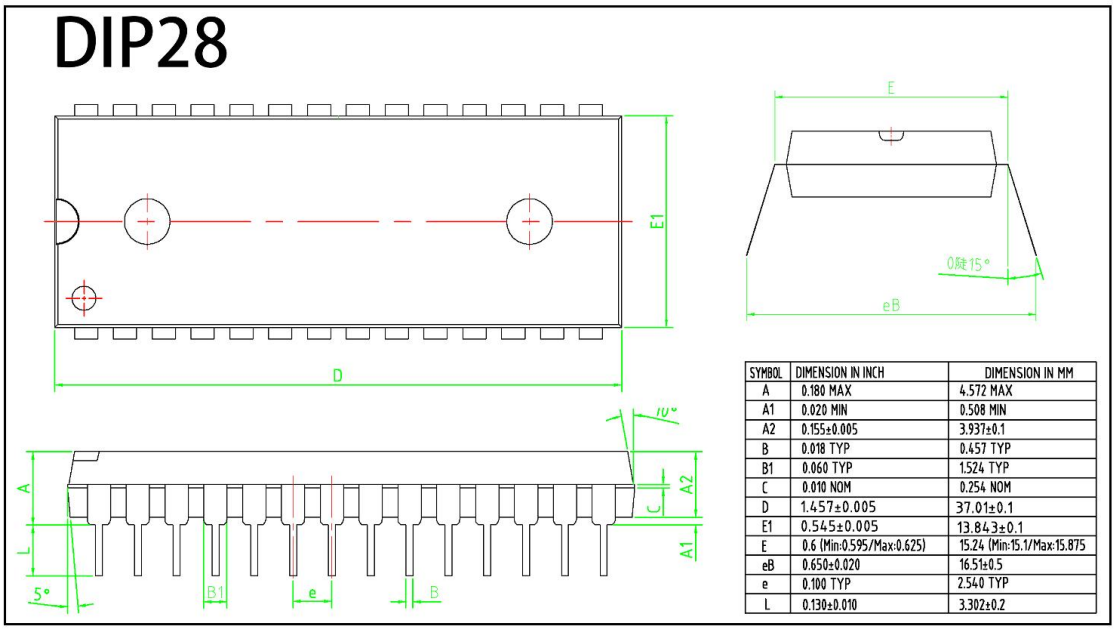
11. DIMENSIONAL DRAWINGS

SOP28



symbol	millimeter		
	Min	Nom	Max
A	2.47	2.52	2.57
A1	0.10	0.15	0.20
A2	2.24	2.34	2.44
b	0.39	----	0.47
b1	0.38	0.41	0.43
c	0.25	----	0.30
c1	0.24	0.25	0.26
D	17.90	18.00	18.10
Df	18.00	----	18.50
E	10.10	10.30	10.50
E1	7.40	7.50	7.60
e		1.27BSC	
L	0.76	0.86	0.96
L1	1.30	1.40	1.50
θ	0°	----	8°
f	0.05	----	0.20

DIP28



SYMBOL	DIMENSION IN INCH	DIMENSION IN MM
A	0.180 MAX	4.572 MAX
A1	0.020 MIN	0.508 MIN
A2	0.155±0.005	3.937±0.1
B	0.018 TYP	0.457 TYP
B1	0.060 TYP	1.524 TYP
C	0.010 NOM	0.254 NOM
D	1.457±0.005	37.01±0.1
E1	0.545±0.005	13.843±0.1
E	0.6 (Min:0.595/Max:0.625)	15.24 (Min:15.1/Max:15.875
eB	0.650±0.020	16.51±0.5
e	0.100 TYP	2.540 TYP
L	0.130±0.010	3.302±0.2