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Nyfea product specification

PRODUCT SPECIFICATION

Customer : _____

Product Name : 8 Channel SMBus and I2C Switch

Part NO : FCA9548

Issue Date : _____

Prepared	Checked	Customer Check
ChenTT	Zelig	

NYFEA

1 Features

- I²C Bus and SMBus compatible
- SCL Frequency: 0 ~ 1MHz
- 1-of-8 Bidirectional translating switches
- Active-low reset input $\overline{\text{RESET}}$
- Three address pins, allowing up to eight FCA9548 devices on the I²C Bus
- Allows voltage-level translation between 1.8V, 2.5V, 3.3V, 5V buses
- Low on-resistance, low standby current
- Supply voltage: 1.65V ~ 5.5V
- Support hot insertion
- Package information:

PART NUMBER	PACKAGE	BODY SIZE(mm²)
FCA9548T	TSSOP-24	7.80 × 4.40
FCA9548Q	QFN-24	4.00 × 4.00

2 Applications

- Servers
- Routers
- Products with I²C slave address conflicts

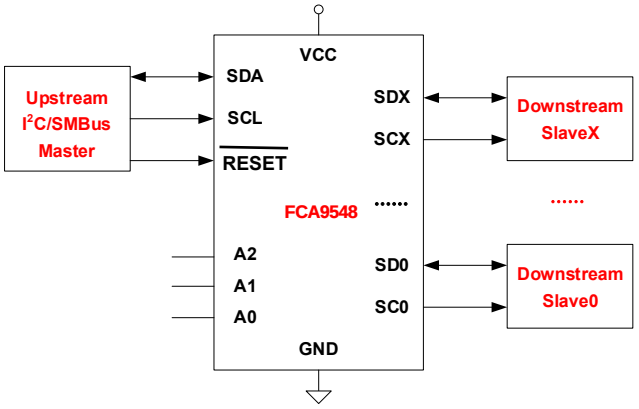
3 Description

The FCA9548 is a quad bidirectional translating switch controlled via the I2C bus. The SCL/SDA upstream pair fans out to four downstream pairs, or channels. Any individual SCX / SDX channel or combination of channels can be selected, determined by the contents of the programmable control register.

An active-low reset input $\overline{\text{RESET}}$ allows the FCA9548 to recover from a situation in which one of the downstream I2C buses is stuck in a low state. Pulling $\overline{\text{RESET}}$ low resets the I2C state machine and causes all the channels to be deselected, as does the internal power-on reset function.

The pass gates of the switches are constructed such that the VCC pin can be used to limit the maximum high voltage, which will be passed by the FCA9548. This allows the use of different bus voltages on each pair, so that 1.8V, 2.5V, or 3.3V parts can communicate with 5-V parts without any additional protection. External pull-up resistors pull the bus up to the desired voltage level for each channel. All I/O pins are 5.5-V tolerant.

Figure 1 Simplified Diagram of FCA9548



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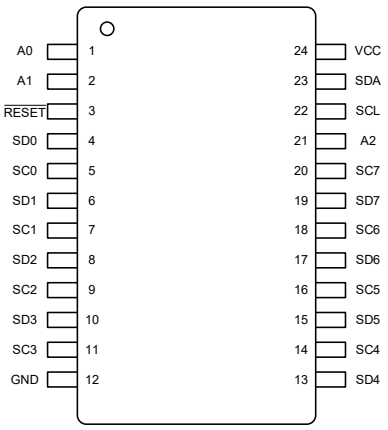
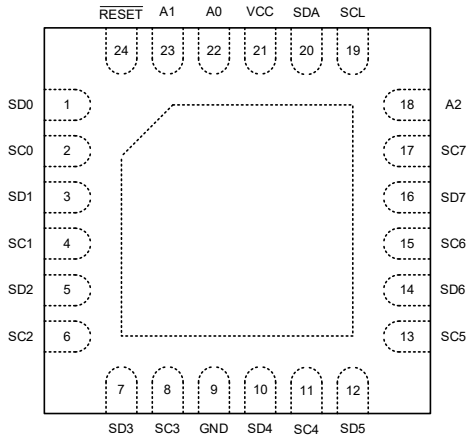
4. Pin Configuration and Functions

FCA9548 24-PIN TSSOP Top View



FCA9548 24-PIN QFN Top View



Pin Functions of TSSOP / QFN Package

PIN			TYPE	DESCRIPTION
NAME	TSSOP	QFN		
A0	1	22	I	Address input 0. Connect directly to VCC or ground.
A1	2	23	I	Address input 1. Connect directly to VCC or ground.
A2	21	18	I	Address input 2. Connect directly to VCC or ground.
GND	12	9	—	Ground.
$\overline{\text{RESET}}$	3	24	I	Active low reset input. Connect to VCC or V_{DPUM} through a pull-up resistor, if not used.
SD0	4	1	I/O	Serial data 0. Connect to V_{DPU0} through a pull-up resistor.
SC0	5	2	I/O	Serial clock 0. Connect to V_{DPU0} through a pull-up resistor.
SD1	6	3	I/O	Serial data 1. Connect to V_{DPU1} through a pull-up resistor.
SC1	7	4	I/O	Serial clock 1. Connect to V_{DPU1} through a pull-up resistor.
SD2	8	5	I/O	Serial data 2. Connect to V_{DPU2} through a pull-up resistor.
SC2	9	6	I/O	Serial clock 2. Connect to V_{DPU2} through a pull-up resistor.
SD3	10	7	I/O	Serial data 3. Connect to V_{DPU3} through a pull-up resistor.
SC3	11	8	I/O	Serial clock 3. Connect to V_{DPU3} through a pull-up resistor.
SD4	13	10	I/O	Serial data 4. Connect to V_{DPU4} through a pull-up resistor.
SC4	14	11	I/O	Serial clock 4. Connect to V_{DPU4} through a pull-up resistor.
SD5	15	12	I/O	Serial data 5. Connect to V_{DPU5} through a pull-up resistor.
SC5	16	13	I/O	Serial clock 5. Connect to V_{DPU5} through a pull-up resistor.
SD6	17	14	I/O	Serial data 6. Connect to V_{DPU6} through a pull-up resistor.
SC6	18	15	I/O	Serial clock 6. Connect to V_{DPU6} through a pull-up resistor.
SD7	19	16	I/O	Serial data 7. Connect to V_{DPU7} through a pull-up resistor.
SC7	20	17	I/O	Serial clock 7. Connect to V_{DPU7} through a pull-up resistor.
SCL	22	19	I/O	Serial clock line. Connect to V_{DPUM} through a pull-up resistor.
SDA	23	20	I/O	Serial data line. Connect to V_{DPUM} through a pull-up resistor.
VCC	24	21	Power	Supply power.

Note: VCC is the supply of FCA9548, V_{DPUM} is the supply of the master, and $V_{DPU7\sim0}$ is the supply of the channel 7~0.

5 Specifications

5.1 Absolute Maximum Ratings

	MIN	MAX	UNIT
Supply voltage VCC	-0.5	7	V
Input voltage V_I	-0.5	7	V
Input current I_I		±20	mA
Output current I_O		±25	mA
Continuous current through VCC/GND pin		±100	mA
Total power dissipation		400	mW
Operating free-air temperature range	-40	85	℃
Storage temperature range	-60	150	℃

Unless otherwise specified, the specifications in the above table apply within the atmospheric temperature range.

Stresses beyond the range may cause permanent damage to the device.

5.2 ESD Ratings

		Value	UNIT
Electrostatic Discharge	Human-body mode (HBM), per ANSI/ESDA/JEDEC JS-001-2017.	±8000	V
	Charged-device model (CDM), per ANSI/ESDA/JEDEC JS-002-2022	±1400	V
Latch-up Effect	Latch-up (LU), per JESD 78F (2022)	±200	mA

5.3 Recommended Operating Conditions

		MIN	NOM	MAX	UNIT
Supply voltage VCC		1.65		5.5	V
High-level input voltage V_{IH}	SCL, SDA	0.7*VCC		6	V
	A2, A1, A0, $\overline{\text{RESET}}$	0.7*VCC		VCC+0.5	
Low-level input voltage V_{IL}	SCL, SDA	-0.5		0.3*VCC	V
	A2, A1, A0, $\overline{\text{RESET}}$	-0.5		0.3*VCC	
Operating temperature range		-40		85	℃

Unless otherwise specified, the specifications in the above table apply within the atmospheric temperature range.

5.4 Electrical Characteristics

Unless otherwise specified, the following data are characteristics at +25℃ and the power supply voltage is in the range of 1.65 V to 5.5 V.

Parameter	Test Conditions	MIN	TYP	MAX	UNIT
Power-on Reset V_{PORR}	VCC rising, No Load		1.20	1.50	V
Power-on Reset V_{PORR}	VCC falling, No Load	0.80	1.05		V
VCC(1) at transmission across voltage domains	V_{PASS}=1V, R_P=4.7kohm(2)			2.2	V
	V_{PASS}=1.8V, R_P=4.7kohm			3.2	
	V_{PASS}=2.5V, R_P=4.7kohm			4.1	
	V_{PASS}=3.3V, R_P=4.7kohm			5.1	
I_{OL}	SDA, V_{OL}=0.4V	3	6.5		mA
	SDA, V_{OL}=0.6V	6	9.7		
F_{SCL}(3)	Standard-Mode			100	kHz
	Fast Mode			400	kHz
	Fast Mode Plus			1000	kHz
Switch on-state resistance R_{ON}	V_O=0.4V, I_O=10mA, VCC=1.8V		52		ohm
	V_O=0.4V, I_O=10mA, VCC=3.3V		10		
	V_O=0.4V, I_O=10mA, VCC=5.5V		7		
	V_O=0.4V, I_O=15mA, VCC=3.3V		10		
	V_O=0.4V, I_O=15mA, VCC=5.5V		7		
C_I	A2, A1, A0, $\overline{RESET}$		4.5	6	pF
I_{CC}	VCC=1.65V, F_{SCL}=100kHz		2		μA
	VCC=3.3V, F_{SCL}=100kHz		4		
	VCC=5.5V, F_{SCL}=100kHz		10		
	VCC=1.65V, F_{SCL}=400kHz		3		
	VCC=3.3V, F_{SCL}=400kHz		6		
	VCC=5.5V, F_{SCL}=400kHz		17		
	VCC=1.65V, SCL=SDA=VDPUM		0.4	0.6	
	VCC=2.7V, SCL=SDA=VDPUM		0.7	1.1	
	VCC=3.3V, SCL=SDA=VDPUM		1.0	1.3	
	VCC=5.5V, SCL=SDA=VDPUM		1.6	2	
$\overline{RESET}$ Pin reset pulse time		20			ns

Note：(1) For details on transmission across voltage domains, see Section 6.2.3 .

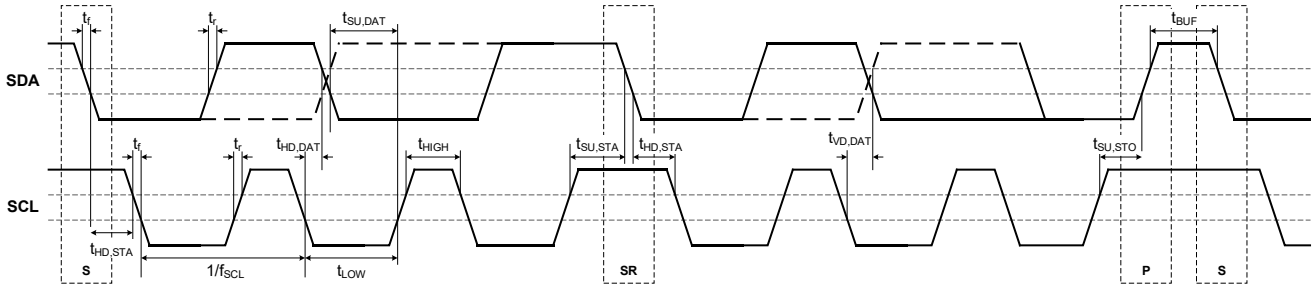
(2) R_P is the pull-up resistor of the corresponding channel. All channel pull-up resistors have equal values.

(3) When F_{SCL}⩾400kHz, the pull-up resistance RP should be ⩽1kohm, depending on the bus load capacitance.

5.5 I²C Timing Requirements

Unless otherwise specified, the following data are the characteristics of the chip in the range of -40 to +85°C.

	Description	Standard-Mode		Fast-Mode		Fast-Mode Plus		Unit
		MIN	MAX	MIN	MAX	MIN	MAX	
f_{SCL}	SCL operating frequency	0	100	0	400	0	1000	kHz
$t_{HD,STA}$	hold time after repeated start condition; After this period, the first clock is generated	4.0		0.6		0.26		μs
t_{LOW}	SCL clock low period	4.7		1.3		0.5		μs
t_{HIGH}	SCL clock high period	4.0		0.6		0.26		μs
$t_{SU,STA}$	repeated start condition setup time	4.7		0.6		0.26		μs
$t_{HD,DAT}$	data hold time	0		0		0		ns
$t_{SU,DAT}$	data setup time	250		100		50		ns
t_r	rise time of SDA and SCL		1000	20	300		120	ns
t_f	fall time of SDA and SCL		300	20*VCC /5.5	300	20*VCC /5.5	120	ns
$t_{SU,STO}$	stop condition setup time	4.0		0.6		0.26		μs
t_{BUF}	bus free time between stop and start condition	4.7		1.3		0.5		μs
$t_{VD,DAT}$	data valid time		3.45		0.9		0.45	μs
C_b	capacitive load for each bus line		400		400		550	pF



6 Detailed Description

6.1 I²C Serial Interface

6.1.1 Bus Overview

I²C interface uses the serial data line SDA and the serial clock line SCL to achieve bidirectional data transmission between different IC devices. Both the SDA and SCL buses need to be connected to the power line through a pull-up resistor R_P. Data transmission only occurs when the bus is not occupied (SDA=SCL=1). In the I²C interface protocol, only one data bit is transmitted during each SCL clock pulse; during the high level of the clock pulse, the data on the SDA bus must remain stable, and any changes in the SDA bus will be recognized as controlling signals. When the bus is not occupied and the SCL bus is high, the change of the SDA bus from high level to low level is defined as start condition, and the change of the SDA bus from low level to high level is defined as stop condition, as shown in Figure 2.

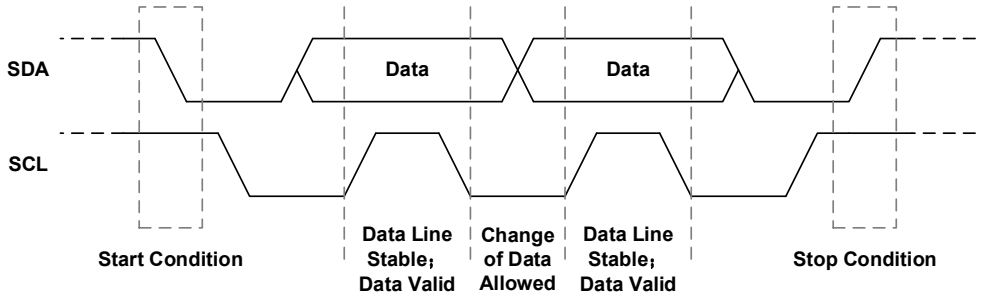


Figure 2. Start Condition, Stop Condition, and Data Bit Transmission in I²C Communication

During I²C communication, a device generating a message is a transmitter and receiving is the receiver. The device that controls the message is the master, and that are controlled by the master are the slaves.

Between the start condition and the stop condition, the data bytes transmitted between the host and the slave are not restricted, and each data byte (8 bits) must be followed by an ACK bit. When the host sends data to the slave, after sending a byte, the host must release the SDA bus so that the slave to respond to the data can pull down the SDA bus to generate an ACK bit and successfully respond to the sent byte. When the slave returns data to the host, the SDA bus also needs to be released after the slave returns a byte so that the host can generate an ACK bit to successfully respond to the returned data byte. During the high pulse of the ninth SCL clock when sending ACK, the SDA bus must maintain a stable low level, and the setup time and hold time of the I²C communication protocol should be met here.

When the slave returns the last byte to the host, the host must send a NACK bit, releases the SDA bus and pulls it high. After that, the host generates a termination condition, and the data transmission ends.

6.1.2 Control Register

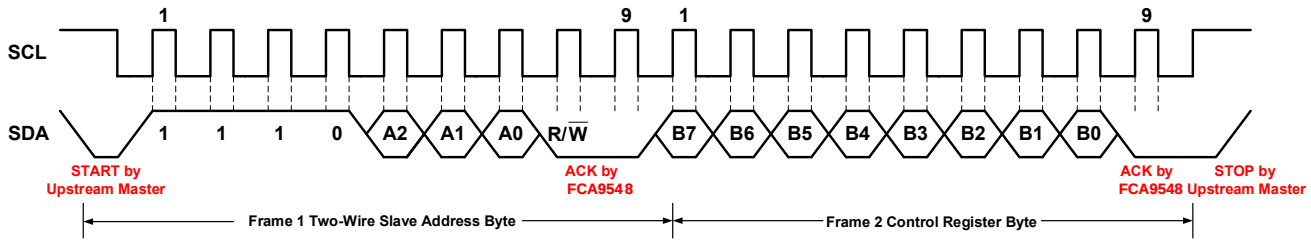


Figure 3 Diagram of Control Register Write Operation

During the use of the chip, the upstream host can configure the control registers inside the FCA9548 to determine the data transmission between the upstream host and one or more downstream slaves. Figure 3 shows a schematic diagram of the upstream host's write operation to the Control register. The upstream host first sends a slave address byte with LSB=0 (i.e., read/write bit = 0) to address the corresponding FCA9548 on the bus. The lower 3 bits of the slave address byte are the address selection bits, and FCA9548 can be configured with a total of 8 different slave addresses through the A2, A1, and A0 bits. The values of bits A2, A1, and A0 are determined by the connection relationship of the A2, A1, and A0 address pins of the chip. If the corresponding address pin

is connected to the power supply voltage, the value of the corresponding address bit is 1; If the corresponding address pin is connected to the ground voltage, the value of the corresponding address bit is 0. See Details in Table 1.

Table 1 Address Reference

ADDRESS PIN CONNECTION			I²C SLAVE ADDRESS
A2	A1	A0	
GND	GND	GND	112d / 70h
GND	GND	VCC	113d / 71h
GND	VCC	GND	114d / 72h
GND	VCC	VCC	115d / 73h
VCC	GND	GND	116d / 74h
VCC	GND	VCC	117d / 75h
VCC	VCC	GND	118d / 76h
VCC	VCC	VCC	119d / 77h

After the addressed FCA9548 successfully responds to the slave address byte, the upstream host proceeds to send the Control register configuration byte.

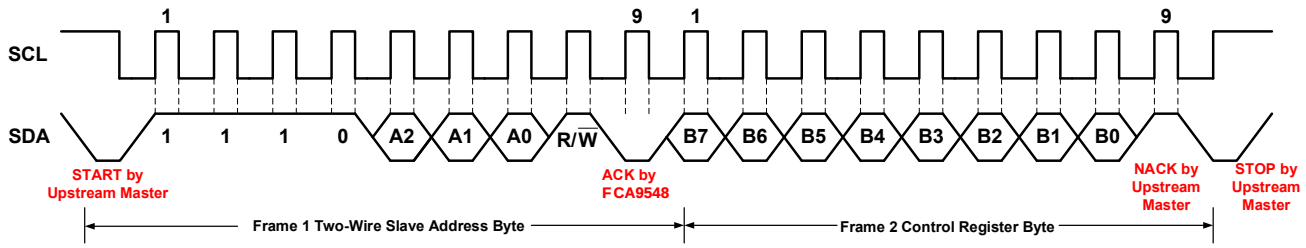


Figure 4 Diagram of Control Register Read Operation

Figure 4 shows a schematic of the upstream host reading the FCA9548 Control registers.

Table 2 gives a bit description of the FCA9548 Control registers. All bits of this register are readable and writeable, and are used to control the data transmission between the upstream slave and one or more downstream channel slaves. When a bit in B7~B0 is written as 1, the switch between the SDX and SCX buses of the slave of the corresponding downstream channel, and the SDA and SCL buses of the upstream master, will be turned on at the Stop Condition at the end of the write operation to the control register. The initial power-up value of the FCA9548 Control register is 00h, that is, the initial power-up state of all downstream channels is off. The FCA9548 allows multiple downstream channels to be open at the same time, taking care that the capacitive load on the bus does not exceed the maximum required in Section 5.5.

Table 2 The definition of Control register

B7	B6	B5	B4	B3	B2	B1	B0	Description
X	X	X	X	X	X	X	0	Channel 0 disabled
							1	Channel 0 enabled
X	X	X	X	X	X	0	X	Channel 1 disabled
						1		Channel 1 enabled
X	X	X	X	X	0	X	X	Channel 2 disabled
					1			Channel 2 enabled
X	X	X	X	0	X	X	X	Channel 3 disabled
				1				Channel 3 enabled
X	X	X	0	X	X	X	X	Channel 4 disabled
			1					Channel 4 enabled
X	X	0	X	X	X	X	X	Channel 5 disabled
		1						Channel 5 enabled
X	0	X	X	X	X	X	X	Channel 6 disabled
	1							Channel 6 enabled
0	X	X	X	X	X	X	X	Channel 7 disabled
1								Channel 7 enabled
0	0	0	0	0	0	0	0	No channel selected

6.2 Device Functional Modes

6.2.1 Power-On Reset

When the supply voltage of the VCC pin of the FCA9548 is powered up, both the control registers and the I2C state machine inside the chip remain in the initial state, at which point all downstream channels are turned off and all bits in the control registers are reset to 0. This initial state will be maintained until VCC>VPORR, after which the FCA9548 will perform the corresponding functions based on actual usage. When the supply voltage of the VCC pin drops to VCC<VPORF, the FCA9548 is reset back to its initial state.

6.2.2 RESETN

The active-low reset pin $\overline{\text{RESET}}$ of FCA9548 can be used to globally reset the chip when meeting a bus-fault condition. To ensure smooth chip reset, the low pulse time applied to the $\overline{\text{RESET}}$ pin must be more than 20ns. When the reset pin is not needed, please connect the pin to the power supply voltage through a pull-up resistor to prevent accidental chip reset.

6.2.3 Data Transmission Across Voltage Domains

The FCA9548 series allow the upstream host and the downstream channel slaves to transmit data across voltage domains. At this time, the power supply voltage VCC of the series limits the lowest voltage allowed for upstream and downstream transmission. This function can achieve data interaction between upstream and downstream without additional protection in the 1.8V, 3.3V, and 5.0V voltage domains. When using this function, it is necessary to ensure that the I²C bus of each upstream and downstream channel is connected to the required power supply voltage through the pull-up resistor R_P, as shown in Figure 5.

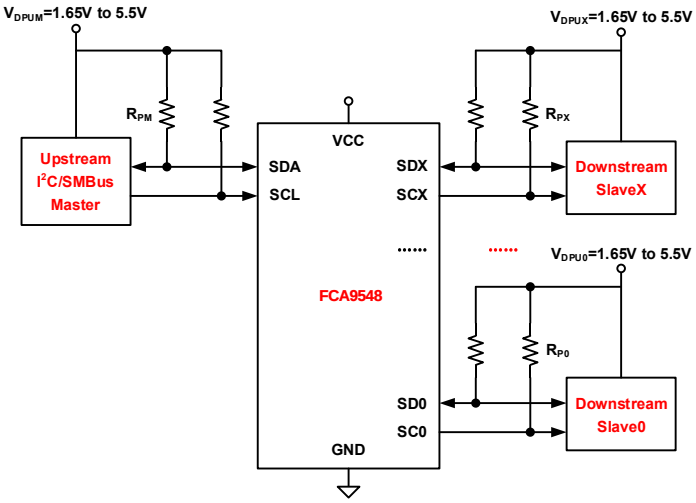


Figure 5 Diagram of Data Transmission Across Voltage Domains

In Figure 5, the power supply voltage of the upstream host is V_{DPUM}, and the supply voltage of each downstream channel slave is V_{DPUX}; SDA and SCL are connected to V_{DPUM} through pull-up resistors R_{PM}; SDX and SCX are connected to V_{DPUX} through the pull-up resistor R_{PX}. The minimum transmission voltage V_{PASS} = min

(V_{DPUM} , V_{DPU0} , ⋯, V_{DPUX}) is defined.

When the Control register of FCA9548 is configured to open channel X, the data transmission on the bus is shown in Figure 6 and Figure 7 (taking SDA and SDX buses as examples), where Figure 6 is the diagram of high-level transmission on the bus and Figure 7 is the diagram of low-level transmission on the bus. Since the circuit system is symmetrical, only the case of V_{DPUM} ＞V_{DPUX} is discussed, that is, V_{PASS} =V_{DPUX}, and V_{DPUM} is always 5.5V.

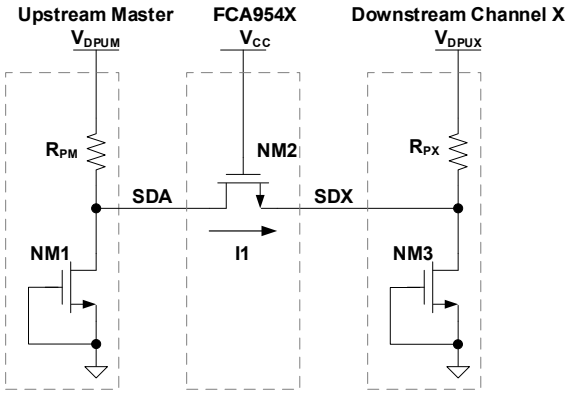


Figure 6 Diagram of High-level Bus Transmission

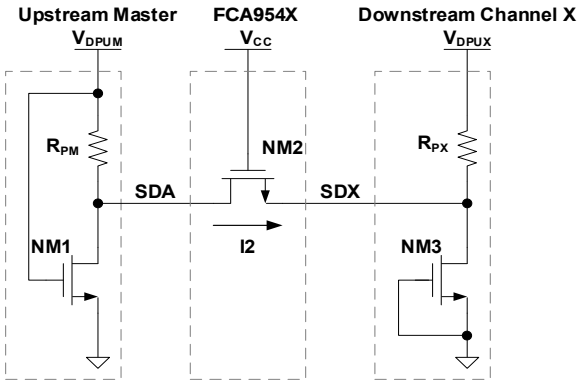


Figure 7 Diagram of Low-level Bus Transmission

When high-level transmission is performed, the following conditions must be met to ensure that the system in Figure 6 works normally:

1) SDA＞0.7*VDPUM, that means SDA will always be recognized as high-level by the upstream host;

2) SDX＜1.1*VDPUX, that means SDX will not exceed the port withstand voltage value of the downstream channel slave;

When V_{PASS}=V_{DPUX}, 2) is the main limitation factor, from which the maximum value of VCC of FCA9548 under various V_{PASS} values can be obtained, as shown in Figure 8, assuming that R_P =R_{PM} =R_{PX}, V_{DPUM} =5.5V.

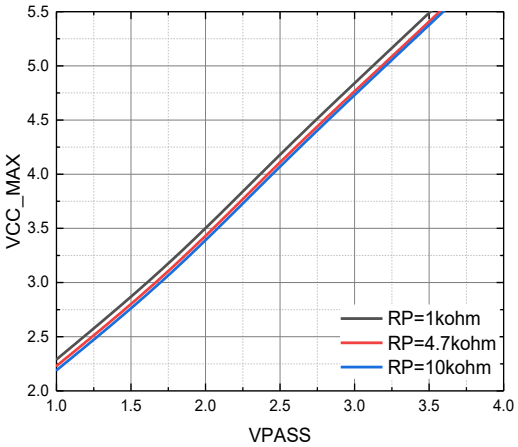


Figure 8 Relation Between Maximum VCC and V_{PASS} during Cross-Voltage Data Transmission

When low-level transmission is performed , the value of |SDA-SDX| mainly depends on the on-resistance R_{ON} of NM2 in Figure 7, as shown in Section 5.4 for details.

7 Detailed Application

NOTE

The following contents are the precautions and usage suggestions for FCA9548 in specific applications by NYFEA which does not make promises about its accuracy or completeness. Customers are responsible for determining suitability of components for their purposes based on their own usage needs and application scenarios. Customers should test and verify their design implementation to confirm system functionality and avoid losses.

The FCA9548 allows multiple downstream channels to be opened simultaneously by configuring the Control register. In this case, the I²C command sent by the upstream master will be transmitted to the downstream slave through each open channel, and special attention must be paid to the total current flowing through the SDA and SCL pins in this process, especially in the cross-voltage domain data transmission, and do not exceed the limit value specified in Section 5.1.

The FCA9548 allows the same I²C address for slaves on several downstream channels. When the upstream master sends a read command to a downstream slave of the same address, if the values in the read-to-read registers of these slaves are different, the values returned to the upstream master on the SDA bus will be conflicted, and the final value returned on the SDA bus is the result of the sum of the values in the registers of each slave (AND). In actual use, please evaluate the risk of use in this case in advance.

The FCA9548 allows the I²C address of the slave of the downstream channel to be the same as the address of the FCA9548 itself. However, this may lead to communication errors, so please evaluate the risks of use in this case in advance.

The FCA9548 is compatible with Standard-Mode, Fast-Mode, and Fast-Mode Plus in the I²C protocol, allowing the bus to operate up to 1MHz. When the chip is operating in these three different modes, the value of the pull-up resistor R_P on the SCL and SDA pins should meet the following conditions:

$$R_P(\min) = \frac{VCC - V_{OL}(\max)}{I_{OL}} \text{、} R_P(\max) = \frac{t_r}{(0.8473 \times C_b)}$$

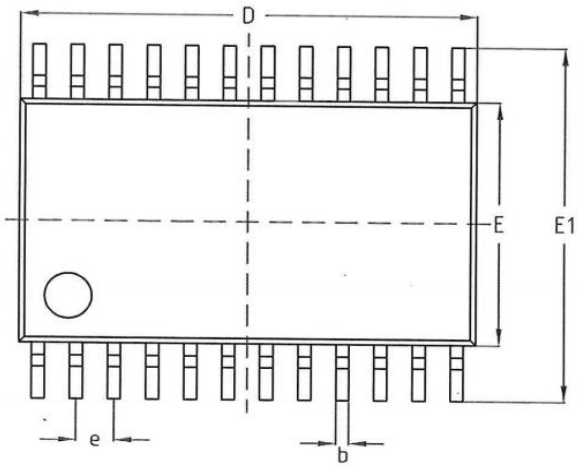
The specific indicators in the formula are detailed in sections 5.4 and section 5 .5.

In general usage scenarios, 4.7kohm is recommended for the R_P when the FCA9548 is operating in Standard-Mode and Fast-Mode (fSCL≤400kHz), and 500ohm is recommended for the R_P when the FCA9548 is operating in Fast-Mode Plus (400kHz≤ fSCL≤1000kHz). The user should determine the ideal R_P value based on the actual bus load and bus operating frequency to prevent errors in I²C communication.

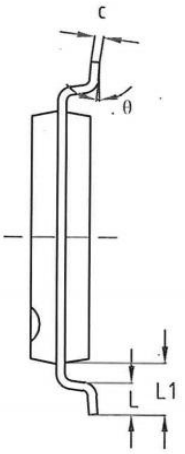
8 Package Informations

8.1 TSSOP-24

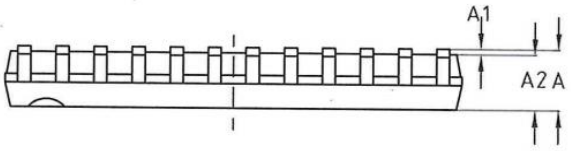
TOP VIEW
正视图



SIDE VIEW
侧视图



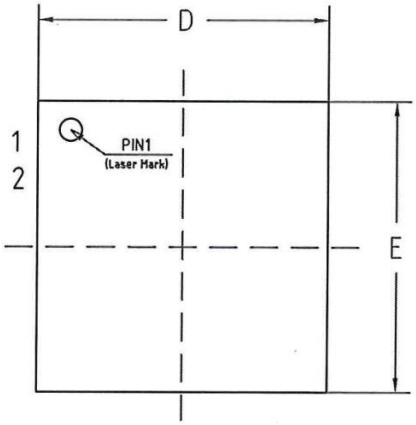
SIDE VIEW
侧视图



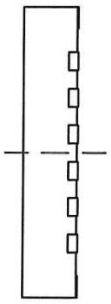
机械尺寸/mm Dimensions			
字符 SYMBOL	最小值 MIN	典型值 NOMINAL	最大值 MAX
A	–	–	1.20
A1	0.05	–	0.15
A2	0.80	1.00	1.05
b	0.19	–	0.30
c	0.09	–	0.20
D	7.70	7.80	7.90
E	4.30	4.40	4.50
E1	6.20	6.40	6.60
e	0.65 BSC		
L1	1.00 REF		
L	0.45	0.60	0.75
θ	0°	–	8°

8.2 QFN-24

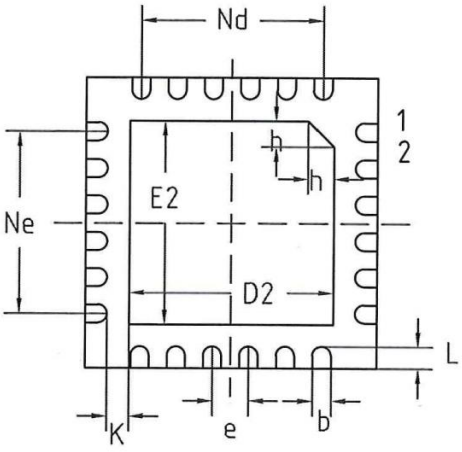
TOP VIEW
正视图



SIDE VIEW
侧视图



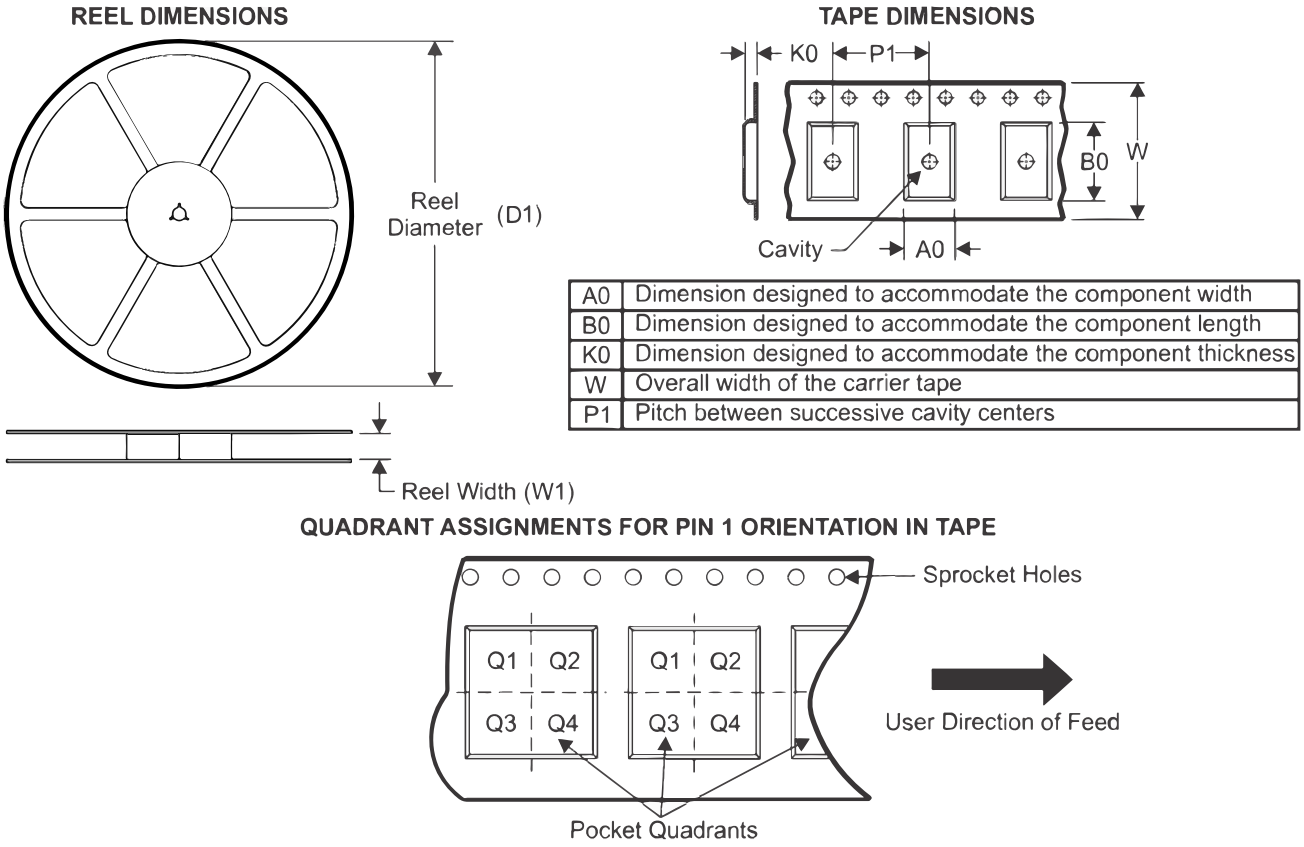
BOTTOM VIEW
背视图



SIDE VIEW
侧视图

机械尺寸/mm			
字符 SYMBOL	最小值 MIN	典型值 NOMINAL	最大值 MAX
A	0.45	0.50	0.55
A1	-	0.02	0.05
A2	0.127 REF		
b	0.2	0.25	0.30
D	3.90	4.00	4.10
D2	2.70	2.80	2.90
E	3.90	4.00	4.10
E2	2.70	2.80	2.90
e	0.50 BSC		
K	0.25	0.30	0.35
L	0.25	0.30	0.35
h	0.30	0.35	0.40
Ne	2.50 BSC		
Nd	2.50 BSC		

8.3 Reel and Tape Information



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

Package	D1 (mm)	W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 quadrant
TSSOP-24	330	16.40	6.95	8.30	1.60	8.00	16.00	Q1
QFN-24	330	12.40	4.30	4.30	1.00	8.00	12.00	Q2

9 Ordering Information

Order Number	Chip Model	Package	Standard Quantity	Note
FCA9548T-T&R	FCA9548T	TSSOP-24	4000	Tape & Reel
FCA9548Q-T&R	FCA9548Q	QFN-24	4000	Tape & Reel