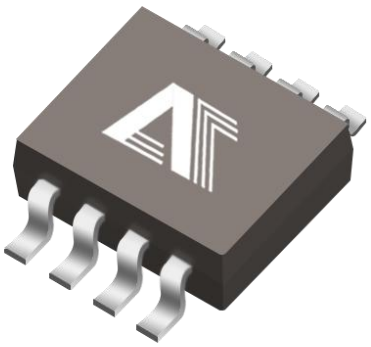
AOTE
SEMICONDUCTOR



Temperature sensor

DS18B20Z

Product Data Sheet

AOTE DCC
RELEASE

◆ Summary ：

The DS18B20 digital thermometer provides temperature measurement with a resolution of 9 to 12 bits, and can achieve lower and upper temperature limit alarms through programmable non-volatile storage units. DS18B20 uses a single bus protocol to communicate with the upper computer, requiring only one signal line and one ground line. Its temperature measurement range is -55C~+125 ℃ (-67T to+257T). The testing accuracy within the range of -10 ℃~70 ℃ can reach 0.4 ℃. In addition, it can also operate in parasitic mode, directly supplying power to the chip through signal lines without the need for additional power supply. Each DS18B20 has a globally unique 64 bit serial number, which allows multiple DS18B20s to be connected in series on the same single bus for networking. With just one processor, multiple DS18B20s distributed over a large area can be controlled. This networking method is particularly suitable for HVAC environmental control, building, equipment, grain temperature measurement, industrial temperature measurement, and process monitoring and control applications.

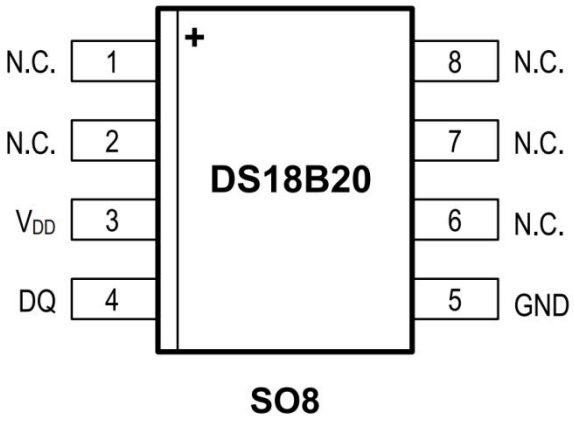
◆ Product features

- SOP8 package that can provide SMT
- Using a single bus interface, only one port pin is needed for communication
- Each chip has a globally unique 64 bit serial number
- Equipped with multi-point distributed temperature measurement function without the need for peripheral components
- Can be powered through a data cable; The power supply voltage range is 2.5V~5.5V
- The measurement range is -55℃to+125℃(-67℉to+257℉), with an accuracy of±0.4℉ within the range of -10℃to70℃
- Temperature resolution 9-12 bits optional
- At a maximum precision of 12 bits, the temperature conversion speed is less than 750ms
- Has user-defined non-volatile temperature alarm settings
- Alarm search command identifies and identifies devices that exceed the programmed temperature with super strong electrostatic protection capability: HBM8000VMM800V

◆ Applications

- Temperature control
- Industrial system
- Consumer goods
- Grain situation temperature measurement
- Thermometer
- Any thermal sensing system

◆ Pin Configuration



SO8

◆ Pin description

Pin position SOP8	name	effect
1，2，6，7，8	N.C.	Air traffic control feet or no need for connection
3	VDD	Power pins; In parasitic power supply mode, the VDD pin must be connected to ground
4	DQ	Data input/output pins; When in parasitic power supply mode, this pin supplies power to the chip (Please refer to the power instructions section of DS18B20)
5	GND	Grounding pin

◆ Details

Overview

The structural diagram of DS18B20 is shown in Figure 1. The chip uses a 64 bit read-only memory to store the unique chip serial number of the device. The internal register of the chip contains two byte temperature registers, which are used to store the data output by the temperature sensor. In addition, the chip also provides a byte temperature alarm threshold register (TH and TL) and a byte configuration register. The configuration register allows users to set the temperature measurement resolution to 9, 10, 11, or 12 bits.

TH, TL, and configuration registers are all non-volatile erasable registers (EEPROM), and the stored data will not disappear after the device is powered off. DS18B20 adopts a single bus protocol and communicates through a single wire port. When all devices are connected to the bus through a tri state port or open drain port, the control line needs to be connected to a weak pull-up resistor. In this bus system, the microprocessor (main device) identifies the devices on the bus and records the device addresses on the bus based on the 64 bit chip serial number unique to each device. Due to each device having a unique chip serial number, the number of devices that can be connected to the bus is actually infinite. Single bus protocol, including detailed explanation of instructions and "timing", can be found in the Single Bus System section.

Another function of DS18B20 is that it can operate without external power supply. When the bus is in a high level state, DQ is connected to the pull-up resistor to supply power to the device through a single bus. The bus signal that is simultaneously in a high-level state charges the internal capacitor (Cpp),When the bus is in a low level state, the capacitor provides energy to the device, and this way of providing energy becomes a "parasitic power source". Of course, DS18B20 can be powered by an external power source through the VDD pin.

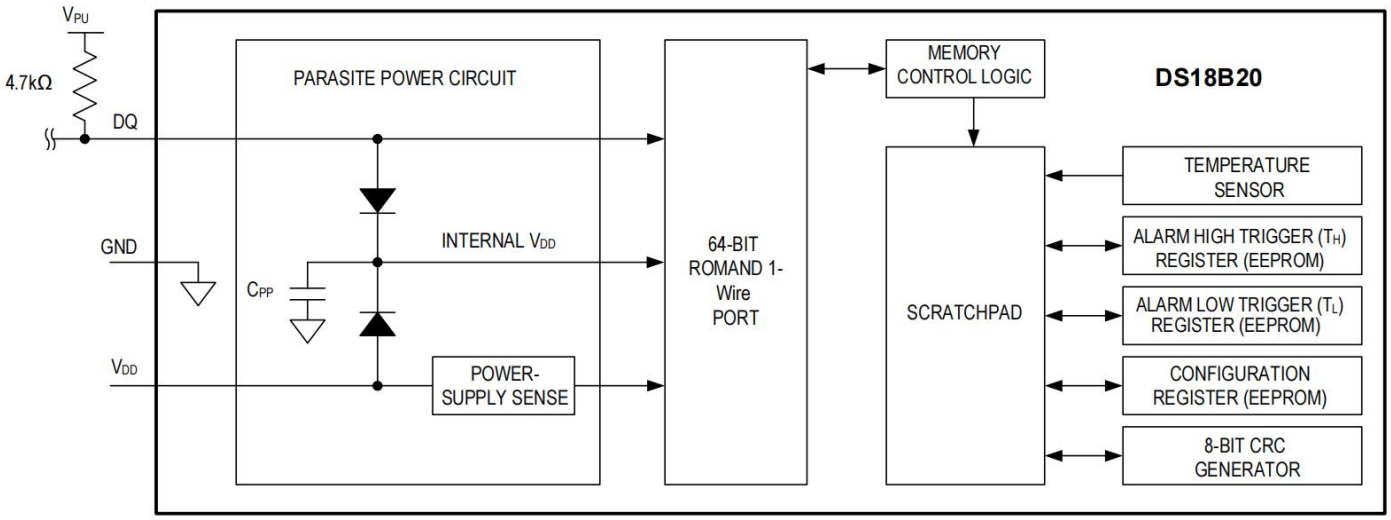


Figure 1 DS18B20 structural diagram

Temperature measurement operation

The core function of DS18B20 is its direct digital temperature sensor. The accuracy of the temperature sensor is user programmable with 9, 10, 11, or 12 bits. The temperature resolutions are 0.5, 0.25, 0.125, and 0.0625, respectively. The default precision of the chip is 12 bits when powered on. DS18B20 maintains a low-power waiting state after startup; When temperature measurement and AD conversion are required, the bus controller must issue a [44h] command. Afterwards, the generated temperature data is stored in the temperature register in the form of two bytes, and DS18B20 continues to remain in a waiting state. When DS18B20 is powered by an external power source, the bus controller initiates a "read timing" after the temperature conversion command (see Single Bus System section). DS18B20 returns 0 during temperature conversion and returns 1 after conversion is complete. If DS18B20 is powered by a parasitic power source, there will be no return value unless the bus is strongly pulled up during temperature conversion. The bus requirements for parasitic power sources are explained in detail in the DS18B20 power supply section.

	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
LS BYTE	2^3	2^2	2^1	2^0	2^{-1}	2^{-2}	2^{-3}	2^{-4}
	BIT 15	BIT 14	BIT 13	BIT 12	BIT 11	BIT 10	BIT 9	BIT 8
MS BYTE	S	S	S	S	S	2^6	2^5	2^4

Figure 2 Temperature Register Format Table

1. Temperature/data relationship

Temperature (°C)	Digital output (binary)	Digital output (hexadecimal)
+125	0000 0111 1101 0000	07D0h
+85	0000 0101 0101 0000	0550h
+25.0625	0000 0001 1001 0001	0191h
+10.125	0000 0000 1010 0010	00A2h
+0.5	0000 0000 0000 1000	0008h
0	0000 O000 OO00 OO00	0000h
-0.5	1111 1111 1111 1000	FFF8h
-10.125	1111 1111 0101 1110	FF5Eh
-25.0625	1111 1110 0110 1111	FE6Fh
-55	1111 1100 1001 0000	FC90h

* The default value of the temperature register during power on reset is+85 ℃

Alarm operation

After completing a temperature conversion, DS18B20 compares the temperature value with a ser-defined alarm threshold of one byte stored in the TH and TL registers (as shown in Figure 3). The flag (S) indicates the positive or negative temperature value: positive S=0, negative S=1. The Th and TL registers are non-volatile (EEPROM), so data is still retained after power failure. In the memory section, we will explain how Ti and TL are stored in the second and third bytes of the register.

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
S	2^6	2^5	2^4	2^3	2^2	2^1	2^0

Figure 3 T_H and T_L register formats

When TH and TL are 8-bit registers, only the 4 to 11 bits of the temperature register are applicable in comparison with TH and TL. If the measured temperature is higher than T or lower than Tt, the alarm condition is met, and an alarm indicator will be set inside DS18B20. This label is updated every time a temperature measurement is taken. Therefore, if the alarm state disappears, the indicator will be turned off after the next temperature transition.

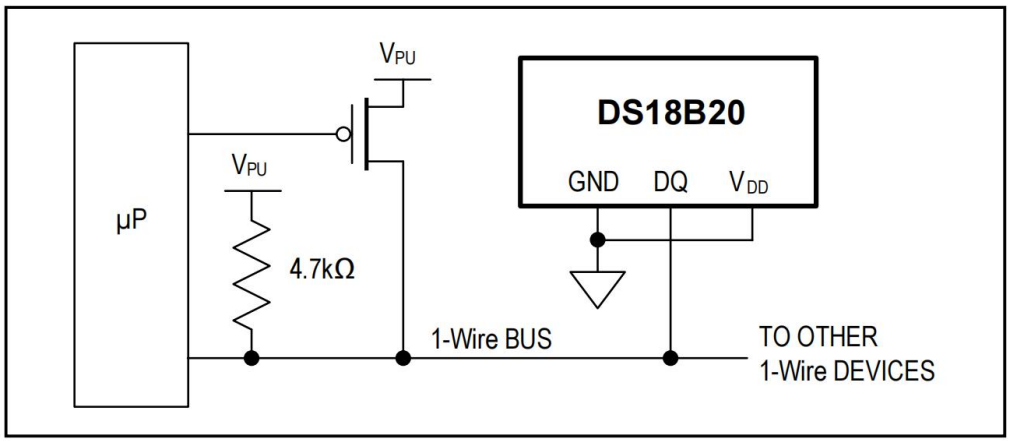
The bus controller detects all DS18B20 alarm identifiers on the bus by issuing an alarm search command [ECh]. Any DS18B20 that sets the alarm flag will respond to this command, so the bus controller can accurately locate every DS18B20 that meets the alarm conditions. If the alarm condition is met and the setting of TH or T has been changed, another temperature conversion will reconfirm the alarm condition.

◆ Power supply for DS18B20

DS18B20 can be powered by an external power supply through pin VDD or operate in parasitic power mode. In parasitic power mode, DS18B20 is allowed to operate in an external power demand state. Parasitic power mode is very useful in remote testing or space limited applications. The control circuit of the parasitic power supply is shown in Figure 1. When the bus is at a high level, the control circuit "steals" energy from the bus. Part of the 'stolen' energy is stored in parasitic power storage capacitors (Cpp), which are released to provide the device with energy when the bus is at a low level. When DS18B20 is in parasitic power mode, the VDD pin must be grounded.

In parasitic power mode, the single bus and CPP can provide sufficient current to meet the specified timing and voltage requirements (see DC and AC characteristics sections) to DS18B20 in most operations. However, when DS18B20 is performing temperature conversion or transferring data from registers to EEPROM, the operating current can reach up to 1.5mA. This current may cause unacceptable voltage drop due to weak pull-up resistors connected to a single bus, which requires a larger current that Cpp cannot provide. In order to ensure sufficient power supply for DS18B20, a strong pull-up must be provided to the single bus when performing temperature conversion or copying data to EEFORM operation, using MOSFET to directly pull the bus to the power supply, as shown in Figure 4. After issuing the temperature conversion instruction [44h] or copy register instruction [48h], the single bus must be converted to a strong pull-up within a maximum of 10us, and must remain in a strong pull-up state at the temperature conversion timing (tvonv) or copy data timing (ter=10ms). When the strong pull-up state is maintained, no other actions are allowed.

Figure 4 Power the DS18B20 for parasitic power supply during temperature conversion



Another method of supplying power to DS18B20 is the traditional approach of connecting an external power source from the VDD pin, as shown in Figure 5. The advantage of doing this is that there is no need for strong pull-up on a single bus, and the bus does not need to always maintain a high level during temperature conversion.

For temperatures above 100, it is not recommended to use parasitic power sources because DS18B20 exhibits high leakage current at such temperatures, which may prevent communication. At temperatures similar to this, it is strongly recommended to use the VDD pin of DS18B20 for power supply. For situations where the bus controller does not know whether the DS18B20 on the bus is using a parasitic power supply or an external power supply, the DS18B20 has prepared a signal indication power supply usage diagram. The bus controller issues a Skip ROM instruction [CCh], followed by a degree power instruction [B4h]. After this instruction is issued, the controller issues a read timing command. The parasitic power supply will pull the bus low, while the external power supply will keep the bus high. If the bus is pulled down, the bus controller will know to provide a strong pull-up to the single bus during temperature conversion.

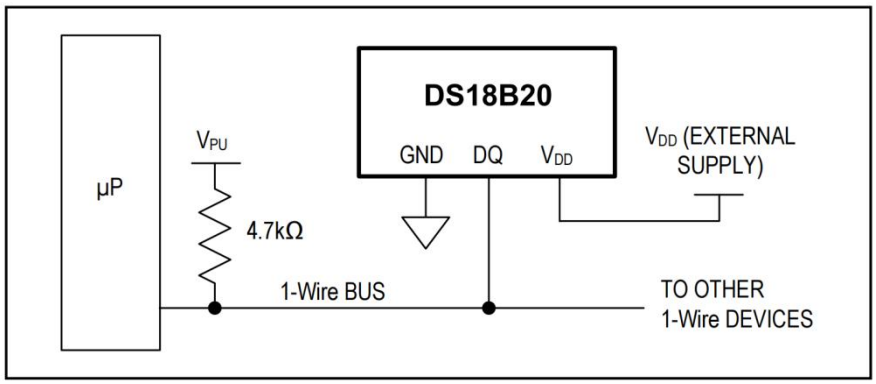


Figure 5 Use an external power source to supply power to DS18B20

◆ Storage

64 bit read-only memory

Each DS18B20 has a globally unique 64 bit encoding stored in ROM. The first 8 digits are the single line series code: 28h. The next 48 digits are a unique serial number. The last 8 bits are the CRC encoding of the above 56 bits. For a detailed explanation of CRC, please refer to the CRC Generator section. The 64 bit ROM and ROM operation control area allow DS18B20 to function as a single bus device and operate according to the single bus protocol detailed in the Single Bus System section.

8-BIT CRC	A8-BIT SERIAL NUMBER	B-BITFAAMLYCODE(28)
MSB LSB MSB	LSB MSB	LSB

Figure 6 64 bit ROM code

◆ Memory

The memory structure of DS18B20 is shown in Figure 7. The memory has a temporary memory SRAM and a non memory for storing draft alarm thresholds Th and T composed of volatile electrically erasable EEOROM. Note that when the alarm function cannot be used, Tn and T registers can be used as regular registers. All memory instructions are detailed in the DS18B20 functional instruction section.

The byte 0 and byte 1 of the memory are respectively the LSB and MSB of the temperature register, and these two bytes of memory are read-only memory. The second and third bytes are Tt and Tt. The fourth byte is the configuration register data, which is detailed in the configuration register section. The 5th byte is reserved by the device and writing is prohibited; The 6th and 7th bytes can be used by users.

The 8th byte of the memory is read-only and contains the CRC code for the above eight bytes. The CRC execution method is described in the CRC Generator section.

Data is written to bits 2, 3, 4, 6, and 7 of the memory through the write register instruction [4Eh]; The data must be transmitted starting from the second byte as the least significant bit. In order to fully verify data, the memory can be read after data is written (using the read register instruction [BEh]). When reading registers, data is moved out of the single bus with byte 0 as the least significant bit. When the bus controller transfers TH, TL, and configuration data from registers to EEPROM, it must issue a copy register instruction [48h].

The data stored in EEPROM memory remains intact even after the device is powered off; When powered on, data is loaded into the register. Data can also be loaded from registers into EEPROM through the recall EEPROM command. After issuing this command, the bus controller issues a read timing DS18B20 and returns 0 to indicate that the recall is in progress, and returns 1 to indicate that the operation has ended.

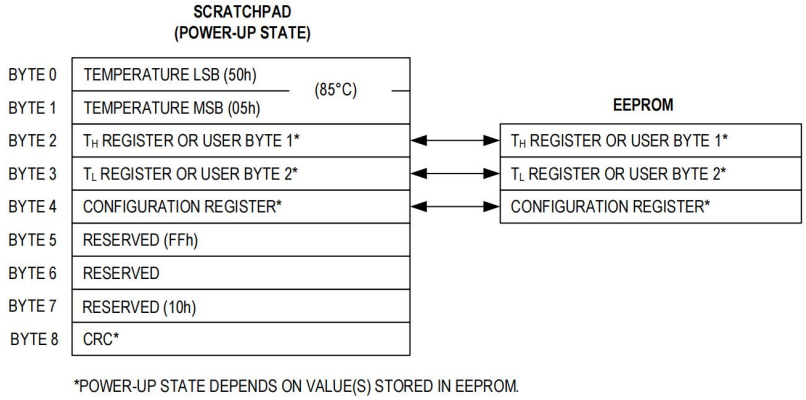


Figure 7. DS18B20 Memory Diagram

Configure registers

The fourth byte of the memory is the configuration register, whose structure is shown in Figure 8. Users can set the RO and R1 bits as shown in Table 2 The 0 precision of DS18B2. Default settings for power on: RO=1, R1=1 (1 bit 2 precision). Note: There is a direct relationship between accuracy and conversion time. Bit 7 and bits 0 to 4 of the configuration register are reserved by the device and writing is prohibited; When reading data, they all appear as logic 1.

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
0	R1	R0	1	1	1	1	1

Figure 8. Configuring registers

2. Sensor Accuracy Configuration Table

R1	R0	Resolution（BITS）	Maximum conversion time	
0	0	9	50ms	(tconv/8)
0	1	10	100ms	(tconv/4)
1	0	11	200ms	(tconv/2)
1	1	12	400ms	(tconv)

◆ CRC generator

CRC is stored in memory as part of DS18B2064 bit ROM. The CRC code is calculated from the first 56 bits of ROM and is included in the important bytes of ROM. CRC is calculated from the data stored in the memory, so when the data in the memory changes, the value of CRC also changes accordingly.

CRC can perform data verification when the bus controller reads DS18B20. In order to verify whether the data is read correctly, the bus controller must compare a CRC value calculated from the received data with the value stored in the 64 bit ROM of DS18B20 (when reading ROM) or the 8-bit CRC value calculated internally in DS18B20 (when reading registers). If the calculated CRC value matches the read CRC value, the data is transmitted error free. The comparison of CRC values and whether to proceed to the next step are entirely determined by the bus controller. When the value stored or calculated in DS18B20 does not match the value calculated by the bus controller, there is no circuit inside DS18B20 that can prevent the command sequence from proceeding. The calculation formula for CRC is as follows:

$$CRC=X^8+X^5+X^4+1$$

A single bus CRC can be generated by a polynomial generator consisting of a shift register and XOR gate, as shown in Figure 9. This circuit includes a shift register and several XOR gates, with each bit of the shift register initialized to 0. Starting from the least significant bit in ROM or the 0 byte of a register, move one bit at a time into the register. After transferring data from the 56 bit ROM or moving it into the highest bit of the 7th byte of the register, the shift register stores the CRC value. Next, the CRC value must be cyclically shifted in. At this point, if the calculated CRC is valid, the shift register will be reset to 0.

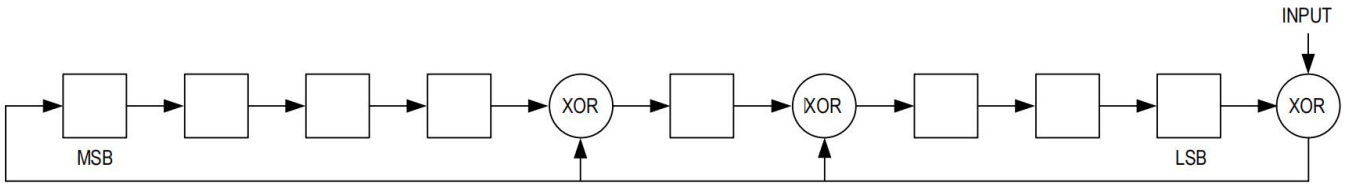


Figure 9 CRC generator

◆ Single bus system

A single bus system uses a single bus controller to control one or more slave devices. 6% always acts as a slave. When only one slave is connected to the bus, the system is called a "single point" system; If multiple slaves are connected to the bus, the system is called a "multi-point" system.

All data and instructions are transmitted through a single bus starting from the least significant bit. There are three aspects to discuss about single bus systems: hardware structure, execution sequence, and single bus signal type and timing.

◆ Hardware structure

A single bus system has only one defined signal line, and each device on the bus must have an open drain or tri state output. Each device master or slave on the bus must have an open drain or tri state output. This mechanism will cause every non transmitting device on the bus to release the bus for other devices to use. The single bus port pin is of the open drain type, and the internal equivalent circuit is shown in Figure 10. A single bus requires an external pull-up resistor of approximately; The idle state of the single bus is high level. If there is a need to pause a transmission for some reason and to resume the transmission, the bus must remain idle. During the recovery period, if a single bus is in an inactive high state, the recovery time between bits can be infinitely long. If the bus stays at a low level exceeding 480us, all devices on the bus will be reset.

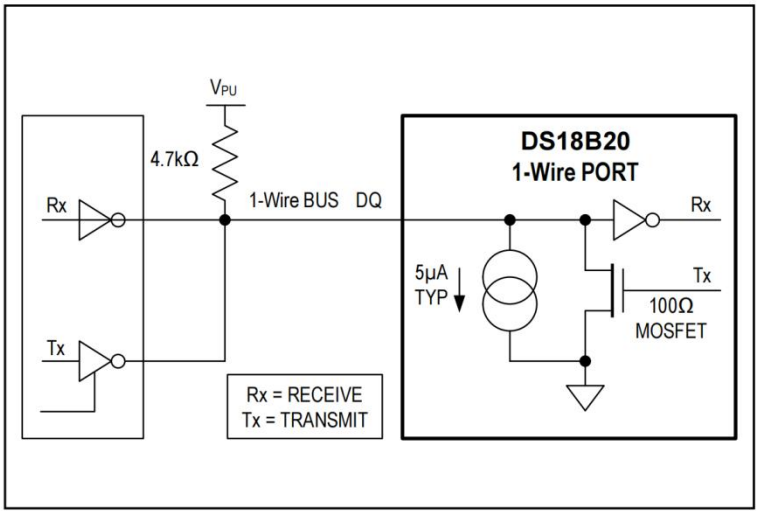


Figure 10. CRC Generator

◆ Execution sequence

The execution sequence for accessing DS18B20 through a single bus is as follows:
Step 1: Initialization
Step 2: ROM operation instructions
Step 3: DS18B20 Function Instruction
Every operation of DS18B20 must meet the above steps. If there are missing steps or the order is chaotic, the device will not have a return value. Excluding ROM search commands and alarm search commands. When these two commands are executed, the main controller must return to step 1.

Initialization

All execution operations through a single bus start from an initialization program sequence. The initialization sequence includes a reset pulse issued by the bus controller and a presence pulse subsequently issued by the slave. The presence of pulses informs the bus controller that DS18B20 is on the bus and ready for operation, as detailed in the bus signal section.

ROM Instruction

Once the bus controller detects the presence of a pulse, it issues a ROM instruction. If there are multiple DS18B20s hanging on the bus, these instructions will give the device a unique 64 bit ROM serial code, allowing the bus controller to select the specific device to be operated on. These instructions can also enable the bus controller to identify how many and what types of devices are hanging on the bus, and they can also identify which devices have met the alarm conditions. There are 5 ROM instructions, all of which are 8-bit in length. The bus controller issues a ROM instruction before initiating a DS18B20 function instruction. The ROM instruction operation diagram is shown in Figure 11.

SEARCH ROM[FOh]

When the system is powered on and initialized, the bus controller must identify all ROM serial codes on the bus to obtain the number and model of slaves. The bus controller searches the ROM code multiple times by searching for ROM instructions to confirm all slave components. If there is only one slave on the bus, a simpler read ROM instruction (see below) can be used instead of a search ROM instruction. After each ROM instruction search, the bus controller must return to step 1 (initialization).

READ ROM[33h]

This command can only be used when there is a single DS18B20 on the system. This command allows the bus controller to read the 64 bit serial code of the slave without using the Search ROM instruction. If there are more than one slave on the bus and this command is used, data conflicts will occur when all slaves attempt to transmit signals simultaneously.

MATCH ROM [55h]

The MATCH ROM instruction is followed by a 64 bit ROM serial number, and the bus controller locates a specific slave device on the multi-point bus. Only DS18B20 that exactly matches the 64 bit ROM serial number can respond to subsequent memory operation instructions; All slaves with serial numbers that do not match the 64ROM will wait for a reset pulse.

SKIP ROM[CCh]

This command allows the bus controller to use functional instructions without providing 64 bit ROM encoding. For example, the bus controller can first issue a ignore ROM instruction and then issue a temperature conversion instruction [44h] to complete the temperature conversion operation. Note: When there is only one slave on the bus, regardless, ignoring the ROM instruction can only be followed by issuing a read register instruction [BEh]. When using this command on a single point bus, the device does not need to send back 64 ROM codes, saving time. If there is more than one slave on the bus and a ignore ROM instruction is issued, data conflicts will occur on the bus due to multiple slaves transmitting data simultaneously.

ALARMSEARCH[ECh]

The operation process of this instruction is the same as that of the search ROM instruction, and only slave machines that meet the alarm conditions will respond to this command. This command allows the master device to determine if any DS18B20 experienced an alarm state during the most recent temperature transition. After each alarm search instruction cycle, the bus controller must return to step 1. For the alarm operation process, please refer to the alarm signal operation section.

DS18B20 functional instruction

After the bus controller uses ROM commands to determine the DS18B20 it wishes to communicate with, the host can issue a DS18B20 functional instruction. These instructions allow the bus controller to read and write registers of DS18B20, initiate temperature conversion, and recognize power mode. The functional instructions of DS18B20 are detailed in the following text, summarized in Table 4, and illustrated in Figure 12 using a flowchart.

CONVERTT[44h]

This command is used to initiate a temperature conversion. After the temperature conversion instruction is executed, the temperature conversion result data generated is stored in the temperature register in the form of 2 bytes, and then DS18B20 remains in a low-power waiting state. If this command is issued in parasitic power supply mode, during the temperature conversion period (tCONV), a strong pull-up must be applied to the single bus within 10us (maximum), as shown in the DS18B20 power supply section. If DS18B20 is powered by an external power source, the bus controller will issue a read timing after issuing the command. If DS18B20 is in the process of conversion, the bus will return 0, and if the temperature conversion is complete, it will return 1. In parasitic power supply mode, this communication method will not be used until the bus is forcefully pulled up.

WRITESCRATCHPAD[4Eh]

This command writes data to the register of DS18B20, starting from the TH register (2nd byte of the register), then writing to the TL register (3rd byte of the register), and finally writing to the configuration register (4th byte of the register). The data is transmitted starting from the least significant bit. The writing of the above three bytes must occur before the bus controller issues a reset command, otherwise a data conflict may occur.

READSCRATCHPAD[BEh]

This command is the host read register command. Reading will start from the least significant bit of byte 0 and continue until the 9th byte (byte 8, CRC) is read. If you do not want to read all bytes, the controller can issue a reset command at any time to abort the reading.

COPYSCRATCHPAD[48h]

This command copies the contents of Th, T, and configuration registers (bytes 2, 3, 4) to EEPROM. If using a parasitic power bus controller, a strong pull-up must be initiated within 10 microseconds of issuing this command and maintained for at least 10 ms, as described in the DS18B20 power supply section.

RECALLE² [B8h]

This command copies TH, TL, and configured data from EEPROM back to registers. After issuing the command, the bus controller sends a read timing, and DS18B20 will output a copy back flag: 0 indicates that copying is in progress, and 1 indicates that copying is complete. This operation is automatically executed when DS18B20 is powered on, so that valid data immediately exists in the register as soon as the device is powered on.

READPOWER SUPPLY [B4h]

After this command is sent to DS18B20, the bus controller issues a read timing. If it is in parasitic power mode, DS18B20 will pull down the bus; If in external power mode, DS18B20 will pull the bus high. The usage information of this instruction is detailed in the DS18B20 power supply section.

3. DS18B20 Function Instruction List

Command	Description	Agreement	1-Wire bus activity after issuing command ACTIVITIVE	Note
TEMPERATURE CONVERSION COMMANDS				
Convert T	Start temperature conversion	44h	DS18B20 transfers the transition state to the host (not applicable to DS18B20 with parasitic power supply)	1
MEMORYCOMMANDS				
Read Scratchpad	Read the entire register including CRC bytes	BEh	DS18B20 sends up to 9 data bytes to the host	2
Write Scratchpad	Write data to registers bytes 2, 3, 4 and 6, 7 (TH, TL, configuration register, and user byte)	4Eh	The host sends 3, 4, or 5 data bytes to DS18B20	3
Copy Scratchpad	Copy TH, TL, configuration registers, and user byte data from registers to EEPROM	48h	None	1
Recall E2	Call TH, TL, configuration registers, and user byte data from EEPROM to registers.	B8h	DS18B20 will transmit the call status to the host	
Read Power Supply	Send DS18B20 power mode signal to the host	B4h	DS18B20 transmits the power status to the host	

Note 1: For DS18B20 to be enabled during temperature conversion and copying data to EEPROM in parasitic power mode, a strong pull-up must be applied to the single bus, and there should be no other activity on the bus during this period.

Note 2: The bus controller can terminate data transmission at any time by issuing a reset signal.

Note 3: The writing of the three bytes TH, TL, and configuration register must be done before the reset signal is initiated.

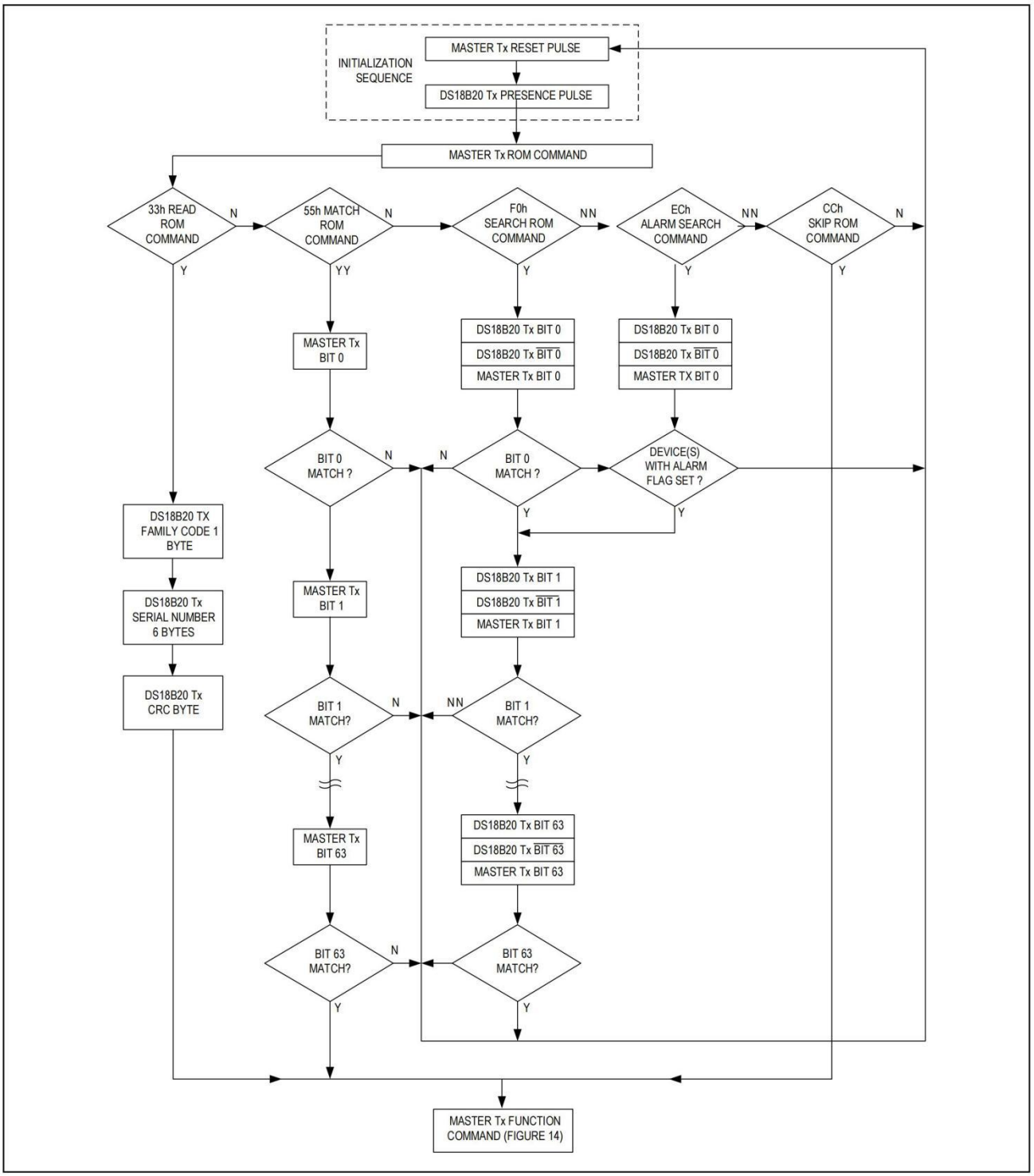


Figure 11. ROM Instruction Flow Chart

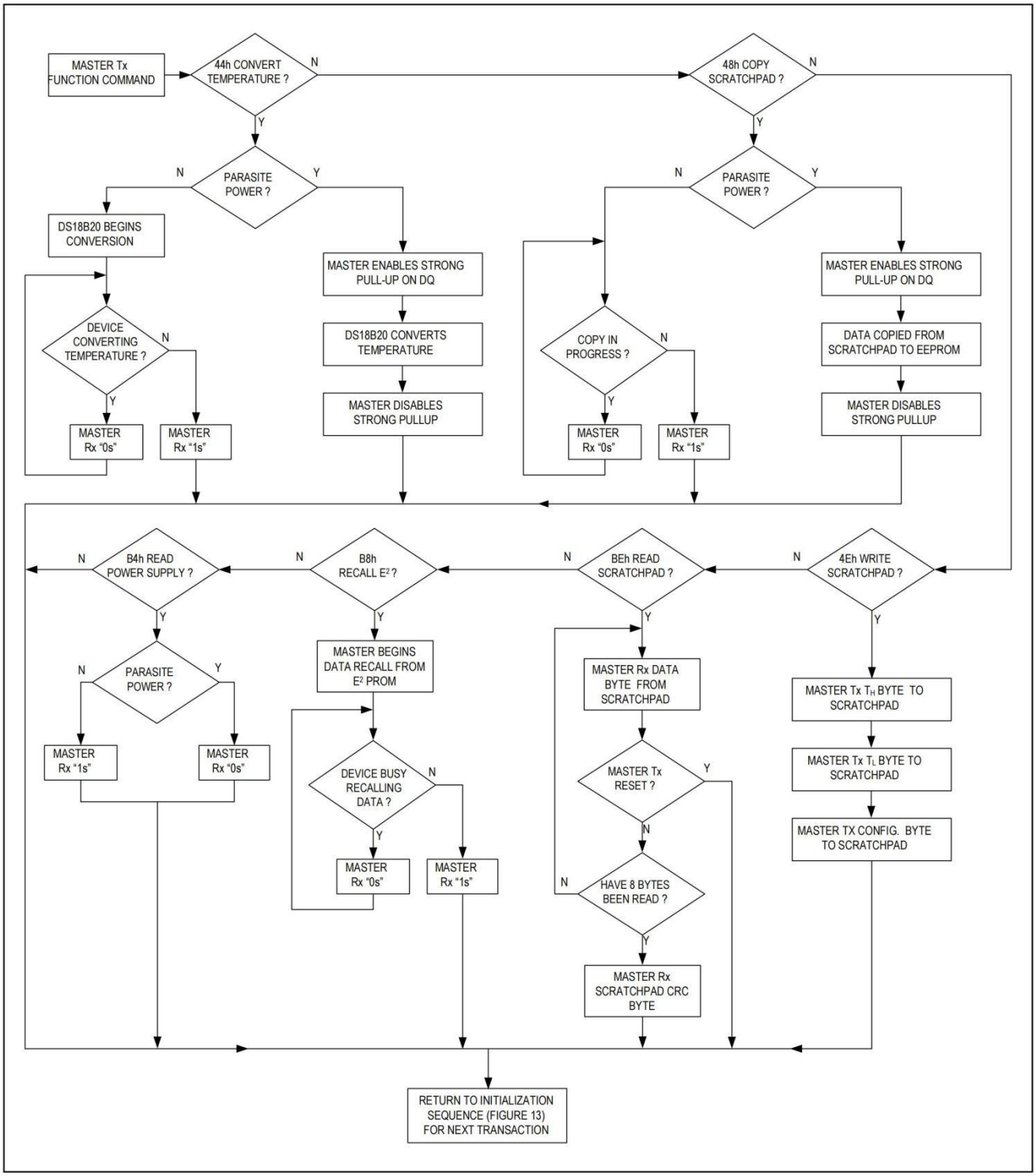


Figure 12. DS18B20 Function Instruction Flow Chart

Single bus signal

DS18B20 requires a strict single bus protocol to ensure data integrity. The protocol defines several types of single bus signals: reset pulse, presence pulse, write 0, write 1, read 0, and read 1. All of these signals, except for the presence pulse, are emitted by the bus controller.

Reset sequence: reset and presence pulse

All communication with DS18B20 starts with an initialization sequence, as shown in Figure 13. A reset pulse followed by a presence pulse indicates that DS18B20 is ready to send and receive data.

During the initialization sequence, the bus controller pulls down the bus and maintains it at 480us to issue a reset pulse signal (TX), then releases the bus and enters the receive state (RX). After the bus is released, the 5kQ pull-up resistor pulls the bus to a high level. When DS18B20 detects the rising edge on the IO pin, it waits for 15-60us and then emits a presence pulse consisting of a low level signal of 60-240us.

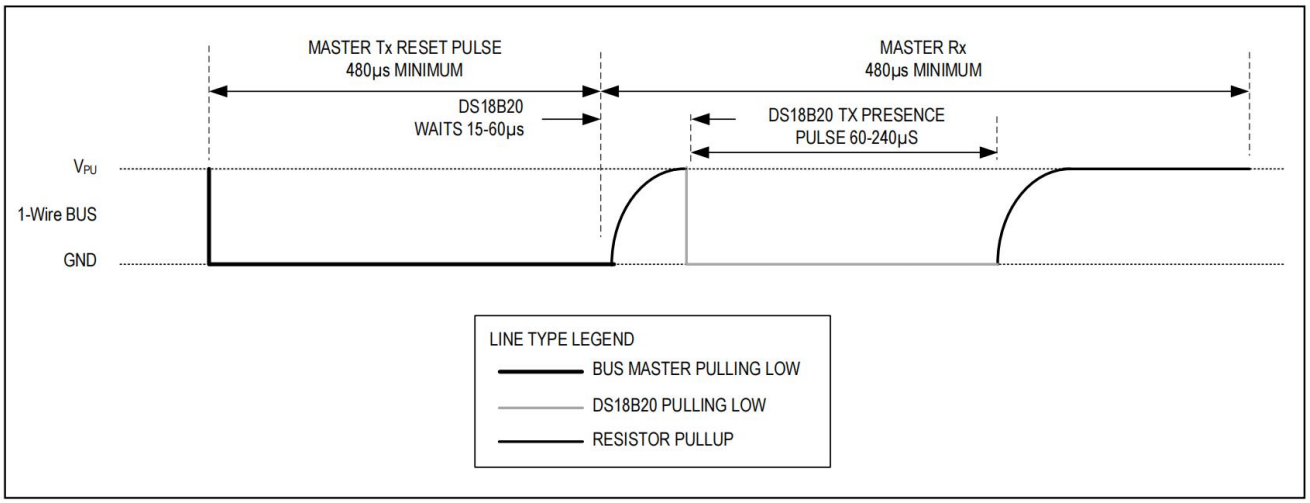


Figure 13. Initialization sequence

Read/Write Timing

The data reading and writing of DS18B20 is carried out through timing processing for information exchange, with 1 bit of data transmitted at each timing.

Write Timing

DS18B20 has two types of write timing: write 1 timing and write 0 timing. The bus controller writes logic 1 by writing 1 timing sequence; Write logical 0 by writing 0 sequence. The write timing must last for at least 60us, including a recovery time of at least 1us between two write cycles. When the bus controller pulls the data line from logic high level to low level, the write timing starts (see Figure 14).

To generate a write timing for the bus controller, the data line must be pulled to a low level and then released, and the bus must be released within 15 microseconds.

After the bus is released, the pull-up resistor pulls the bus high. To generate write 0 timing, the bus controller must pull the data line to a low level and maintain it for at least 60us.

After the bus controller initializes the write timing, DS18B20 uses signal lines within a window of 15us to 60us. If the line is at a high level, write 1. On the contrary, if the line is at a low level, it means writing 0.

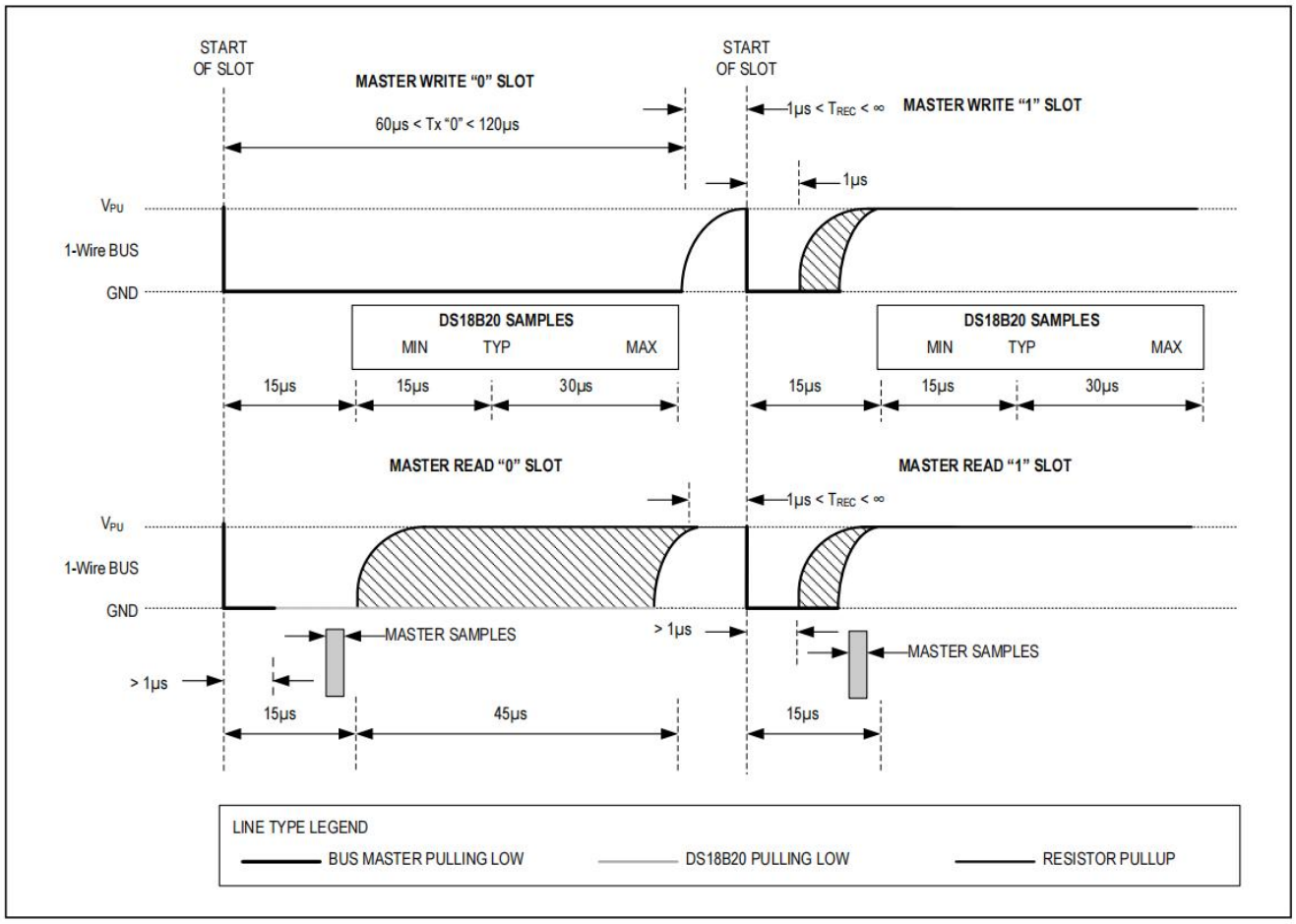


Figure 14. Timing diagram of read/write time slots

Read timing sequence

When the bus controller initiates a read timing, DS18B20 is only used to transmit data to the controller. Therefore, the bus controller must immediately start reading timing after issuing the read register instruction [BEh] or read power mode instruction [B4h] in order for DS18B20 to provide the requested data. In addition, the bus controller reads the timing after issuing the temperature conversion instruction [44h] or recalling the EEPROM instruction [B8h], as detailed in the DS18B20 functional instruction section.

All read timing must be at least 60us, including a recovery time of at least 1us during two read cycles. When the bus control pulls the data line from high level to low level, the read timing starts, and the data line must maintain at least 1us before the bus is released (see Figure 14). After the bus controller issues a read timing, DS18B20 pulls up or down the bus to transmit 1 or 0. After the transmission of O is completed, the bus will be released and return to a high-level idle state through a pull-up resistor. The data output from DS18B20 is valid for 15 microseconds after the falling edge of the read timing occurs. Therefore, the bus controller releases the bus within 15 microseconds of the start of the read timing and samples the bus state to read the status of the data line.

Figure 15 indicates that the sum of TNr, Tgc, and Ts MPLE must be less than 15us. Figure 16 suggests that the system time can be maximized by keeping Twr and Tgc as short as possible and placing the controller sampling time at the end of the 15us cycle.

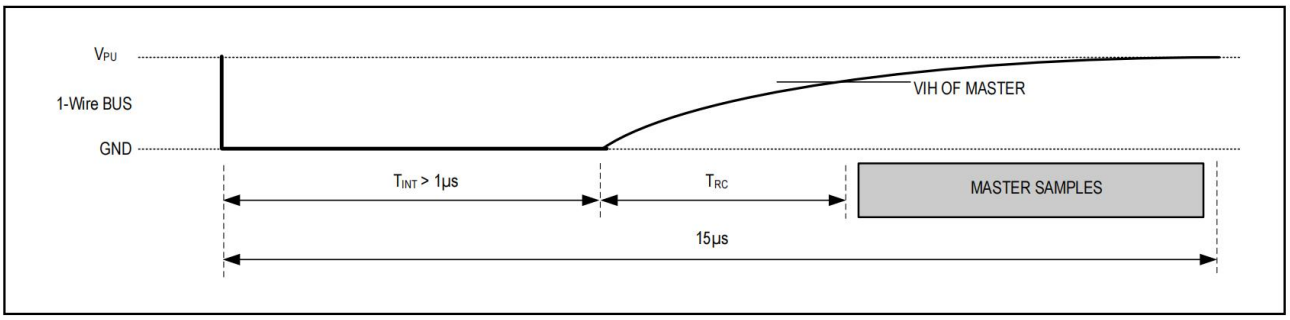


Figure 15. Detailed timing sequence of controller reading 1

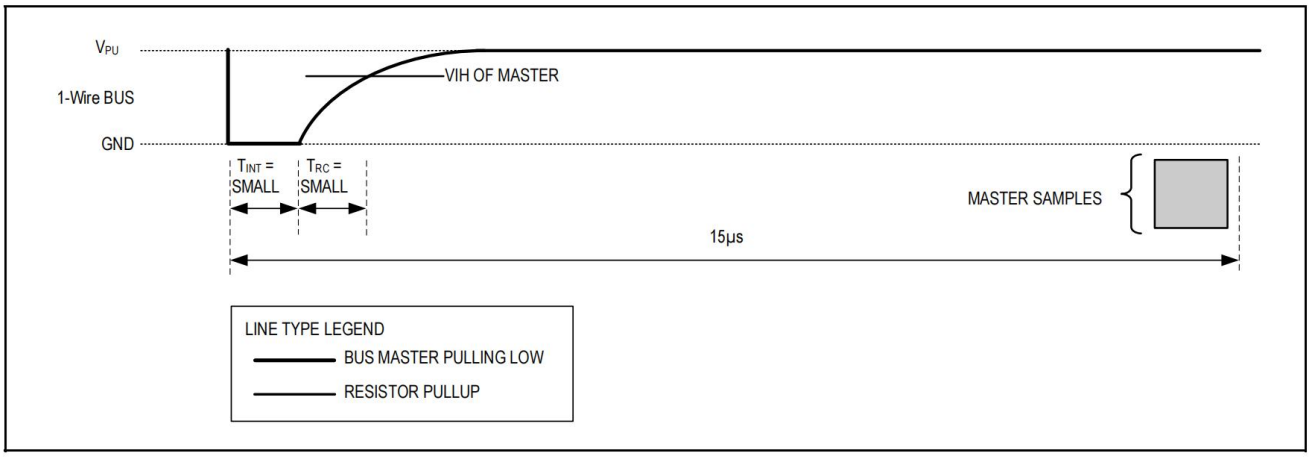


Figure 16. Recommended control read 1 timing sequence

◆ Example of DS18B20 Operation

Example 1

In this example, there are multiple DS18B20 buses on the bus that are powered by parasitic power sources. The bus controller starts temperature conversion on a specific DS18B20, then reads its registers and recalculates the CRC to confirm the data.

MASTER MODE	DATA(LSB FIRST)	COMMENTS
Tx	Reset	The controller sends a reset pulse
Rx	Presence	DS18B20s returns pulse presence
Tx	55h	The main controller sends matching ROM instructions
Tx	64-bit ROM code	The main controller sends DS18B20 address
Tx	44h	The main controller sends temperature conversion instructions
Tx	DQ line held high by strong pull up	DQ signal maintains high level for at least 500ms, temperature conversion has been completed
Tx	Reset	Reset pulse
Rx	Presence	DS18B20s returns pulse presence
Tx	55h	The main controller sends matching ROM instructions
Tx	64-bit ROM code	The main controller sends DS18B20 address
Tx	BEh	Main control sends and reads register instructions
Rx	9 data bytes	Read the entire register and add CRC: The controller recalculates the CRC of the 8 data bytes read from the register, compares the calculated CRC with the read CRC, and if they are the same, the controller proceeds downwards; If they are different, operate again

Example 2

In this example, there is only one parasitic power supply on the bus for DS18B20. The controller writes TH, TL, and configuration registers, then reads the registers and calculates CRC to verify the data. The main controller then copies the data in the registers to the EEPROM.

MASTER MODE	DATA(LSB FIRST)	COMMENTS
Tx	Reset	Reset pulse
Rx	Presence	DS18B20 returns pulse presence
Tx	CCh	Skip ROM instruction
Tx	4Eh	Write register instruction
Tx	3 data bytes	Write 3 data to Th, TL, and configuration registers
Tx	Reset	Reset pulse
Rx	Presence	DS18B20 returns pulse presence
Tx	CCh	Skip ROM instruction
Tx	BEh	Read register instruction
Rx	9 data bytes	The main controller reads all registers, including the CRC: The controller recalculates the CRC of the 8 bytes read from the registers, compares the calculated CRC with the read CRC, and if they are the same, the controller proceeds downwards; If they are different, repeat the read operation.
Tx	Peset	Reset pulse
Rx	Presence	DS18B20 returns pulse presence
Tx	CCh	Skip ROM instructions
Tx	48h	Copy Register Instruction
Tx	)Q line held high by strong pullup	The controller applies a strong pull-up to DQ during the copy operation and maintains it for at least 10ms

◆ Extreme usage conditions

Voltage range of each pin to ground: -0.5V to+6.0V

The operating temperature range: -55 ℃ to+125 ℃

The storage range : -55 ℃ to+125 ℃

Welding temperature range: Refer to STD-020A rule

The above points out the environmental conditions required for the device to operate normally, and long-term operation under extreme conditions may affect the reliability of the device.

◆ DC characteristics

Parameter	Symbol	Conditions	Min	Typ	Max	Unit	Note
power supply voltage	V_{DD}	Local power supply	+2.5		+5.5	V	1
Pull up power supply voltage	V_{PU}	Parasite Power	+2.5		+5.5	V	1,2
		Local power supply	+2.5		V_{DD}		
temperature error	t_{ERR}	-10℃~+85℃			±0.4	℃	3
		-55℃~+1245℃			±1.2		
Input logic low level	V_{IL}		-0.3		+0.8	V	1,4,5
Input logic high level	V_{IH}	Local power supply	+2.2		The lower of 5.5 and VDD+0.3	V	1,6
		Parasite Power	+2.5				
Inject current	I_L	$V_{I/O}$=0.4V	4.0			mA	1
standby current	I_{DDS}			750	1000	nA	7,8
operating current	I_{DD}	V_{DD}=5V		1	1.5	mA	9
DQ input current	I_{DQ}			5		μA	10
drift				±0.2		℃	11

Note:

1) All voltages are based on the ground potential as the reference potential.

2) The pull-up voltage is obtained as follows: assuming the pull-up device is perfect, the pull-up high ceiling should be equal to the VPU. In order to meet the VIH specification of DS18B20, the actual transistor pull-up power supply must include the limit of voltage drop; Therefore $V_{PU\_ACTUAL}=V_{PU\_IDEAL}+V_{TRANSISTOR}$.

3) The typical curve is shown in Figure 17.

4) The logic 0 level is obtained when the absorbed current is 4mA.

5) In the parasitic power mode, in the low voltage state, in order to ensure the presence of pulse V_{ILMAX}, it may be necessary to reduce it to 0.5V.

6) Logic 1 voltage is obtained when the source current is 1mA.

7) The standby current is defined at 70 hours; The typical standby current value at 125 hours is 3uA.

8) To reduce I_{DDS}, the range of DQ is as follows: GNDDQGND+0.3V or V_{DD}-0.3VDQV_{DD}.

9) Dynamic current involves temperature conversion and writing to EEPROM memory.

10) The DQ data line is in a (High resistance state).

11) The drift of the data was obtained after testing for 1000 hours at+125 power supply voltage VDD=5.5V.

◆ Communication characteristics

Non volatile memory (-55 ℃ to+100 ℃); VDD=2.5V to 5.5V)

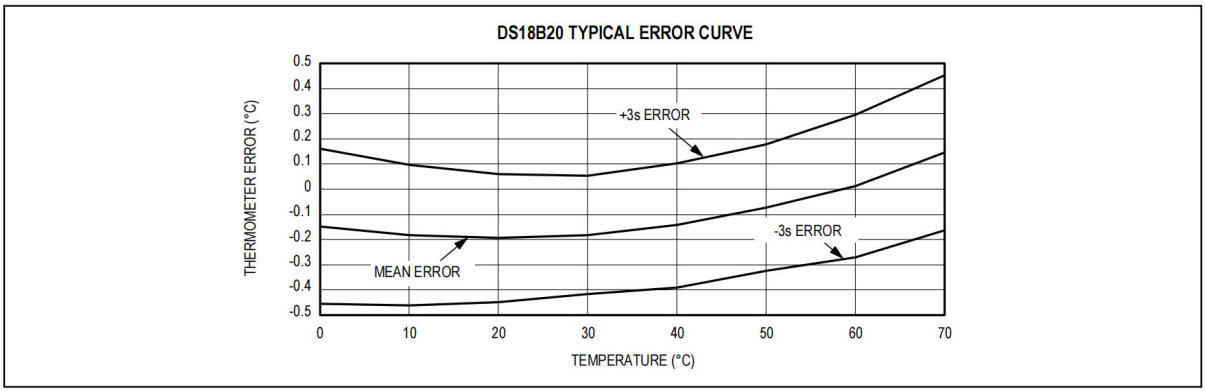
Parameter	Symbol	Conditions	Min	Typ	Max	Unit
NV Write Cycle Time	t_{WR}			8	12	ms
EEPROM Writes	N_{EEWR}	-55℃ to +55℃	1000			writes
EEPROM Data Retention	t_{EEDR}	-55℃ to +55℃	10			years

(-55℃ to +100℃;VDD=2.5V to 5.5V)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit	Note
Temperature Conversion Time	t_{CONV}	9-bit resolution			50	ms	1
		10-bit resolution			100		
		11-bit resolution			200		
		12-bit resolution			400		
Time to Strong Pullup On	t_{SPON}	Start Convert T Command Issued			10	μs	
Time Slot	t_{SLOT}		60		120	μs	1
Recovery Time	t_{REC}		1			μs	1
Write 0 Low Time	t_{LOW0}		60		120	μs	1
Write 1 Low Time	t_{LOW1}		1		15	μs	1
Read Data Valid	t_{RDV}				15	μs	1
Reset Time High	t_{RSTH}		480			μs	1
Reset Time Low	t_{RSTL}		1			μs	1
Presence-Detect High	t_{PDHIGH}		15		60	μs	1
Presence-Detect Low	t_{PDLOW}		60		240	μs	1
Capacitance	$C_{IN/OUT}$				25	pF	

Note:

1) The typical characteristic curve is shown in Figure 17



z

2) Please refer to Figure 18 for the timing sequence.

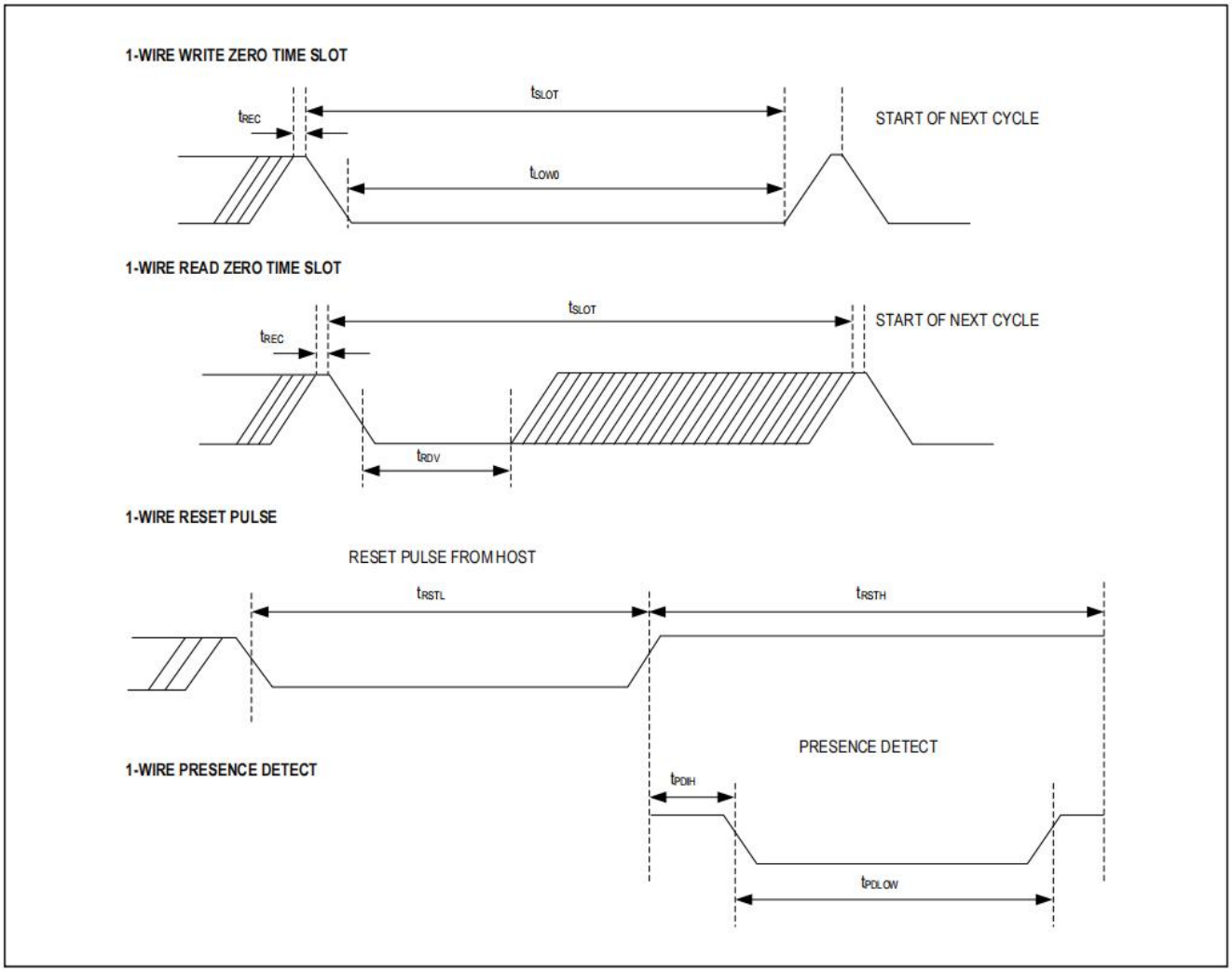


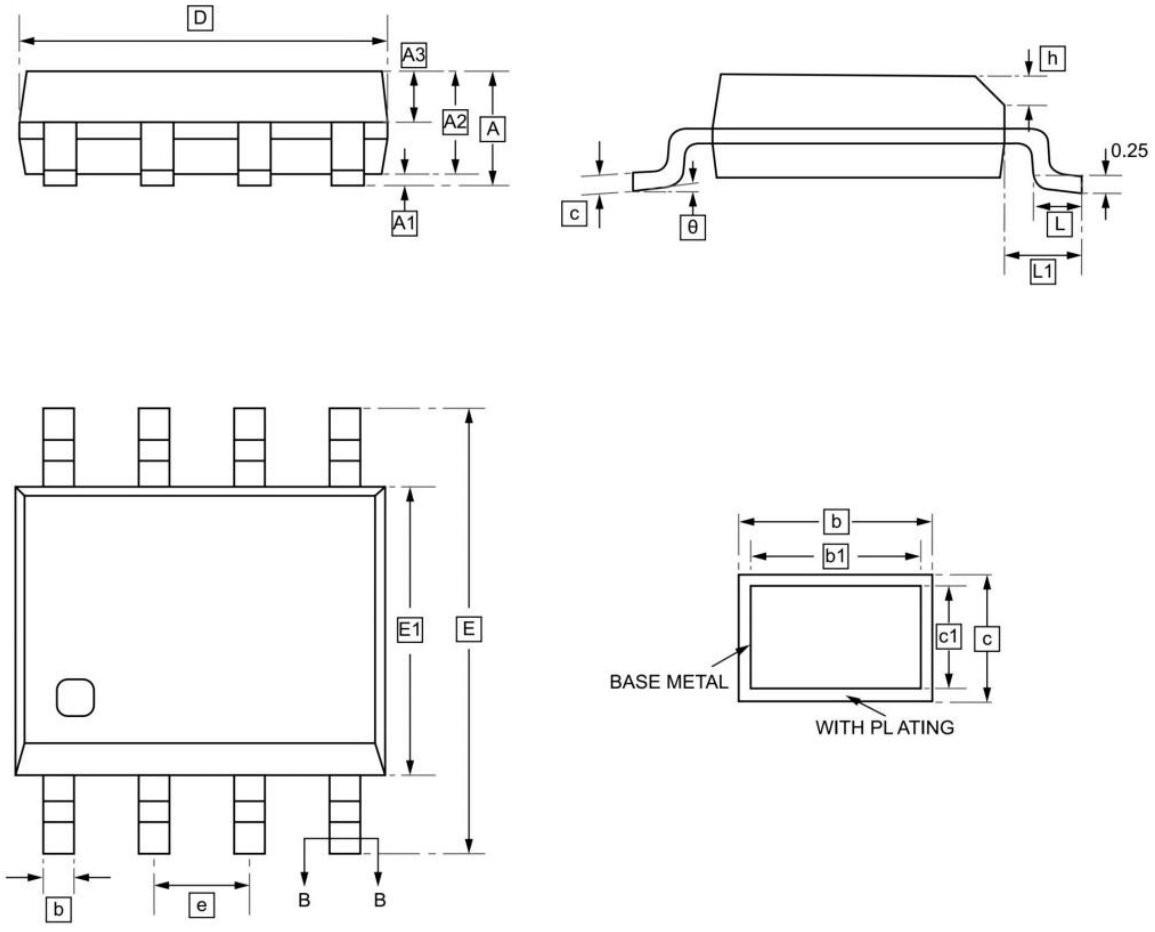
Figure 18. Timing

◆ List of Product Packaging Models

Model	Package form	Accuracy
DS18B20Z	SOP8	±0.5℃

◆ Package size

1) DS18B20Z SOP8 package



Symbol	A	A1	A2	A3	b	b1	c	c1	D	E	E1	E
Min	-	0.10	1.30	0.60	0.39	0.20	0.20	0.19	4.80	5.80	3.80	1.27 BSC
Max	1.75	0.225	1.50	0.70	0.47	0.24	0.21	0.21	5.00	6.20	4.00	

Symbol	h	L	L1	θ
Min	0.25	0.50	1.05 REF	0°
Max	0.50	0.80		8°

◆ Attention

- AOTE implements dynamic technical updates. Specifications are subject to change. Refer to the official website for the latest version.
- Users must strictly adhere to specified conditions. Failures caused by misuse (overload, high temperature, incompatible circuits) are excluded from warranty.
- Contact technical support for customized validation in critical applications (medical devices, industrial control).
- This document is valid until December 31, 2026. Updates will be notified on the official website.
- For further clarification on technical specifications or application solutions, please contact us through official channels: