3.8V-40V, 3.5A Synchronous Step-Down DCDC Converter With Ultra-Low IQ

1 FEATURES

- Wide Input Range: 3.8V-40V
- Up to 3.5A Continuous Output Current
- 0.8V ± 1% Feedback Reference Voltage
- Integrated 80mΩ High-Side Power MOSFET and 50mΩ Low-Side Power MOSFET
- Adjustable Frequency 300kHz to 2.2MHz
- Pulse Skipping Mode (PSM) at Light Load
- 25uA Quiescent Current in Sleep Mode
- Programmable Soft-Start Time
- Frequency Spread Spectrum (FSS) Modulation for EMI Reduction
- External Clock Synchronization
- Available in an eSOP-8L Package

2 APPLICATIONS

- USB Type-C PD and USB Charging
- Battery Powered System - Drone, GPS Tracker etc.
- Automotive System
- Medical Power System
- 12-V, 24-V, Industry Power System

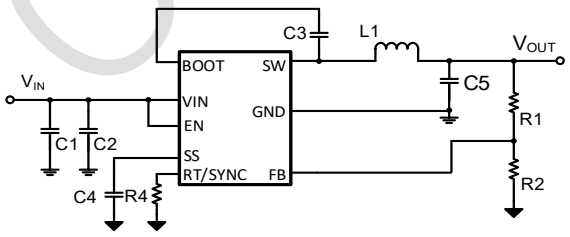
3 ORDERING INFORMATION

TYPE	MARKING	PACKAGE
GBI8432SMAR	8432	eSOP-8

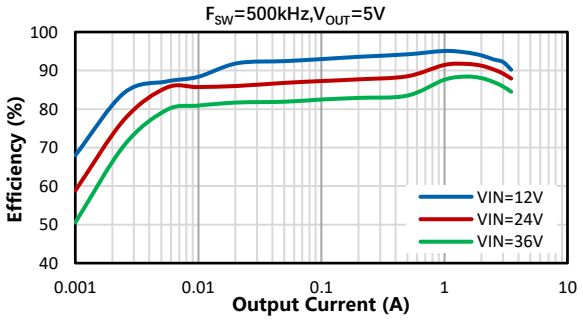
4 DISCRIPTION

The GBI8432 is a 3.8V-40V input, 3.5A buck converter with an integrated 80mΩ high-side and 50mΩ low-side MOSFET. The GBI8432 adopts peak current mode and supports a 300kHz-2.2MHz adjustable switching frequency range, setting by external resistor. The ULQ control makes quiescent current is 25uA in sleep mode and the shutdown current is 1uA, making it suitable for battery-powered system. The device integrates protections like cycle-by-cycle current limit, thermal shutdown, output over-voltage, over-temperature, input over and under-voltage protections and Hiccup when output short. It has the frequency spread spectrum (FSS) feature for EMI reduction. It' s available in an 8-pin eSOP-8L package.

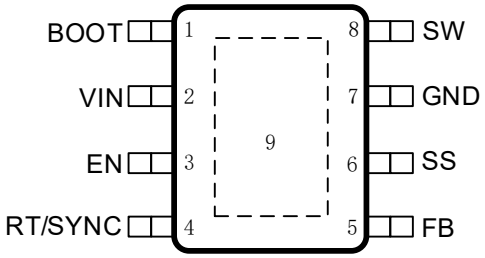
5 TYPICAL APPLICATIONS



Simplified Schematic



6 PIN CONFIGURATION AND FUNCTIONS



Top View: GBI8432 eSOP-8L

PIN OUT		I/O	PIN FUNCTION
NAME	NO.		
BOOT	1	I	Power supply for the high-side power MOSFET gate driver. Must connect a 0.1uF or greater ceramic capacitor between BOOT pin and SW pin.
VIN	2	I	Power supply input. Must be locally bypassed.
EN	3	I	Enable logic input. Floating the pin enables the device. This pin supports high voltage up to VIN supply. The device has precision enable thresholds 1.18V rising / 1.10V falling for programmable UVLO threshold. The hysteresis is programmable by external resistor network.
RT/SYNC	4	I	Resistor for switching frequency set or external clock input.
FB	5	I	Buck converter output feedback sensing voltage. Connect a resistor divider from VOUT node to FB pin and from FB pin to GND to set up output voltage. The device regulates FB to the internal reference of 0.8V typically.
SS	6	I	Connect to a capacitor to set soft-start time.
GND	7	G	Ground.
SW	8	O	Switching node of the buck converter.
Thermal Pad	9	G	Must be grounded in PCB layout.

7 SPECIFICATIONS

7.1 ABSOLUTE MAXIMUM RATINGS

Over operating free-air temperature unless otherwise noted

DESCRIPTION	PARAMETER	MIN	MAX	UNIT
Input Voltage	VIN, EN to GND	-0.3	42	V
	FB, SS to GND	-0.3	6.5	V
	RT/SYNC to GND	-0.3	6.5	V
Output Voltage	SW to GND	-0.3	42	V
	SW to GND (20ns transient)	-3	42	V
	BOOT to SW		6.5	V
Junction temperature	T_J	-40	150	°C
Storage temperature	T_{STG}	-65	150	°C

7.2 ESD RATINGS

PARAMETER	DEFINITION	MIN	MAX	UNIT
V_{ESD}	Human Body Model (HBM), per ANSI-JEDEC-JS-001-2014 specification, all pins (1)		±2000	V
	Charged Device Model (CDM), per ANSI-JEDEC-JS-002-2014 specification, all pins (1)		±1500	V

(1) HBM and CDM stressing are done in accordance with the ANSI/ESDA/JEDEC JS-001/002-2014 specification

7.3 RECOMMENDED OPERATING CONDITIONS

Over operating free-air temperature range unless otherwise noted

PARAMETER	DEFINITION	MIN	MAX	UNIT
V_{IN}	Supply voltage range	3.8	40	V
BOOT to SW		0	6	V
FB		0	6	V
EN		0	40	V
f_{SW}	Switching frequency range at RT mode and external clock synchronization	300	2200	kHz
T_J	Operating junction temperature	-40	150	°C

7.4 THERMAL INFORMATION

PARAMETER	THERMAL METRIC	eSOP-8L	UNIT
$R_{\theta JA}$	Junction to ambient thermal resistance	41.2	°C/W
$R_{\theta JB}$	Junction to board thermal resistance	18.4	°C/W
$R_{\theta JC\_top}$	Junction to case (top) thermal resistance	64.9	°C/W
$R_{\theta JC\_bot}$	Junction to case (bottom) thermal resistance	3.5	°C/W
ψ_{JB}	Junction to board characterization parameter	18.2	°C/W
ψ_{JT}	Junction to top characterization parameter	6.9	°C/W

7.5 ELECTRICAL CHARACTERISTICS

V_{IN}=EN=3.8V~40V, T_J=-40°C~150°C, typical values are tested under 25°C.

SYMBOL	PARAMETER	TEST CONDITION	MIN	TYP	MAX	UNIT
Power Supply						
V_{IN}	Operating input voltage		3.8		40	V
V_{IN_UVLO}	Input UVLO Hysteresis	V_{IN} rising		3.5 450	3.64	V mV
I_{SHDN}	Shutdown current	EN=0, No load, 3.8V≤V_{IN}≤40V		1	7	uA
I_Q	Quiescent current	EN=floating, No load, No switch, 3.8V≤V_{IN}≤40V, BOOT-SW=5V		25	62	uA
Enable and Feedback						
V_{EN_H}	Enable high threshold		1.13	1.18	1.23	V
V_{EN_L}	Enable low threshold		1.01	1.10	1.15	V
I_{EN_pullup}	Enable pin pull-up current	EN=1V	1.15	1.5	1.67	uA
		EN=1.5V	4.22	5.5	6.04	uA
V_{FB}	Feedback Voltage		0.792	0.8	0.808	V
Power MOSFET						
R_{DSON_H}	High side FET on-resistance			80		mΩ
R_{DSON_L}	Low side FET on-resistance			50		mΩ
Switching Characteristics						
f_{SW}	Switching frequency	R_T=200k		500		kHz

SYMBOL	PARAMETER	TEST CONDITION	MIN	TYP	MAX	UNIT
	Switching frequency range set by RT pin		300		2200	kHz
	Sync external switching frequency range		300		2200	kHz
f_{jitter}	Frequency spread band using RT mode	f_{SW} =500kHz		±6		%
t_{ON_MIN}	Minimum on-time			80		ns
Soft Start and Protection						
I_{SS}	Soft start current			3		uA
I_{LIM_HSD}	HSD peak current limit	V_{IN}=24V	4.41	5	5.84	A
I_{LIM_LSD}	LSD valley current limit	V_{IN}=24V		5.5		A
t_{Hiccup_wait}	Hiccup wait time			512		cycles
t_{Hiccup_start}	Hiccup restart time			8192		cycles
T_{SD}	Thermal shutdown threshold			170		°C
	Hysteresis			30		
Output Voltage Protection						
V_{OVP_H}	Output over voltage protection rising			110		%
V_{OVP_L}	Output over voltage protection falling			105		%
V_{BOOT_UV}	BOOT-SW UVLO threshold	BOOT-SW falling		2.36		V
		BOOT_UV hysteresis		300		mV

7.6 TYPICAL CHARACTERISTICS

V_{IN}=24V, F_{SW}= 500kHz, T_A= 25°C, unless otherwise noted.

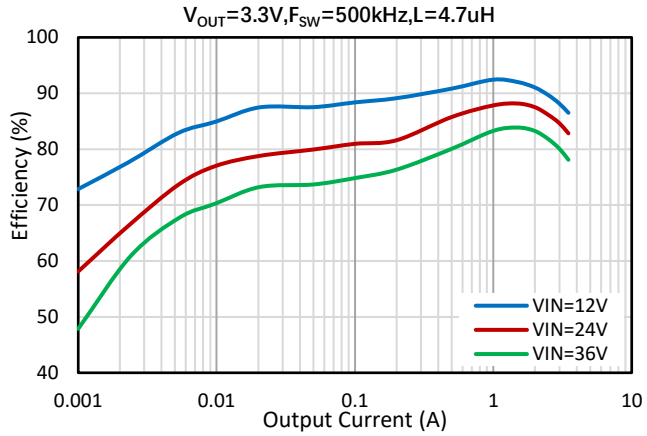


Figure 1. Power Efficiency, V_{OUT}=3.3V

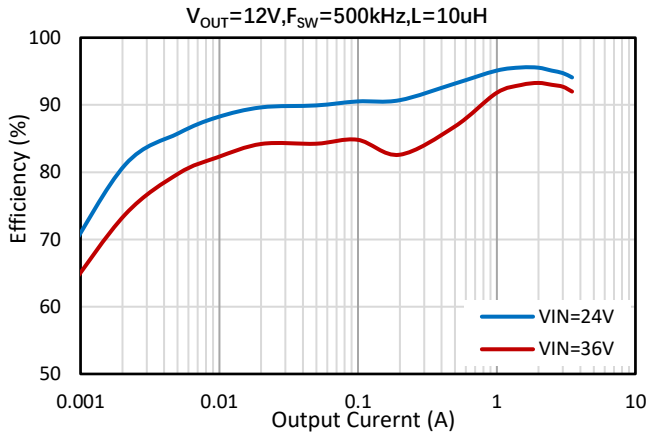


Figure 2. Power Efficiency, V_{OUT}=12V

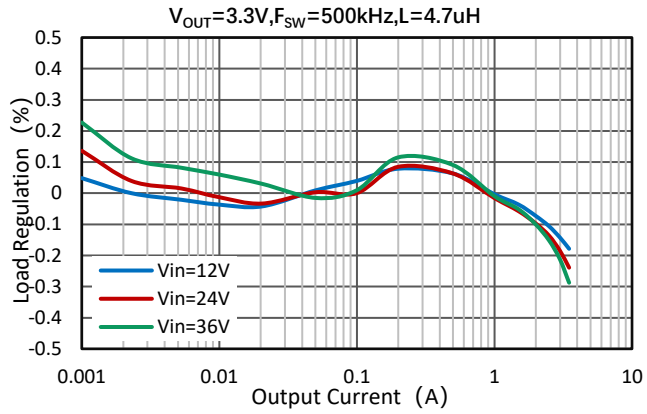


Figure 3. V_{OUT} vs. Load Regulation, V_{OUT}=3.3V

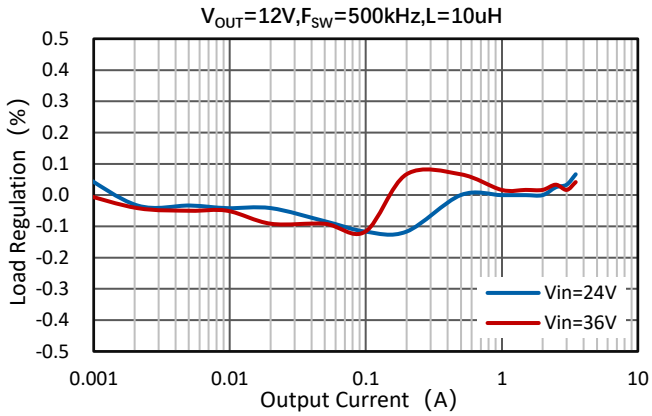


Figure 4. V_{OUT} vs. Load Regulation, V_{OUT}=12V

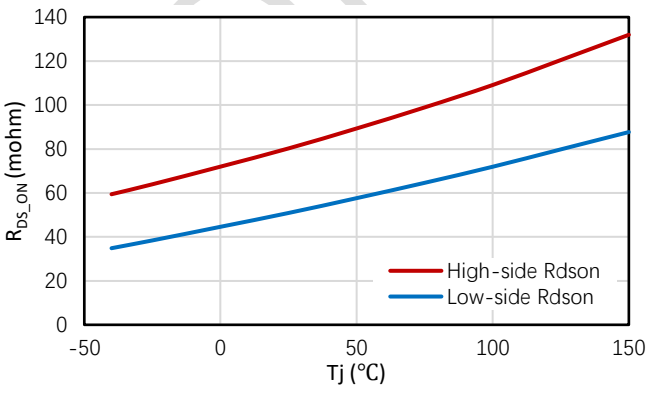


Figure 5. On Resistance vs. Junction Temperature

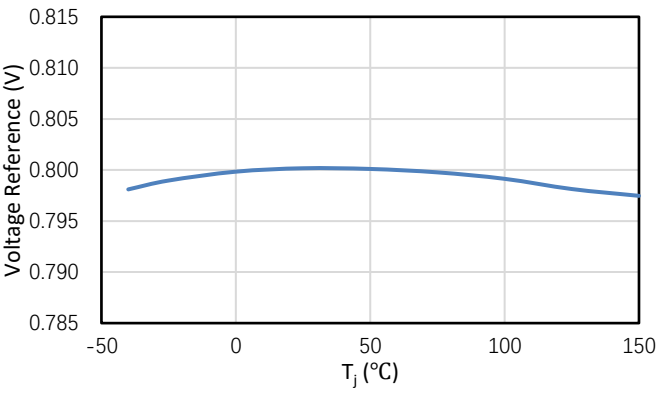


Figure 6. Voltage Reference vs. Junction Temperature

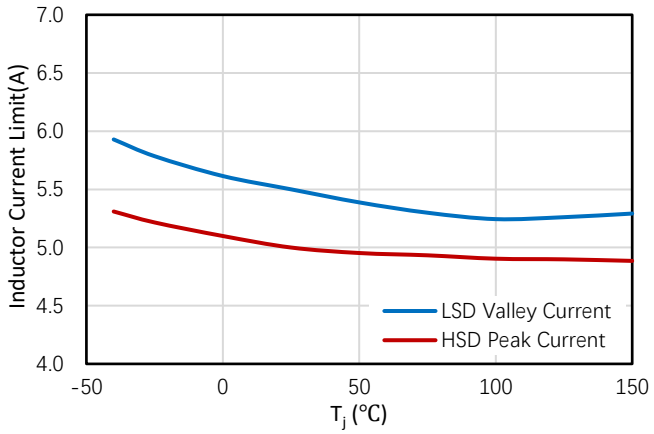


Figure 7. Switch Current Limit vs. Junction Temperature

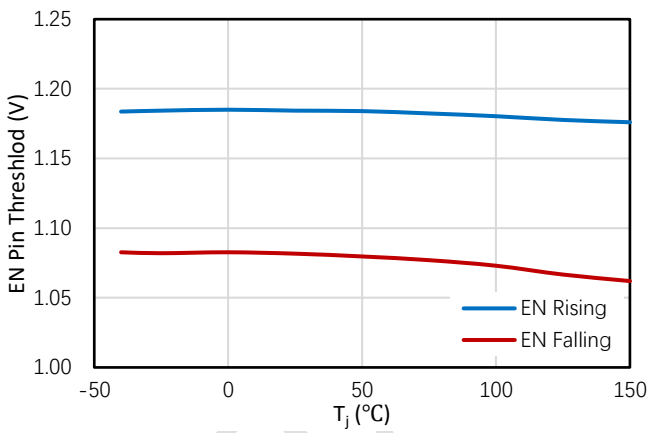


Figure 8. EN Pin Voltage vs. Junction Temperature

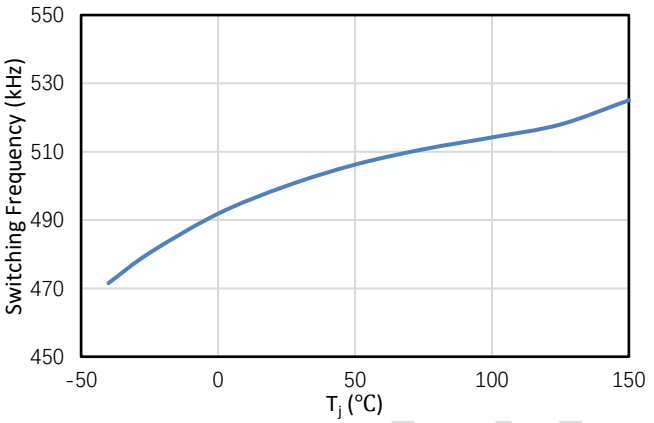


Figure 9. Switching Frequency vs. Junction Temperature

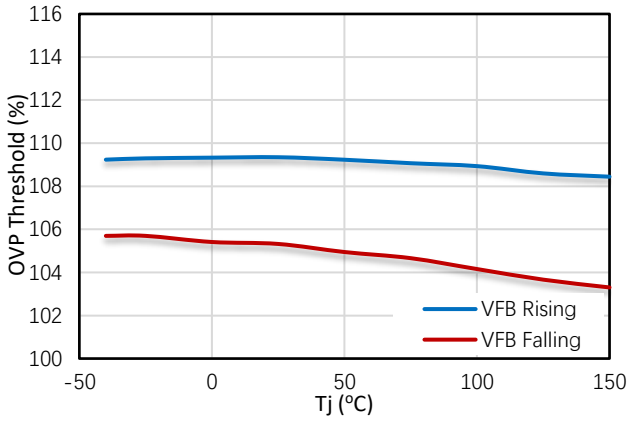


Figure 10. OVP Threshold vs. Junction Temperature

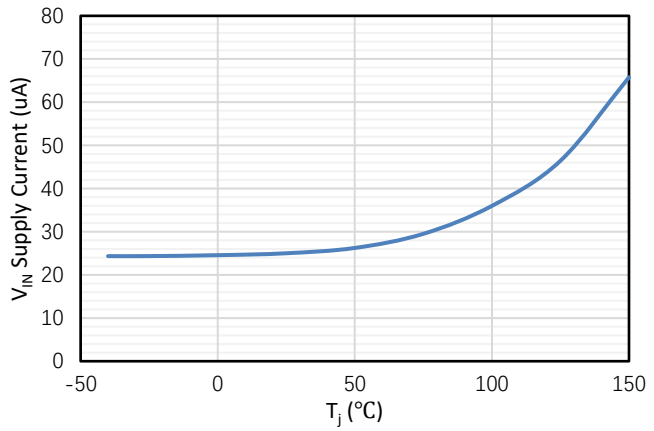


Figure 11. VIN Supply Current vs. Junction Temperature

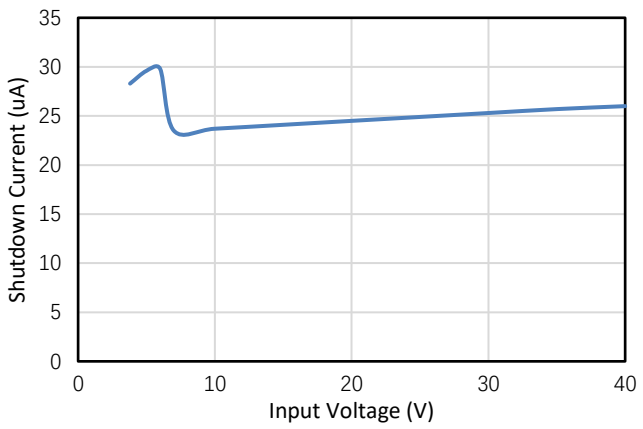


Figure 12. VIN Supply Current vs. Input Voltage

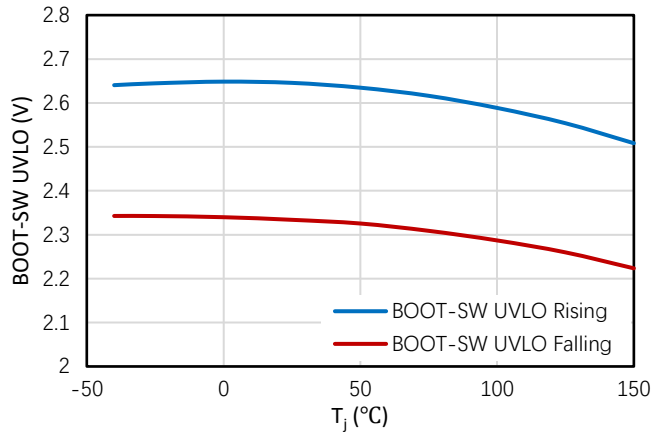


Figure 13. BOOT-SW UVLO vs. Junction Temperature

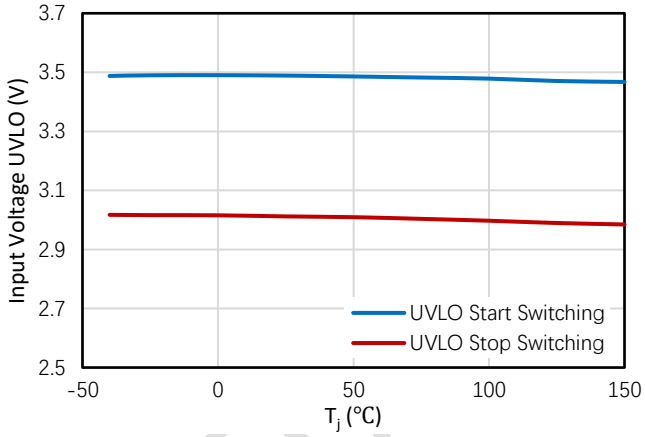


Figure 14. Input Voltage UVLO vs. Junction Temperature

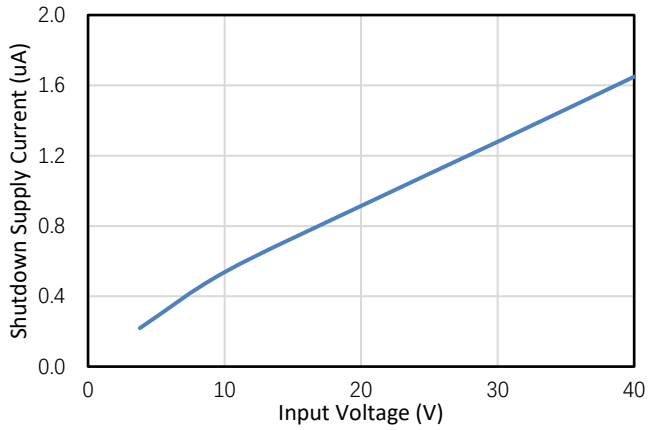


Figure 15. Shutdown Supply Current vs. Input Voltage

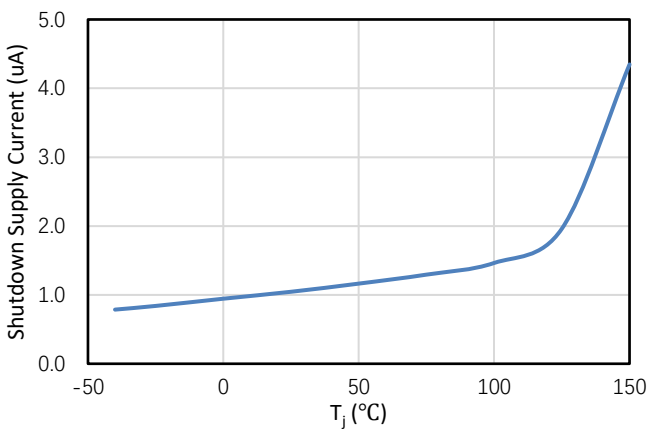


Figure 16. Shutdown Supply Current vs. Junction Temperature

8 FUNCTION BLOCK DIAGRAM

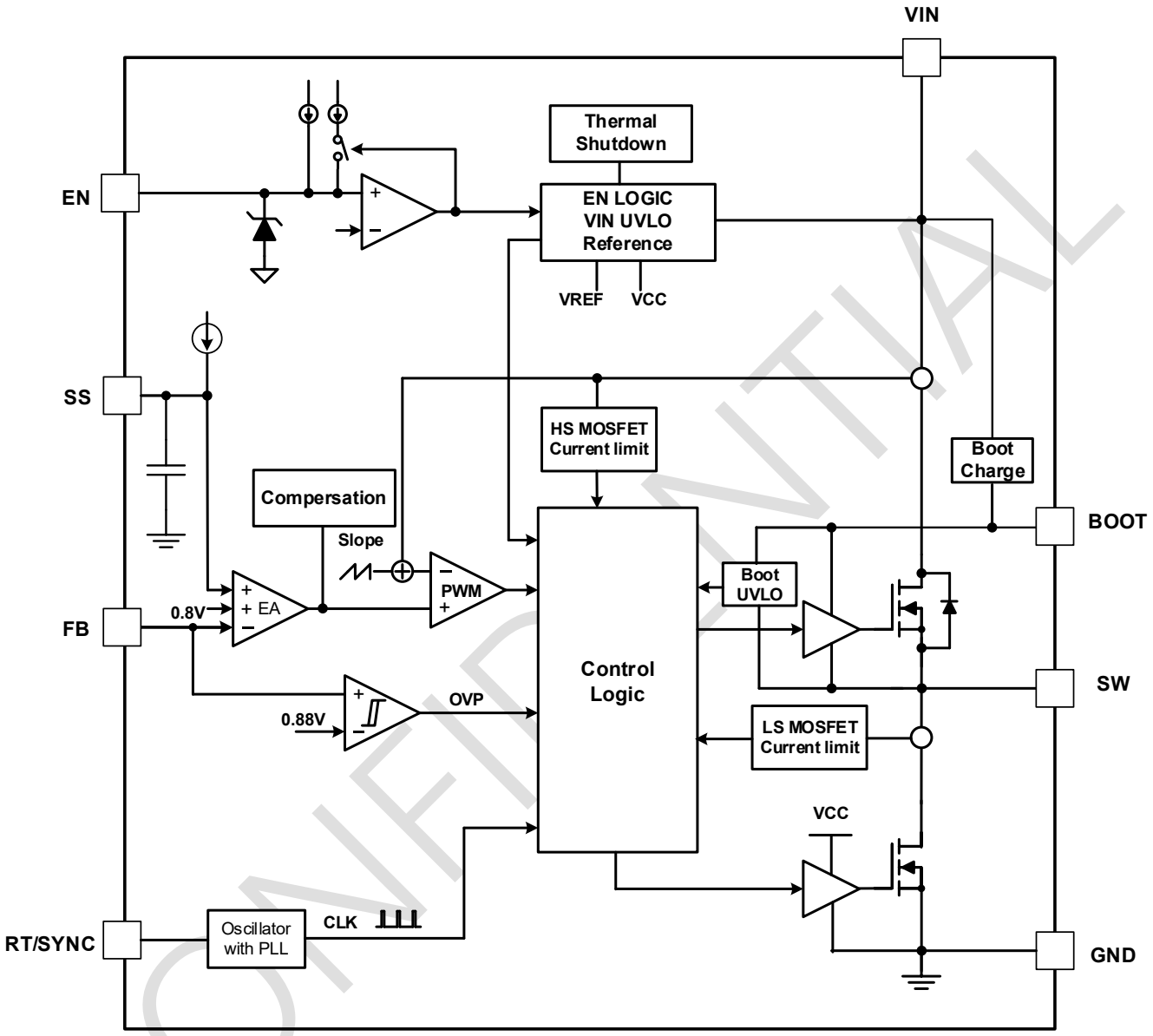


Figure 37. Block Diagram of GBI8432

9 DISCRIPTION

9.1 Overview

The GBI8432 is a 40V, 3.5A buck converter with an integrated 80mΩ high-side and 50mΩ low-side MOSFET. With a wide input range from 3.8V to 40V, the device adopts peak current mode and supports a wide adjustable switching frequency range from 300kHz to 2.2MHz setting by external resistor connected between RT/SYNC pin and GND. The GBI8432 has an internal phase-locked loop (PLL) connected to the RT/SYNC pin that will synchronize the power switch turn on to a falling edge of an external clock signal.

The quiescent current of this device is 25uA in sleep mode and the shutdown current is 1uA. The GBI8432 adopts adjustable soft-start time by connecting an external capacitor from SS pin to GND.

The device has a default input start-up voltage of 3.5V with 450mV hysteresis. The EN pin is a high-voltage pin with a precision threshold that can be used to adjust the input voltage lockout thresholds with two external resistors to meet accurate higher UVLO system requirements. Floating EN pin enables the device. Connecting EN pin to VIN directly starts up the device automatically.

The GBI8432 implements the Frequency Spread Spectrum (FSS) modulation spreading of ±6% centered switching frequency. FSS improves EMI performance by not allowing emitted energy to stay in any one receiver band for a significant length of time. The converter has optimized gate driver scheme to achieve switching node voltage ringing-free without sacrificing the MOSFET switching time to further damping high frequency radiation EMI noise.

The device integrates protections, like cycle-by-cycle current limit, thermal shutdown protection, output over-voltage protection and input over-voltage and under-voltage protection. When the output hard-short, the GBI8432 goes to the Hiccup mode. The device also supports monolithic startup with pre-biased output condition.

It's available in an 8-pin eSOP-8L package.

9.2 Peak Current Mode Control

The GBI8432 employs fixed frequency peak current mode control. An internal clock initiates turning on the integrated high-side power MOSFET in each cycle, then inductor current rises linearly. When the current through high-side MOSFET reaches the threshold level set by the internal compensation voltage of the internal error amplifier, the high-side MOSFET turns off. When the high-side MOSFET turns off, the inductor current discharges through the integrated low-side MOSFET till the next clock cycle begins.

The integrated error amplifier and the internal compensation builds up the feedback loop to regulates the output voltage to the reference. The error amplifier comparing the voltage of the FB pin with an internal

reference voltage of 0.8V. The load current increasement reduces the feedback voltage which is relative to a voltage raise of the error amplifier output till the average inductor current matches the increased load current.

The device also integrates an internal slope compensation circuitry to prevent sub-harmonic oscillation when duty cycle is greater than 50% for a fixed frequency peak current mode control.

9.3 Pulse Skipping Mode (PSM) and Ultra-Low IQ

The GBI8432 operates in Pulse Skipping Mode (PSM) with light load current to improve efficiency. A decrease of the load current leads an increasement in the feedback voltage which yields down the compensation voltage. When the compensation voltage drops to a low clamp threshold, the PSM is triggered. During the skipping period, the discharge of output capacitor leads the output voltage drop which makes the FB voltage decay. Once the FB voltage drops lower than the reference voltage and the compensation voltage rises above the low clamp threshold, the integrated high-side MOSFET turns on in next clock pulse. After several switching cycles with typical 0.9A peak inductor current, the internal compensation voltage drops and is clamped again and pulse skipping mode repeats if the output continues light loaded.

This PSM helps achieving higher efficiency by skipping cycles to reduce switching power loss and gate drive charging loss. Regarding to improve efficiency further, the Ultra-low IQ control in PSM mode is integrated, therefore, the quiescent current is 25uA during skipping period with no switching.

9.4 VIN Power and Input Over-voltage Protection

The GBI8432 is designed to operate from an input voltage supply range between 3.8V to 40V, at least 0.1uF and 4.7uF decoupling ceramic cap are recommended to bypass the supply noise. If the input supply locates more than a few inches from the converter, an additional 47uF electrolytic bulk capacitor may be required in addition to the local ceramic bypass capacitors.

The GBI8432 integrates the input over-voltage protection, when the input voltage is larger than about 45V, the buck is shutdown the disables the output.

9.5 Under Voltage Lockout Threshold and Enable

The EN pin of GBI8432 is a high voltage pin which can be connected to VIN directly to start-up the device. The GBI8432 is enabled when the EN pin voltage higher than the enable threshold of 1.18V and disabled when the EN pin voltage lower than 1.10V. Grace to the internal 1.0uA pull-up current, the device is default enabled when the EN pin floats.

The Under Voltage Lock Out (UVLO) default startup threshold is typical 3.5V with VIN rising and shutdown

threshold is 3.05V with VIN falling. The more accurate UVLO threshold can be programmed through the precision enable threshold of EN pin. Connect an external resistor divider (RL and RH) shown in Figure 18 from VIN to EN. The UVLO rising and falling threshold can be calculated by Equation 1 and Equation 2 respectively.

$$\mathrm{RH} = \frac{V_{rise} - 1.07 * V_{fall}}{1.07 * 5.5uA - 1.5uA} \quad (1)$$

$$\mathrm{RL} = \frac{1.18\mathrm{V}}{\frac{V_{rise} - 1.18V}{R_H} + 1.5uA} \quad (2)$$

where

- V_{rise} is rising threshold of Vin UVLO
- V_{fall} is falling threshold of Vin UVLO

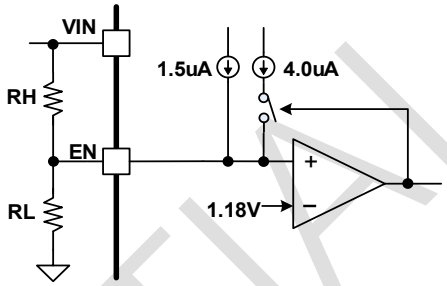


Figure 18. System UVLO by EN divider

9.6 Output Voltage

The GBI8432 regulates the internal reference voltage at 0.8V with ±1% tolerance over the operating temperature and voltage range.

The output voltage is set by a resistor divider from the output node to the FB pin. It is recommended to use 1% tolerance or better resistors. Use Equation 3 to calculate resistance of resistor dividers. To improve efficiency at light loads, larger value resistors are recommended. However, if the value is higher, the regulator will be more noise sensitive. R_{FB_BOT} in the range of 10kΩ to 100kΩ is recommended for most application.

$$R_{FB\_TOP} = \left(\frac{V_{OUT}}{0.8V} - 1\right) * R_{FB\_BOT} \quad (3)$$

where

- R_{FB_TOP} is the resistor connecting the output to the FB pin.
- R_{FB_BOT} is the resistor connecting the FB pin to the ground.

9.7 Bootstrap Voltage Regulator

An external bootstrap capacitor between BOOT pin and SW pin powers floating high-side power MOSFET gate driver. The bootstrap capacitor voltage is charged from an integrated voltage regulator when high-side power MOSFET is off.

The floating supply (BOOT to SW) UVLO threshold is 2.66V rising and hysteresis of 300mV. When the converter operates with high duty cycle or prolongs in sleep mode for certain long time, the required time

interval to recharging bootstrap capacitor is too long to keep the voltage at bootstrap capacitor sufficient. When the voltage across bootstrap capacitor drops below 2.36V, BOOT UVLO occurs.

9.8 LDO Mode Operation

GBI8432 supports the LDO mode operation, the effective duty cycle during LDO mode operation can be approaching to 100%. During the condition of ultra-low voltage difference between the input voltage and the output voltage, the GBI8432 operates in Low Drop-Out mode. High-side MOSFET remains turning on until the BOOT UVLO happens, which means BOOT-SW voltage drops below 2.36V, the high-side MOSFET turns off and low-side MOSFET turns on to recharge bootstrap capacitor periodically in the following several switching cycles. Low-side MOSFET only turns on for about 200ns in each refresh cycle to minimize the output voltage drops. Low-side MOSFET may turn on for several times till the bootstrap voltage is charged to higher than 2.66V for high-side MOSFET working normally. And as described, when the GBI8432 works in LDO mode, the switching frequency is automatically reduced.

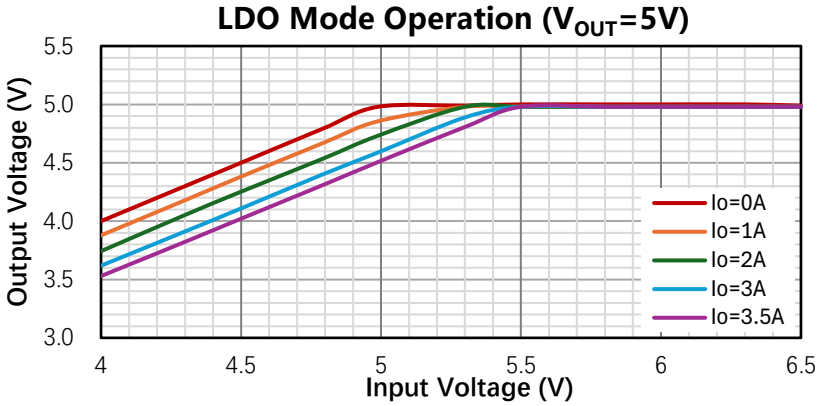


Figure 19. GBI8432 LDO Mode Operation

9.9 Switching Frequency and External Clock Synchronization Mode

The switching frequency of the GBI8432 is set by placing a resistor between RT/SYNC pin and the GND. The RT/SYNC pin is not allowed to be left floating or shorted to the GND.

In resistor setting frequency mode, use Equation 4. to determine the resistance for a switching frequency needed.

$$RT(K\Omega) = \frac{100000}{Fsw(kHz)} \quad (4)$$

Where, Fsw is switching clock frequency.

When works in external clock synchronization mode, the switching frequency synchronizes to an external clock applied to RT/SYNC pin, the rising edge of the SW synchronizes to the falling edge of the external clock at RT/SYNC pin with typical 65ns time delay. A square wave clock signal to RT/SYNC pin must have high level no lower than 3.1V, low level no higher than 0.4V, and pulse width is larger than 80ns. The synchronization frequency range is from 300KHz to 2.2MHz.

Figure 20 shows the applications where both resistor setting frequency mode and external clock synchronization mode are needed. Before an external clock is present, the device works in resistor setting frequency mode. When an external clock presents, the device automatically transitions from resistor setting frequency mode to external clock synchronization mode. An internal PLL locks internal clock frequency to the external clock within about 85us. The converter transitions from the external clock synchronization mode to the resistor setting frequency mode once the external clock disappears.

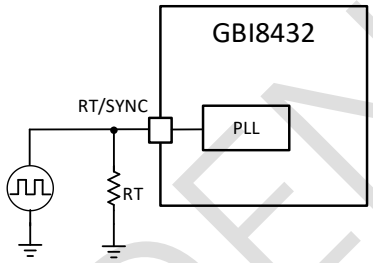


Figure 20. Setting Frequency and Clock Synchronization

9.10 Frequency Spread Spectrum

To reduce EMI, the GBI8432 implements Frequency Spread Spectrum (FSS) feature, which shifts the switching frequency periodically within a certain frequency range around the setting switching frequency. The jittering span is ±6% of the switching frequency with 1/512 swing frequency. This frequency dithering function is effective only for frequency adjusted by resistor placed at RT/SYNC pin. When an external clock synchronization application, the FSS function is disabled automatically.

9.11 Programmable Soft-Start

GBI8432 features programmable soft-start time to avoid inrush current during start-up stage by placing a soft-start capacitor from SS pin to ground. The soft-start time is easily calculated following Equation 5.

$$C_{soft-start}(\text{nF}) = t_{ss}(\text{ms}) * \frac{3\text{uA}}{0.8V} \quad (5)$$

Where:

- $C_{soft\text{-}start}$ is the soft-start capacitor connected from SS pin to the ground
- t_{ss} is the soft-start time

9.12 Overcurrent and Short Circuit Protection

The GBI8432 adopts the peak current mode control. In the overcurrent momentum, the output voltage is yield down by heavy load and the error amplifier drives the compensation voltage high to increase the switching current. As the error amplifier output increases, it will be clamped internally, and the high-side current is clamped by a maximum peak current threshold. The peak current threshold is constant over the full duty cycle range.

When the output over-current or short circuit occurs, the converter cannot provide enough energy to satisfy loading requirement, the converter enters hiccup mode. During hiccup, the inductor current is clamped at over current limitation. Thus, the output voltage drops below regulated voltage with FB voltage less than internal reference voltage continuously. The internal COMP voltage ramps up to high clamp voltage 3.0V typical. When COMP voltage is clamped for 512 cycles, the converter stops switching. After remaining OFF for 8192 cycles, the device restarts from soft starting phase. If overload or hard short condition still exists during soft-start and triggers the COMP voltage clamped, after soft start time and COMP clamping still keeps for 512 cycles, the device enters into turning-off mode again. When overload or hard short condition is removed, the device automatically recovers to enter normal regulating operation. The hiccup protection mode above makes the average short circuit current to alleviate thermal issues and protect the converter.

9.13 Overvoltage Protection

The GBI8432 implements the overvoltage protection (OVP) circuitry to minimize output voltage overshoot during load transient, recovering from output fault condition or light load transient. When the FB pin voltage reaches the rising OVP threshold which is typically 110% of V_{REF}, the high-side MOSFET will be turned off immediately which make the device under OVP. When the FB pin voltage drops below the falling OVP threshold, the high-side MOSFET is turned on and resumed normal operation. The falling OVP threshold is typically 105% of V_{REF}.

9.14 Thermal Shutdown

The GBI8432 features an internal thermal shutdown circuit to protect the device from the damage during excessive heat and power dissipation conditions. The thermal shutdown circuit will be asserted when the junction temperature exceeds typically 170ºC. When the junction temperature falls below 140ºC, the device restarts with internal soft start phase.

10 APPLICATION INFORMATION

Typical Application

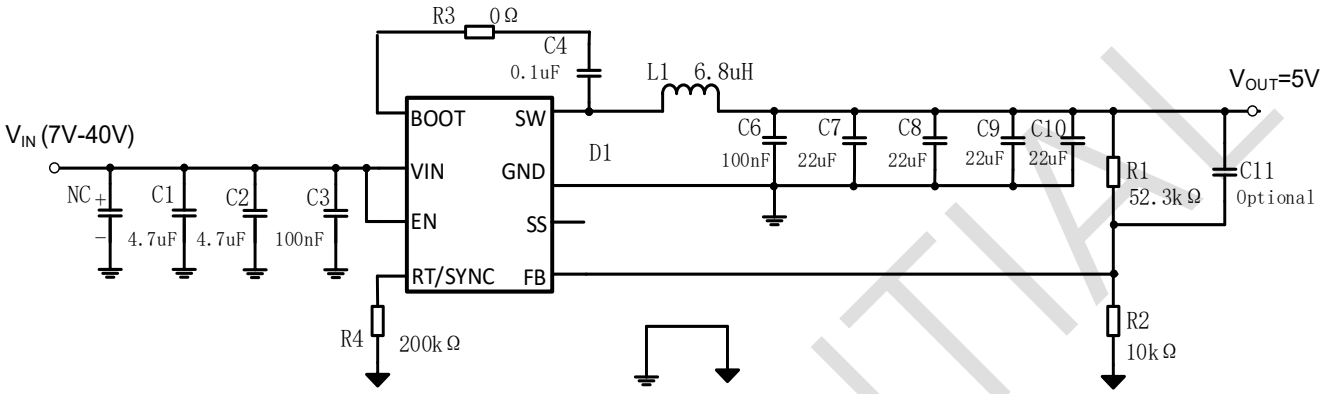


Figure 21. 24V INPUT, 5V/3.5A OUTPUT

Table 1. Design Parameters

Design Parameters	Example Value
Input Voltage	24V typical, 7~40V
Output Voltage	5V
Output Current	3.5A
Output voltage ripple (peak to peak)	<50mV
Overshoot/Undershoot range (0.75~2.25A)	5%
Input Voltage ripple (peak to peak)	<400mV
Switching Frequency	500kHz

10.1 Set Output Voltage

The GBI8432 output voltage can be easily set up using a resistor divider network R1 and R2 as shown in the typical application circuit Figure 21. Use Equation 6 to calculate the resistor divider values.

$$R1 = \frac{(V_{OUT} - 0.8) \times R2}{0.8} \quad (6)$$

In this design example the Vout is 5V. Set the resistor R2 value to be approximately 10k.

$$R1 = \frac{(V_{OUT} - 0.8) \times R2}{0.8} = \frac{(5 - 0.8) \times 10k\Omega}{0.8} = 52.5\ k\Omega$$

Slightly increasing or decreasing R1 to a closest available resistance, the 52.3 kΩ is selected.

10.2 Set Switching Frequency

The GBI8432 switching frequency is able to be set-up by placing a local resistor from RT/SYNC pin to GND. Use following equation to calculate the resistor value.

$$R4(K\Omega) = \frac{100000}{fsw(KHz)} = \frac{100000}{500} = 200\ k\Omega \quad (7)$$

For 500kHz switching frequency, the R4 is 200 kΩ.

10.3 Input Capacitor Selection

For good input voltage filtering, choose low-ESR ceramic capacitors. A X7R ceramic capacitor 4.7uF to 22μF is recommended for the decoupling capacitor and a 0.1μF ceramic bypass capacitor is recommended to be placed as close as possible to the VIN pin. These capacitors must be rated for at least 50V.
For this design, two 4.7uF X7R capacitors and one 0.1uF capacitor rated 50V is recommended.
The input voltage ripple can be calculated by using Equation 8 to calculate the input voltage ripple:

$$\Delta V_{IN} = \frac{I_{OUT}}{C_{IN} \times f_{SW}} \times \frac{V_{OUT}}{V_{IN}} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) = \frac{3.5A}{2 \times 4.7uF \times 500k} \times \frac{5V}{24V} \times \left(1 - \frac{5V}{24V}\right) = 126\ mV \quad (8)$$

Where:

- C_{IN} is the input capacitor value
- f_{sw} is the converter switching frequency
- I_{OUT} is the maximum load current

10.4 Inductor Selection

The performance of inductor affects the power supply' s steady state operation, transient behavior, loop stability, and buck converter efficiency. The critical parameters of inductor is the inductance, the DC resistance (DCR), the saturation current and the RMS current.
Use following equation to the minimum inductance:

$$L_{MIN} = \frac{V_{OUT} \times (V_{INMAX} - V_{OUT})}{V_{INMAX} \times K_{IND} \times I_{OUT} \times f_{SW}} \quad (9)$$

Where

- V_{OUT} is output voltage
- K_{IND} is the Ripple Ration of the inductor ripple current ($\Delta iL/I_{OUT}$), 0.4 is recommended here
- V_{INMAX} is the maximum input voltage
- f_{SW} is the converter switching frequency
- I_{OUT} is the output current

In this design example:

$$L > L_{MIN} = \frac{V_{OUT} \times (V_{INMAX} - V_{OUT})}{V_{INMAX} \times K_{IND} \times I_{OUT} \times f_{SW}} = \frac{5V \times (40V - 5V)}{40V \times 0.4 \times 3.5A \times 500KHz} = 6.3\ uH$$

Generally, the Inductor values can have ±20% or even ±30% tolerance with no current bias. When the inductor current approaches saturation level, its inductance can decrease 20% to 35% from the value at 0A current depending on how the inductor vendor defines saturation. When selecting an inductor, choose its rated current especially the saturation current larger than its peak current during the operation. The peak switching current of inductor is calculated in below:

$$I_{LPEAK} = I_{OUT} + K_{IND} \times \frac{I_{OUT}}{2} = 3.5A + 0.4 \times \frac{3.5A}{2} = 4.2\ A$$

A minimum inductance of 6.8uH and the peak saturation current of 5.5A is recommended.

10.5 Output Capacitor

The output capacitor must be chosen carefully with the reason that this capacitor value determines the regulator pole, the output voltage ripple, and how the regulator responds to a large change in load current. Generally, choose a low-ESR output capacitor like a ceramic capacitor from X5R or X7R family to get small output voltage ripple.

From the required output voltage ripple (<50mV), use the Equation 10 to calculate the minimum required effective capacitance, C_{OUT}.

$$C_{OUT} > \frac{\Delta I_{LPP}}{8 \times V_{OUT\_Ripple} \times f_{SW}} = \frac{K_{IND} \times I_{OUT}}{8 \times V_{OUT\_Ripple} \times f_{SW}} \quad (10)$$

The allowed maximum ESR of the output capacitor is calculated by the Equation 11.

$$R_{ESR} < \frac{V_{OUT\_Ripple}}{k_{IND} \times I_{OUT}} \quad (11)$$

Where

- V_{OUT_Ripple} is output voltage ripple caused by charging and discharging of the output capacitor.
- k_{IND} is the Ripple Ration of the inductor ripple current ($\Delta iL/I_{OUT}$), 0.4 is recommended here
- I_{OUT} is the maximum output current
- f_{SW} is the converter switching frequency.

In this design, V_{OUT_Ripple} is smaller than 50mV, f_{SW} is 500kHz, I_{OUT} is 5A and K_{IND} is 0.4:

$$C_{OUT} > \frac{0.4 \times 3.5A}{8 \times 50mV \times 500k} = 7\ uF$$

$$R_{ESR} < \frac{50mV}{0.4 \times 3.5A} = 35.7\ m\Omega$$

In buck converter, higher capacitor values can be used to improve the load transient response. Normally the converter control loop needs to take some switching clock cycles to respond to the output voltage changes. The output capacitors must be relatively large enough to charge or discharge current to maintain the output voltage within the specified range in 3 clock cycles. The following two Equations are used to calculate the minimum capacitance to keep the undershoot and overshoot voltages within a specified range.

$$C_{OUT} > \frac{3 \times (I_{TOH} - I_{TOL})}{f_{SW} \times V_{OUS}} \quad (12)$$

$$C_{OUT} > \frac{I_{TOH}^2 - I_{TOL}^2}{(V_{OUT} + V_{OOS})^2 - V_{OUT}^2} \times L \quad (13)$$

Where

- I_{TOH} is the high level of output current during load transient
- I_{TOL} is the low level of output current during load transient
- V_{OUS} is the undershoot voltage
- V_{OOS} is the overshoot voltage
- L is the inductance of inductor in design
- f_{SW} is the converter switching frequency.

For this design example:

$$C_{OUT} > \frac{3 \times (I_{TOH} - I_{TOL})}{f_{SW} \times V_{OUS}} = \frac{3 \times (2.25A - 0.75A)}{500kHz \times 250mV} = 36\ uF$$

$$C_{OUT} > \frac{2.25A^2 - 0.75A^2}{(5V + 250mV)^2 - 5^2} \times 8.2uH = 14.4\ uF$$

Considering the ceramic capacitor degrading under DC bias, the X7R capacitor of 4x22uF with 25V DC rating and 15mΩ ESR is selected.

10.6 Bootstrap Capacitor

For proper operation of the device, a 0.1uF ceramic capacitor of X5R or X7R must be placed between the SW pin to the BOOT pin. The DC rating of this capacitor is must be 10V or higher voltage level.

10.7 Typical BOM Recommendation

Table 2 lists the recommended BOM for typical applications by referring Figure 21. Considering the capacitor' s degrading under DC bias, it is recommended to leave margin on the voltage rating to ensure adequate effective capacitance. Typically, 4x 22μF(1210/25V) ceramic output capacitors are recommended for most applications. For higher output applications, better load transient performance or has smaller effective ceramic output capacitance, plus one output electrolytic capacitor (ECAP >=47uF) are recommended, if for achieving lower output ripple, removing electrolytic capacitor and add more ceramic output capacitors are recommended.

Table 2. Typical BOM For Fsw=500kHz

V_{OUT}	L	C_{OUT}	R1	R2	R4
3.3V	4.7uH	4x22uF	32k	10k	200k
5V	6.8uH	4x22uF	52.5k	10k	200k
12V	10uH	4x22uF	140k	10k	200k
24V	33uH	3x10uF (50V)	290k	10k	200k

10.8 Application Curves

Figure 22 through Figure 37 apply to the circuit of Figure 21. V_{IN} = 24 V, T_A = 25°C, unless otherwise specified.

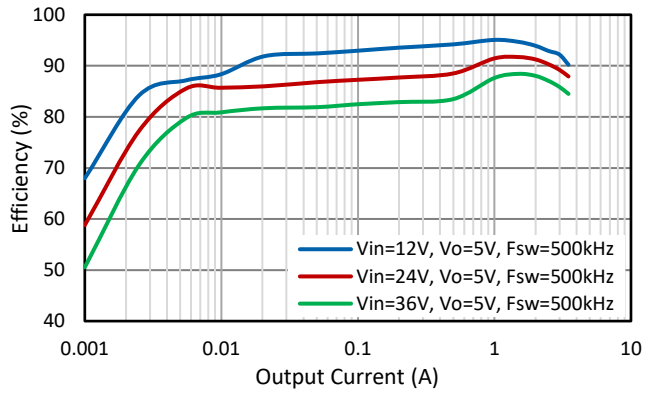


Figure 22. Power Efficiency

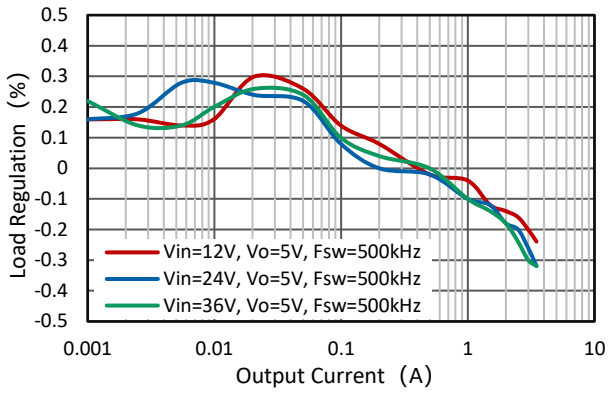


Figure 23. V_{OUT} vs. Load Regulation

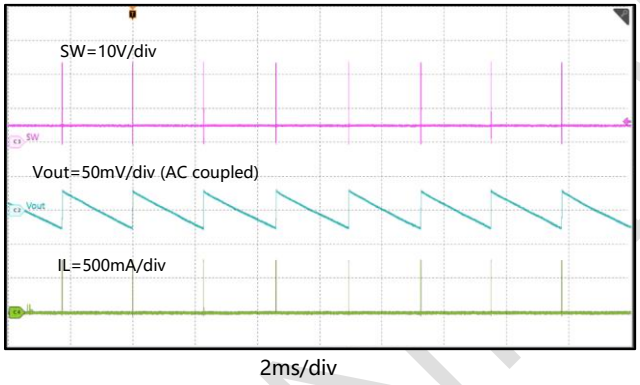


Figure 24. Output Voltage Ripple, I_{OUT}=1mA

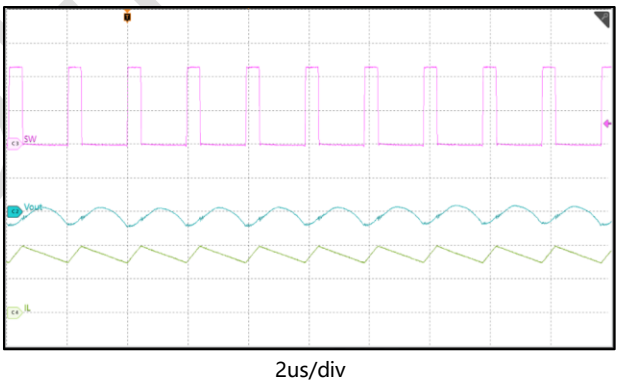


Figure 25. Output Voltage Ripple, I_{OUT}=3.5A

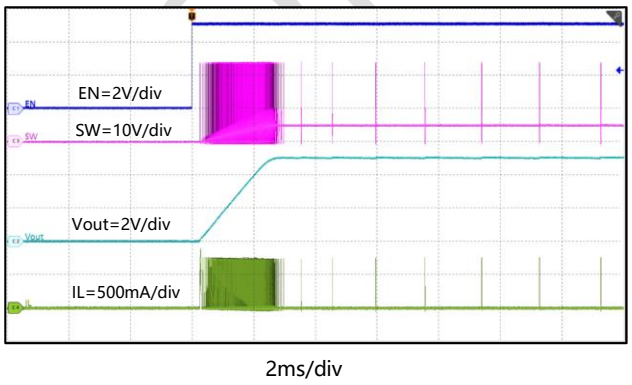


Figure 26. Start-Up with EN, I_{OUT}=1mA

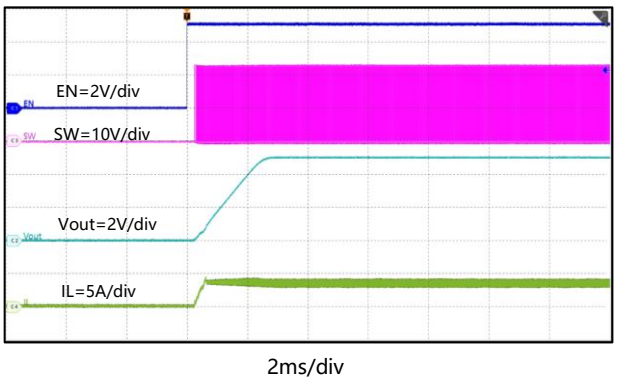
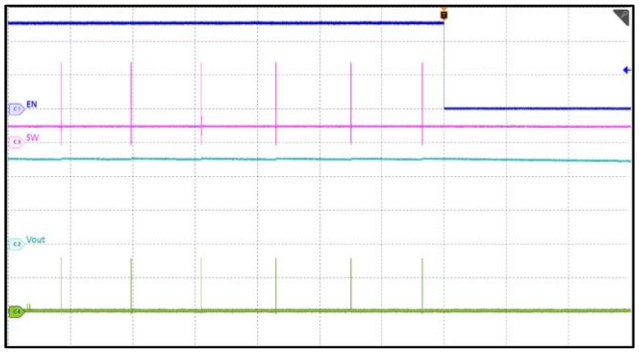
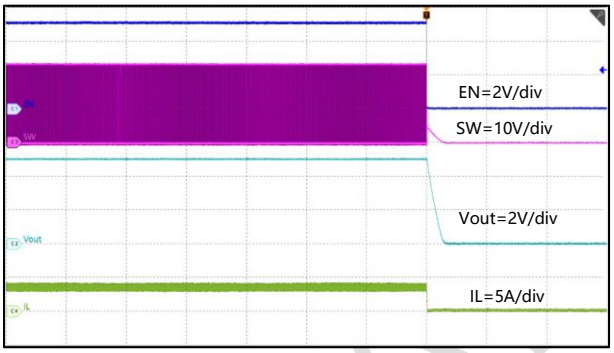


Figure 27. Start-Up with EN, I_{OUT}=3.5A



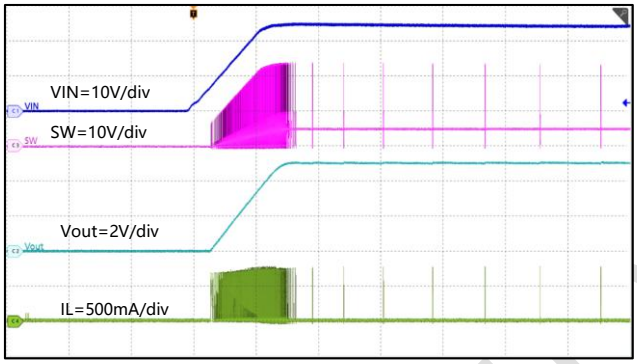
2ms/div

Figure 28. Shut-down with EN, I_{OUT}=1mA



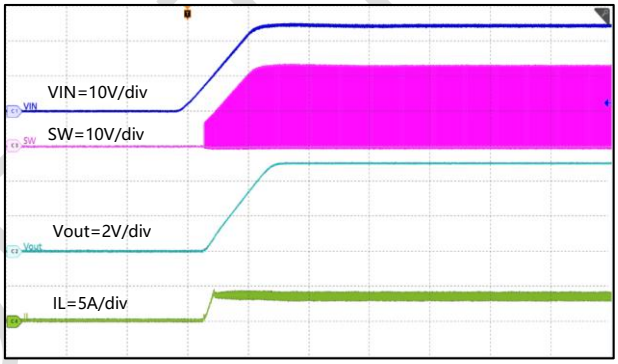
400us/div

Figure 29. Shut-down with EN, I_{OUT}=3.5A



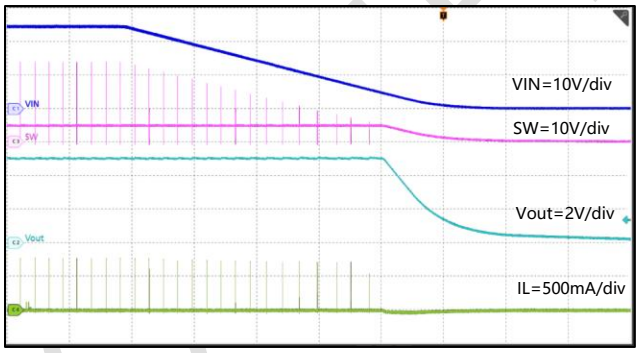
2ms/div

Figure 30. Start-Up with VIN rising, I_{OUT}=1mA



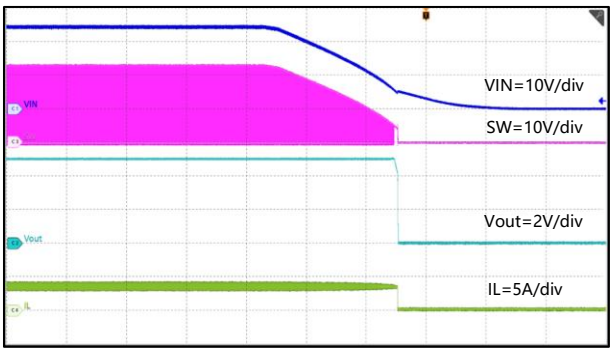
2ms/div

Figure 31. Start-Up with VIN Rising, I_{OUT}=3.5A



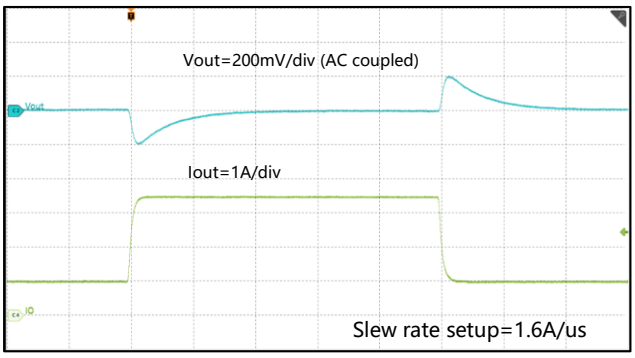
10ms/div

Figure 32. Shut-Down with VIN falling, I_{OUT}=1mA



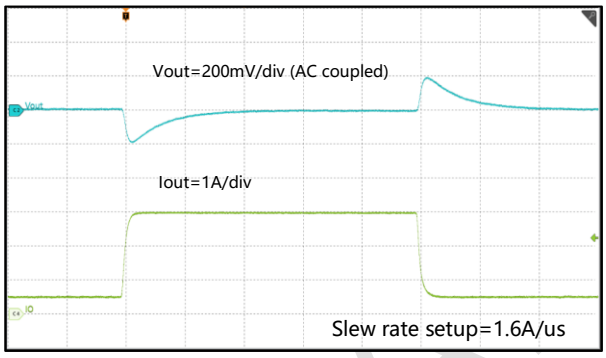
10ms/div

Figure 33. Shut-Down with VIN falling, I_{OUT}=3.5A



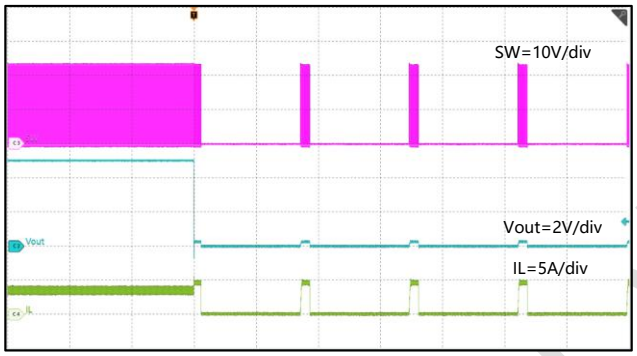
200us/div

Figure 34. Transient Response 1.0A-3.5A



100us/div

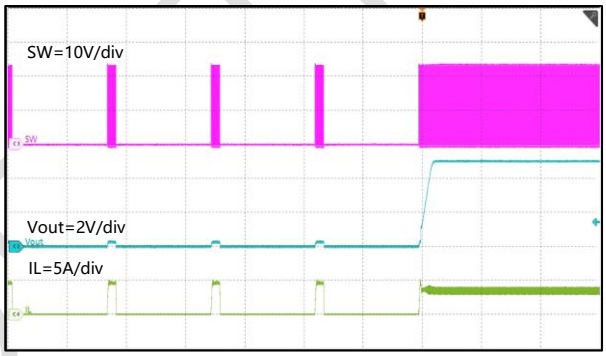
Figure 35. Transient Response 0.5A-3.0A



10ms/div

Figure 36. Normal Operation to Hard-short

I_{OUT}=3.5A



10ms/div

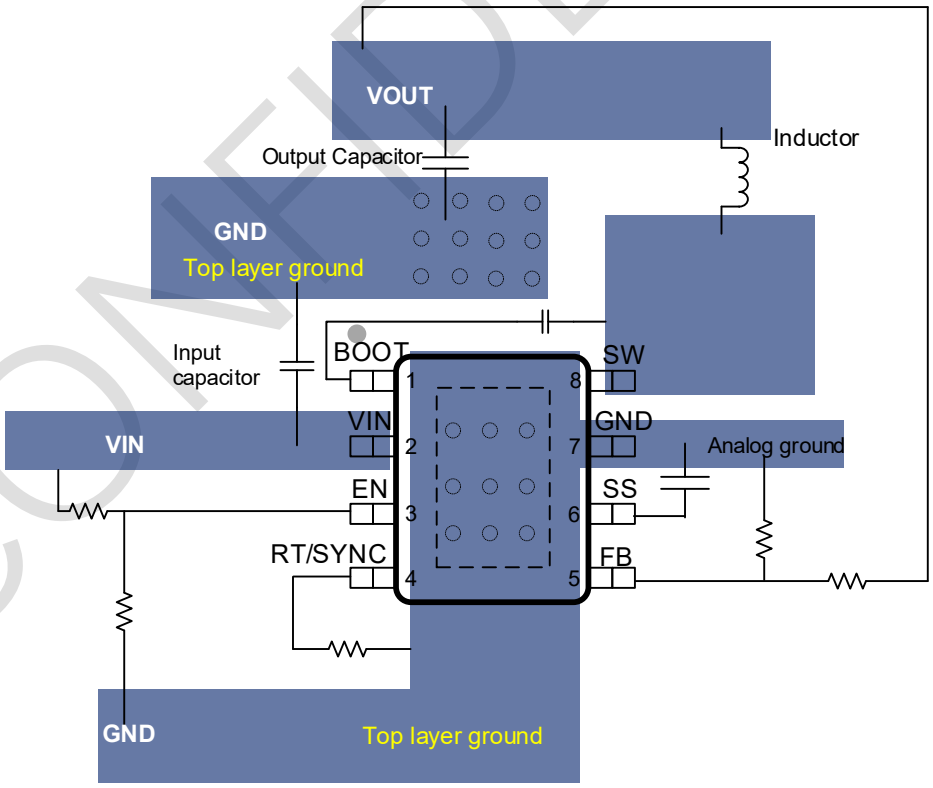
Figure 37. Hard-short Recover

I_{OUT}=3.5A

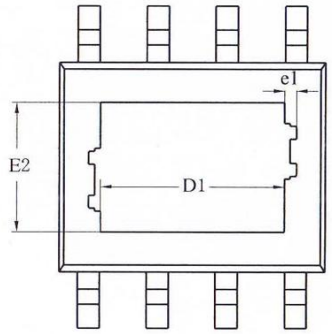
11 Layout Guideline

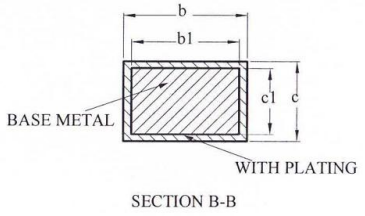
Layout is critical for proper operation. Please follow the layout guidelines.

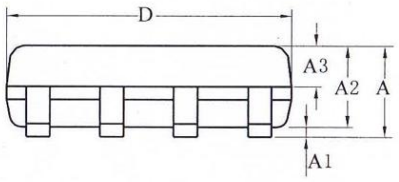
1. The power ground is very critical. The power trace should take lowest impedance as possible and the ground area should be sufficient and event to optimize thermal.
2. The GND Pin should be connected directly to the thermal pad under the IC, 8mil Max thermal via recommended.
3. Place the bypass input capacitor with low ESR as close as possible to the VIN pin and GND. The bypassing loop from VIN terminal to the GND should be as short as possible.
4. The RT/SYNC is sensitive to noise. The RT resistor should be placed as close as possible to the RT/SYNC pin with minimum trace length to the GND.
5. The inductor should be located as close as possible to the SW pin for reducing magnetic and electrostatic noise.
6. The feedback resistor divider should be placed close to the FB pin.
7. The ground connected to the input capacitors and output capacitors should be tied to the system ground plane in only one spot to minimize conducted noise to the system ground plane.
8. Four-layer layout is strongly recommended for better thermal performance.

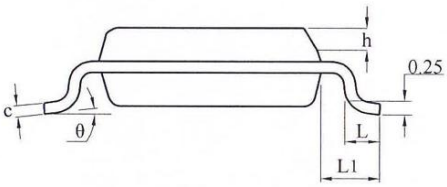


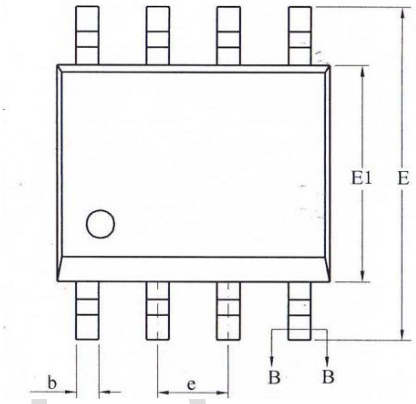
PACKAGE INFORMATION (eSOP-8L Package)







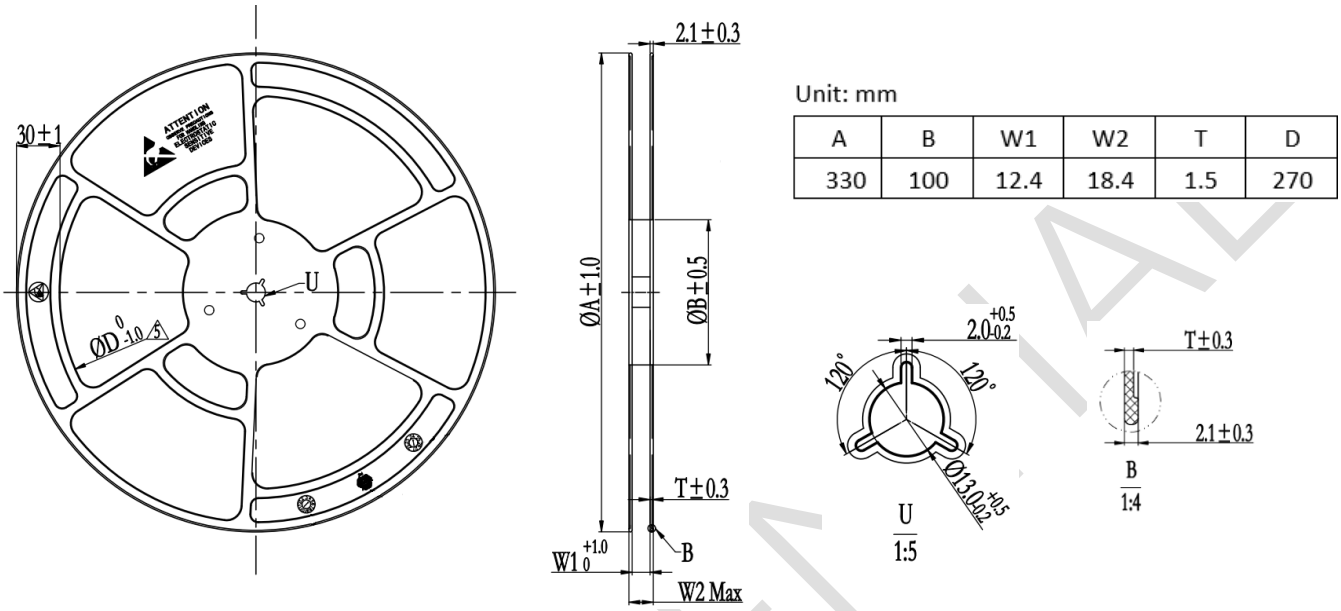




D1	E2	e1
3.10	2.21	0.10

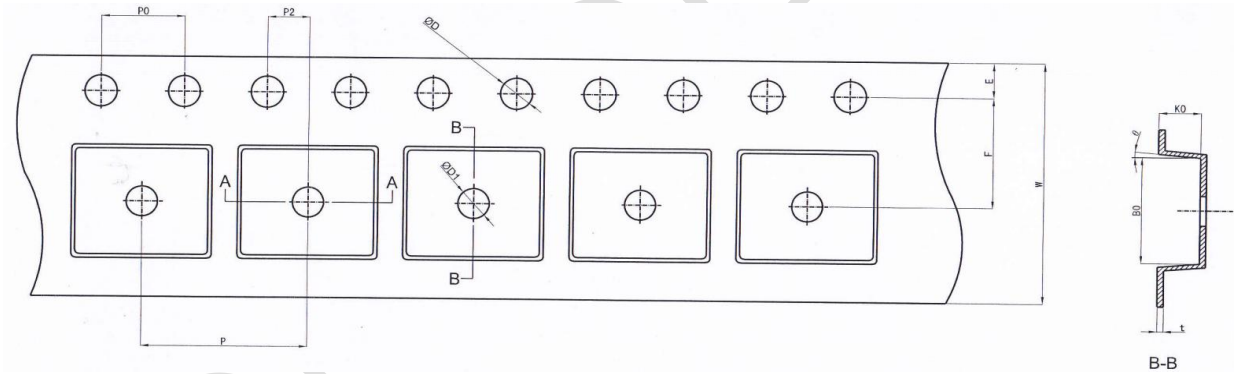
Symbol	Millimeter		
	Min	Nor	Max
A	-	-	1.65
A1	0.05	-	0.15
A2	1.30	1.40	1.50
A3	0.60	0.65	0.70
b	0.39	-	0.47
b1	0.38	0.41	0.44
c	0.20	-	0.24
c1	0.19	0.20	0.21
D	4.80	4.90	5.00
E	5.80	6.00	6.20
E1	3.80	3.90	4.00
e	1.27BSC		
h	0.25	-	0.50
L	0.50	0.60	0.80
L1	1.05REF		
θ	0	-	8°

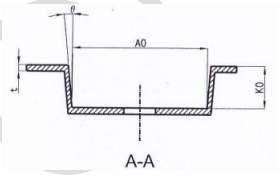
TAPE AND REEL INFROMATION



Unit: mm

A	B	W1	W2	T	D
330	100	12.4	18.4	1.5	270





Unit: mm

E	F	D	D1	t	θ
1.75	5.5	1.5	1.55	0.3	3°

Part Number	Pins	Package Quantity	A0 (mm)	B0 (mm)	K0 (mm)	W (mm)	P (mm)	P0 (mm)	P2 (mm)
GBI8432SMAR	8	4000	6.6	5.3	1.9	12.0	8.0	4.0	2.0