



钜地半导体
Tudi Semiconductor

Product Specification

TUDI- SN74AHCT1G08

Single 2-Input Positive-AND Gate

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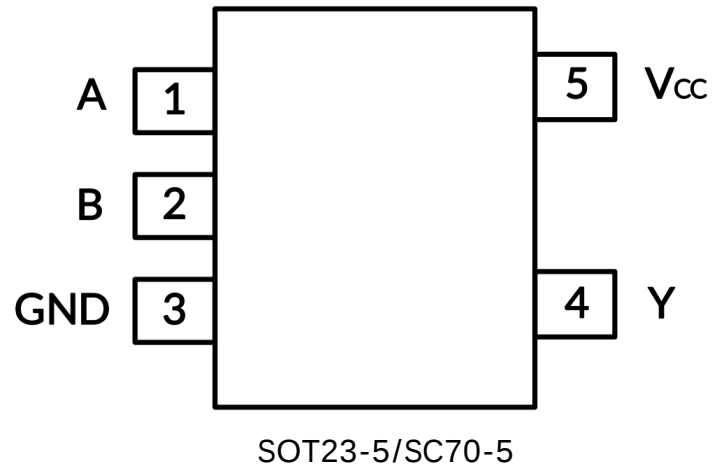
**semiconductor device
manufacturer**

- Design
- research and development
- production
- and sales



FEATURES

- Operating Voltage Range: 2.0V to 5.5V
- Low Power Consumption: 0.1 μ A (TYP)
- Operating Temperature Range:
-40 ° C to 125 ° C
- Inputs Are TTL-Voltage Compatible
- High Output Drive: $\pm$ 32mA at $V_{CC}=5.0V$
- Micro SIZE PACKAGES: SOT23-5, SC70-5



APPLICATIONS

- Active Noise Elimination
- Bar Code Scanner
- Blood Pressure Monitor
- CPAP Machine
- Fingerprint identification
- Network attached storage (NAS)

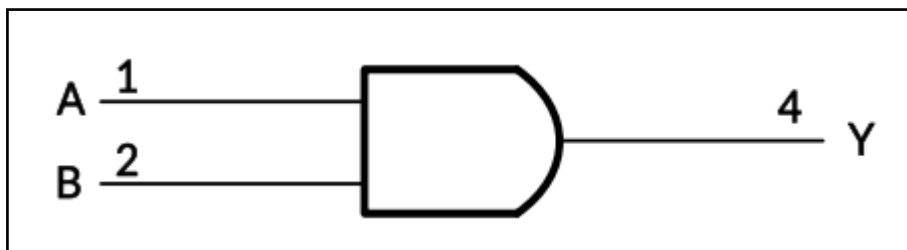
DESCRIPTIONS

The SN74AHCT1G08 single 2-input positive-AND gate is designed for 2.0 to 5.5V V_{CC} operation. The SN74AHCT1G08 device performs the Boolean function $Y=A \bullet B$ or $Y= A + B$ in positive logic. The device is fully specified for partial-power-down applications using I off. The I off circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down.

The SN74AHCT1G08 is available in Green SOT23-5 and SC70-5 packages. It operates over an ambient temperature range of -40 ° C to 125 ° C



LOGIC SYMBOL



FUNCTION TABLE

INPUTS		OUTPUT
A	B	Y
H	H	H
L	H	L
H	L	L
L	L	L

$Y=A \bullet B$ H=High Voltage Level L=Low Voltage Level

PIN CONFIGURATION AND FUNCTIONS (TOP VIEW)

PIN	NAME	I/O	DESCRIPTION
1	A	1	Input
2	B	I	Input
3	GND	P	Ground
4	Y	O	Output
5	V _{cc}	P	Power pin



Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted) ^{(1) (2)}

		MIN	MAX	UNIT
V_{CC}	Supply voltage range	-0.5	6.5	V
V_I	Input voltage range (2)	-0.5	6.5	V
V_O	Voltage range applied to any output in the high-impedance or power-off state (2)	-0.5	6.5	V
V_O	Voltage range applied to any output in the high or low state (2)(3)	-0.5	$V_{CC}+0.5$	V
I_{IK}	Input clamp current $V_I < 0$		-50	mA
I_{OK}	Output clamp current $V_O < 0$		-50	mA
I_O	Continuous output current		± 50	mA
	Continuous current through V_{CC} or GND		± 100	mA

Package Thermal Impedance

	PARAMETER		MIN	MAX	UNIT
θ_{JA}	Package thermal impedance ⁽⁴⁾	SOT23-5 SC70-5		230 376	/W
Temperature					
	PARAMETER		MIN	MAX	UNIT
Temperature	Junction temperature, T_j ⁽⁵⁾		-65	150	
	Storage temperature, T_{stg}		-65	150	

ESD Ratings

The following ESD information is provided for handling of ESD-sensitive devices in an ESD protected area only.

	VALUE	UNIT
Human-Body Model(HBM)	± 2000	V
Charged-Device Model(CDM)	±1000	
Machine Model(MM)	±200	

ESD SENSITIVITY CAUTION



ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

NOTE:

- (1) Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under Recommended Operating Conditions is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) The input and output negative-voltage ratings may be exceeded if the input and output current ratings are observed.
- (3) The value of V_{CC} is provided in the Recommended Operating Conditions table.
- (4) The package thermal impedance is calculated in accordance with JEDEC-51.
- (5) The maximum power dissipation is a function of $T_{J(MAX)}$, $R_{\theta JA}$, and T_A . The maximum allowable power dissipation at any ambient temperature is $P_D = (T_{J(MAX)} - T_A) / R_{\theta JA}$. All numbers apply for packages soldered directly onto a PCB.



ELECTRICAL CHARACTERISTICS

over recommended operating free-air temperature range (TYP values are at $T_A = +25^{\circ}\text{C}$, Full= -40°C to 125°C , unless otherwise noted.) (1)

Recommended Operating Conditions

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	MAX	UNIT
Supply Voltage	V_{CC}	Operating	2.0	5.5	V
		$V_{CC}=2.0\text{V}$	1.0		V
High-Level Input Voltage	V_{IH}	$V_{CC}=3.3\text{V}$	1.5		
		$V_{CC}=4.5\text{V to }5.5\text{V}$	2.0		
		$V_{CC}=2.0\text{V}$		0.3	V
Low-Level Input Voltage	V_{IL}	$V_{CC}=3.3\text{V}$		0.55	
		$V_{CC}=4.5\text{V to }5.5\text{V}$		0.8	
Input Voltage	V_I		0	5.5	V
Output Voltage	V_O		0	V_{CC}	V
Input Transition Rise or Fall	t/v	$V_{CC}=2.0\text{V to }5.5\text{V}$		5	ns/V
Operating Temperature	T_A		-40	125	



DC Characteristics

PARAMETER	TEST CONDITIONS	V _{CC}	TEMP	MIN(2)	TYP(3)	MAX(2)	UNIT
V _{OH}	I _{OH} = -100μA	2.0V to 5.5V	Full	V _{CC} -0.1			V
	I _{OH} = -8mA	2.0		1.6			
	I _{OH} = -24mA	3.3		2.5			
		4.5V		3.8			
	I _{OH} = -32mA	5V		4.2			
		5.5V		4.8			
V _{OL}	I _{OL} =100μA	2.0V to 5.5V	Full			0.1	V
	I _{OH} =8mA	2.0				0.45	
	I _{OH} =24mA	3.3				0.55	
		4.5V				0.55	
	I _{OL} =32mA	5V				0.5	
		5.5V				0.45	
I _I A or B inputs	V _I =5.5V or GND	0V to 5.5V	+25		±0.1		μA
			Full			±5	
I _{off}	V _I or V _O =5.5V	0V	+25		±0.1		μA
			Full			± 10	
I _{CC}	V _I =5.5V or GND, I _O =0	2.0V to 5.5V	+25		0.1		μA
			Full			10	
I _{CC} T	One input at 3.4V ,Other inputs at V _{CC} or GND	5.5V	Full			500	μA
C _i (Input Capacitance)	V _{CC} =0V,f=10MHz	0V	+25		6		pF

(1) All unused inputs of the device must be held at VCC or GND to ensure proper device operation.

(2) Limits are 100% production tested at 25°C. Limits over the operating temperature range are ensured through correlations using statistical quality control (SQC) method.

(3) Typical values represent the most likely parametric norm as determined at the time of characterization. Actual typical values may vary over time and will also depend on the application and configuration.



AC Characteristics

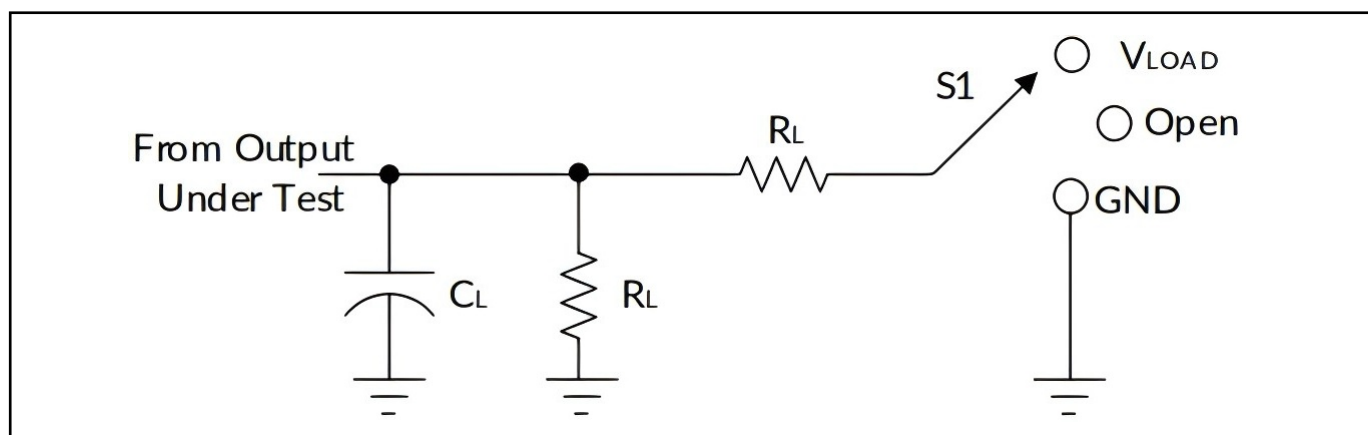
PARAMETER	SYMBOL	TEST CONDITIONS		MIN(2)	TYP(3)	MAX(2)	UNIT
Propagation Delay	t_{pd}	$V_{CC}=2.0V\pm0.2V$	$C_L=30pF, R_L=500\Omega$		15.5		
		$V_{CC}=3.3V\pm0.3V$	$C_L=50pF, R_L=500\Omega$		13.5		ns
		$V_{CC}=5V\pm0.5V$	$C_L=50pF, R_L=500\Omega$		4.1		
Power Dissipation Capacitance	C_{pd}	$V_{CC}=5V$	$f=10MHz$		22		pF

(1) All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation.

(2) This parameter is ensured by design and/or characterization and is not tested in production.

(3) Typical values represent the most likely parametric norm as determined at the time of characterization. Actual typical values may vary over time and will also depend on the application and configuration.

PARAMETER MEASUREMENT INFORMATION



TEST	S1
t_{pLH}/t_{pHL}	Open
t_{pLz}/t_{pzL}	V_{LOAD}
t_{pHz}/t_{pzH}	GND



INPUTS

V_{CC}	V_I	t_r, t_f	V_M	V_{LOAD}	C_L	R_L	V
$2.0V \pm 0.2V$	V_{CC}	$\leq 2ns$	$V_{CC}/2$	$2 \times V_{CC}$	30pF	500 Ω	0.15V
$3.3V \pm 0.3V$	3V	$\leq 2.5ns$	1.5V	6V	50pF	500 Ω	0.3V
$5V \pm 0.5V$	V_{CC}	$\leq 2.5ns$	$V_{CC}/2$	$2 \times V_{CC}$	50pF	500 Ω	0.3V

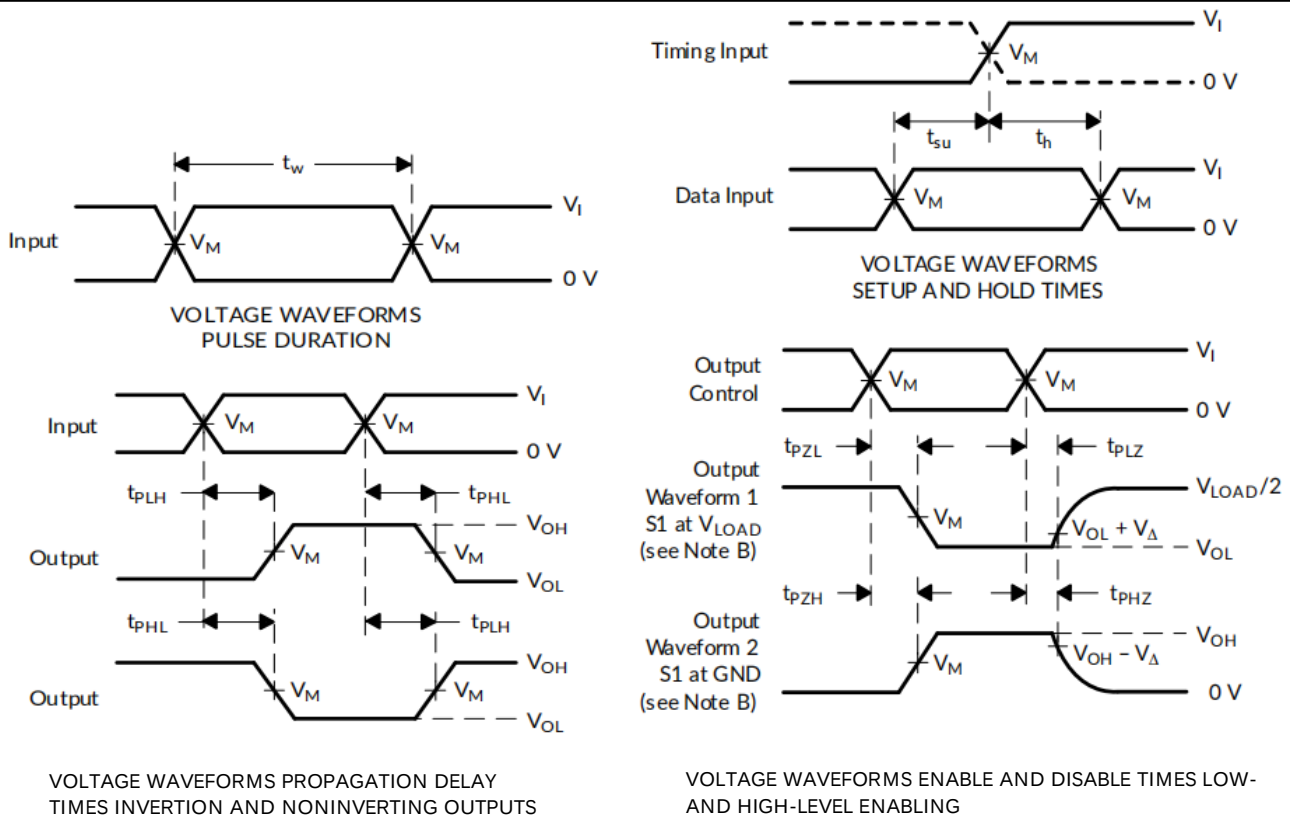


Figure 1. Load Circuit and Voltage Waveforms

NOTES: A. C_L includes probe and jig capacitance.

B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.

C. All input pulses are supplied by generators having the following characteristics: $PRR \leq 10 \text{ MHz}$, $Z_o = 50 \Omega$.

D. The outputs are measured one at a time, with one transition per measurement.

E. t_{PLZ} and t_{PHZ} are the same as t_{dis} .

F. t_{PZL} and t_{PZH} are the same as t_{en} .

G. t_{PLH} and t_{PHL} are the same as t_{pd} .

H. All parameters and waveforms are not applicable to all devices.

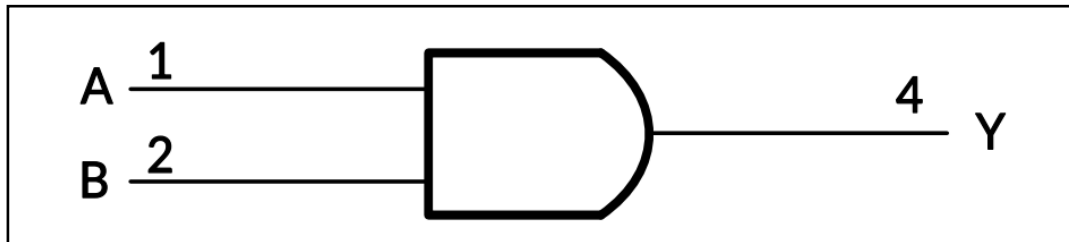


DETAILED DESCRIPTION

Overview

The SN74AHCT1G08 device is a single 2-input positive-AND gate. The device performs the Boolean AND function ($Y=A \bullet B$ or $Y= A + B$) in positive logic. Low I_{CC} current allows this device to be used in power sensitive or battery-powered applications. Robust inputs allow the device to up-translate with a propagation delay of 4.1 ns.

Functional Block Diagram



Feature Description

- The V_{CC} for the device is optimized at 5 V.
- The inputs accept V_{IH} levels of 2 V.
- Output ringing is minimized by slow edge rates.
- Inputs are TTL-Voltage compatible.

APPLICATION AND IMPLEMENTATION

Application Information

The SN74AHCT1G08 device is a single AND gate, which is often used for many common functions like power sequencing or an on LED indicator. Because the device is configured to output LOW unless all inputs are HIGH, an LED tied to the output of the device will only turn HIGH when all systems connected are sending a HIGH, or ready signal.

Design Requirements

This device uses CMOS technology and has balanced output drive. Take care to avoid bus contention because it can drive currents that would exceed maximum limits. The high drive also creates fast edges into light loads, so routing and load conditions must be considered to prevent ringing.



POWER SUPPLY RECOMMENDATIONS

The power supply pin should have a good bypass capacitor to prevent power disturbance. For devices with a single supply, a 0.1 μ F capacitor is recommended and if there are multiple V_{CC} terminals then 0.01 μ F or 0.022 μ F capacitors are recommended for each power terminal. It is acceptable to parallel multiple bypass caps to reject different frequencies of noise. The 0.1 μ F and 1 μ F capacitors are commonly used in parallel. The bypass capacitor should be installed as close to the power terminal as possible.

LAYOUT

Layout Guidelines

When using multiple bit logic devices inputs should not ever float. In many cases, functions or parts of functions of digital logic devices are unused; for example, when only two inputs of a triple-input AND gate are used or only 3 of the 4 buffer gates are used. Such input pins should not be left unconnected because the undefined voltages at the outside connections result in undefined operational states. Specified below are the rules that must be observed under all circumstances. All unused inputs of digital logic devices must be connected to a high or low bias to prevent them from floating. The logic level that should be applied to any particular unused input depends on the function of the device. Generally, they will be tied to GND or V_{CC} whichever make more sense or is more convenient.

Layout Example

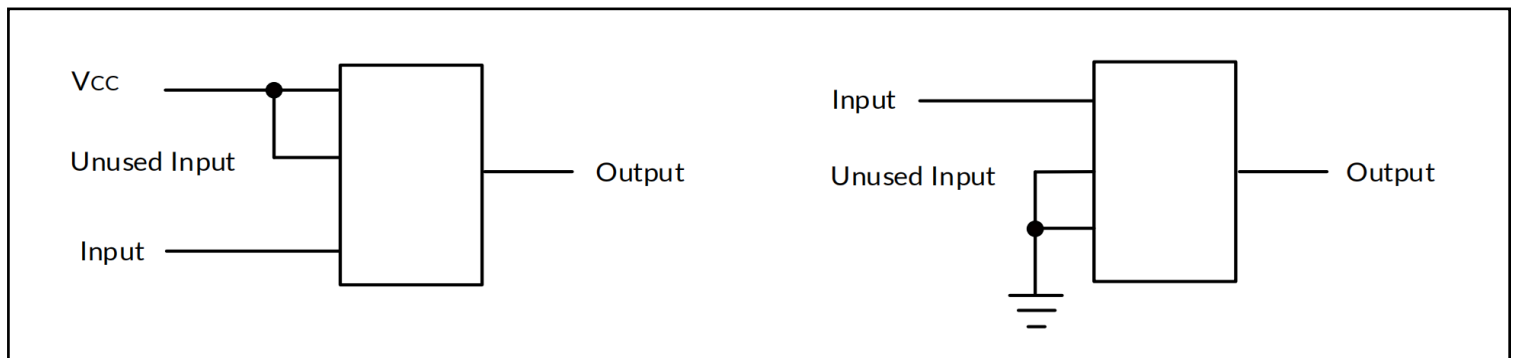


Figure 2. Layout Diagram



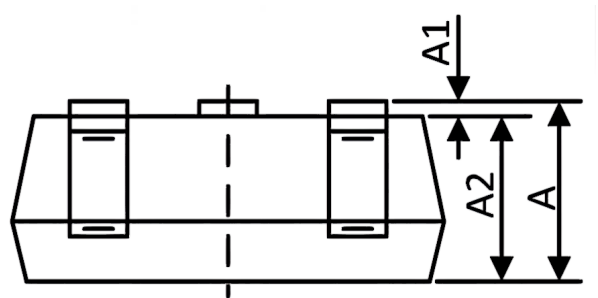
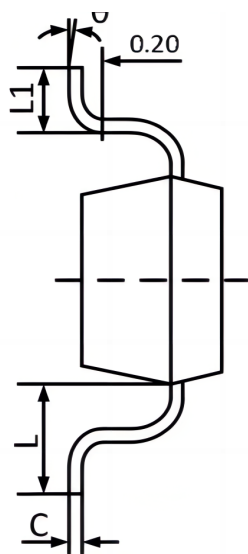
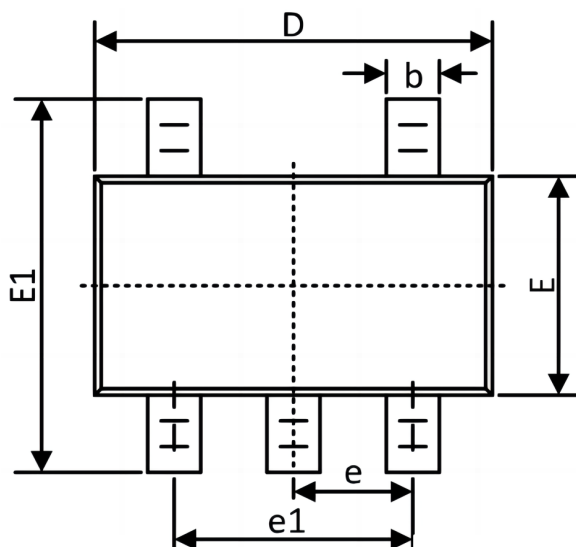
Order information

Order Number	Package	Package Quantity	Marking On The park	Temperature
SN74AHCT1G08DCKR-TUDI	SC70-5	Tape,Reel,3000	BEG	-40°C~125°C
SN74AHCT1G08DBVR-TUDI	SOT23-5	Tape,Reel,3000	B08S	

Revision history

Revision Number	Date	Revision	Page
V1.0	2018/7/10	New	1-15

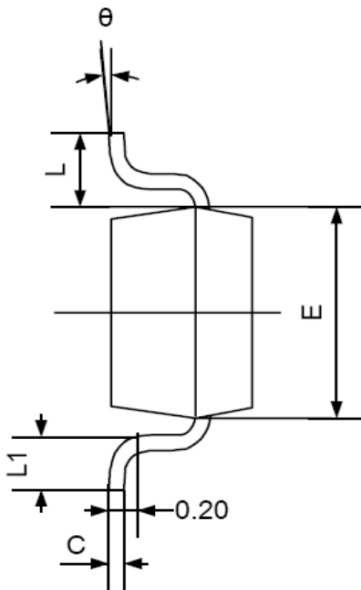
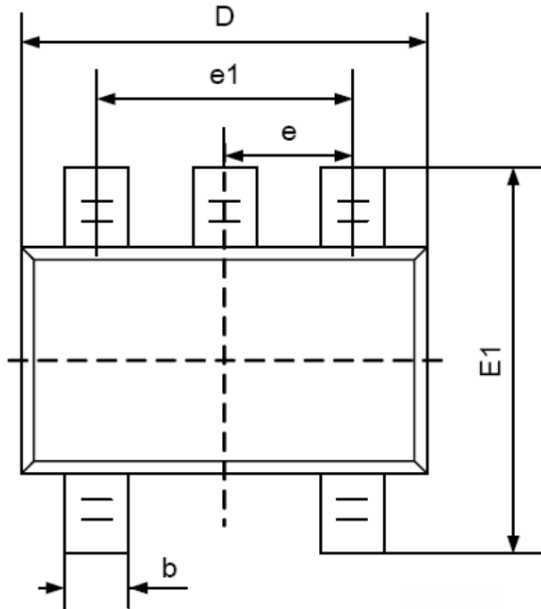
Package SOT23-5



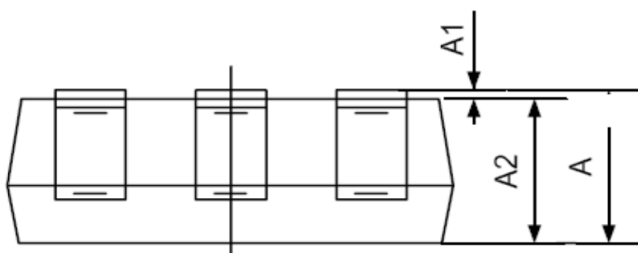
Symbol	Dimensions In Millimeters		Dimensions In Inches	
	MIN	MAX	MIN	MAX
A	1.050	1.250	0.041	0.049
A1	0.000	0.100	0.000	0.004
A2	1.050	1.150	0.041	0.045
b	0.300	0.400	0.012	0.016
C	0.100	0.200	0.004	0.008
D	2.820	3.020	0.111	0.119
E	1.500	1.700	0.059	0.067
E1	2.650	2.950	0.104	0.116
e	0.950TYP		0.037TYP	
e1	1.800	2.000	0.071	0.079
L	0.700REF		0.028REF	
L1	0.300	0.600	0.012	0.024
θ	0°	8°	0°	8°



Package SC70-5



Symbol	DimensionsIn Millimeters		DimensionsIn Inches	
	Min	Max	Min	Max
A	0.900	1.100	0.035	0.043
A1	0.000	0.100	0.000	0.004
A2	0.900	1.000	0.035	0.039
b	0.150	0.350	0.006	0.014
C	0.080	0.150	0.003	0.006
D	2.000	2.200	0.079	0.087
E	1.150	1.350	0.045	0.053
E1	2.150	2.450	0.085	0.096
e	0.650TYP		0.026TYP	
e1	1.200	1.400	0.047	0.055
L	0.525REF		0.021REF	
L1	0.260	0.460	0.010	0.018
theta	0°	8°	0°	8°





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