钍地半导体
Tudi Semiconductor

Product Specification

TUDI- SN74LVC1G02

Single 2-Input Positive-NOR Gate

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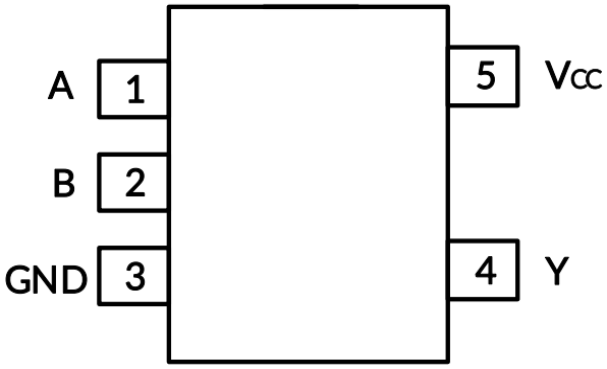
semiconductor device manufacturer

- Design
- research and development
- production
- and sales

FEATURES

- Operating Voltage Range: 1.65V to 5.5V
- Low Power Consumption: 0.1 μ A (TYP)
- Operating Temperature Range: -40 ° C to +125 ° C
- Inputs Accept Voltage to 5.5V
- High Output Drive: ±24mA at V_{cc}=3.0V
- Micro SIZE PACKAGES: SOT23-5, SC70-5



SOT23/SC70

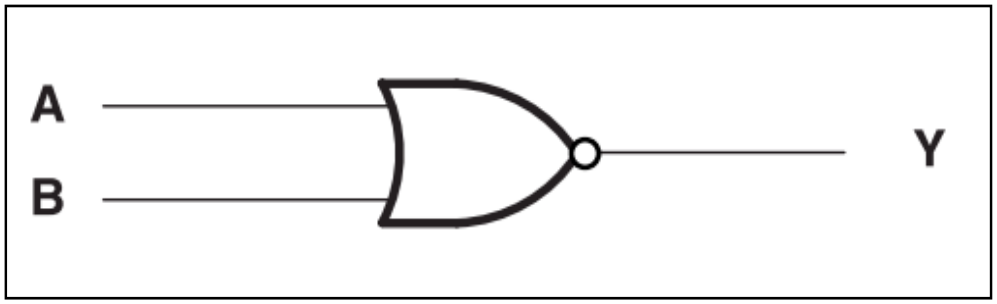
APPLICATIONS

- Active Noise Elimination
- Bar Code Scanner
- Blood Pressure Monitor
- CPAP Machine
- Fingerprint identification
- Network attached storage (NAS)

DESCRIPTIONS

The SN74LVC1G02 single 2-input positive-NOR gate is designed for 1.65V to 5.5V V_{CC} operation. The SN74LVC1G02 device performs the Boolean function Y=A+B or Y=A•B in positive logic. The device is fully specified for partial-power-down applications using I_{off}. The I_{off} circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down. The SN74LVC1G02 is available in Green SOT23-5 and SC70-5 packages. It operates over an ambient temperature range of -40 ° C to +125 ° C.

SIMPLIFIED SCHEMATIC



FUNCTION TABLE

INPUTS		OUTPUT
A	B	Y
H	H	L
L	H	L
H	L	L
L	L	H

Y=A+B
H=High Voltage Level
L=Low Voltage Level

PIN CONFIGURATION AND FUNCTIONS (TOP VIEW)

PIN	NAME	I/O	FUNCTION
1	A	I	Input
2	B	I	Input
3	GND	P	Ground
4	Y	O	Output
5	V_{cc}	P	Power pin

Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted) (1) (2)

		MIN	MAX	UNIT
V_{cc}	Supply voltage range	-0.5	6.5	V
V_I	Input voltage range(2)	-0.5	6.5	V
V_O	Voltage range applied to any output in the high-impedance or power-off state(2)	-0.5	6.5	V
V_O	Voltage range applied to any output in the high orlow state (2)(3)	-0.5	V_{cc}+0.5	V
I_{IK}	Input clamp current V_I <0		-50	mA
I_{ok}	Output clamp current V_O<0		-50	mA
I_O	Continuous output current		±50	mA
	Continuous current through V_{cc} or GND		±100	mA

Package Thermal Impedance

	PARAMETER	MIN	MAX	UNIT
θ_{JA}	Package thermal impedance (4)	SOT23-5 SC70-5	230 380	°C/W

Temperature

	PARAMETER	MIN	MAX	UNIT
Temperature	Junction temperature,T_J(5)	-65	150	℃
	Storage temperature,T_{stg}	-65	150	

ESD Ratings

The following ESD information is provided for handling of ESD-sensitive devices in an ESD protected area only.

	VALUE	UNIT
Human-Body Model(HBM)	±2000	V
Charged-Device Model (CDM)	±1000	
Machine Model(MM)	±200	

ESD SENSITIVITY CAUTION

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

NOTE:

(1) Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under Recommended Operating Conditions is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

(2) The input and output negative-voltage ratings may be exceeded if the input and output current ratings are observed.

(3) The value of V_{CC} is provided in the Recommended Operating Conditions table.

(4) The package thermal impedance is calculated in accordance with JESD-51.

(5) The maximum power dissipation is a function of $T_{J(MAX)}$, $R_{\theta JA}$, and T_A. The maximum allowable power dissipation at any ambient temperature is $P_D = (T_{J(MAX)} - T_A) / R_{\theta JA}$. All numbers apply for packages soldered directly onto a PCB.

ELECTRICAL CHARACTERISTICS

over recommended operating free-air temperature range (TYP values are at T_A = +25°C, Full=-40°C to 125°C, unless otherwise noted.) (1)

Recommended Operating Conditions

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	MAX	UNIT
Supply voltage	V_{CC}	Operating	1.65	5.5	V
		Data retention only	1.5		
High-level input voltage	V_{IH}	V_{CC}=1.65V to 1.95V	0.65×V_{CC}		V
		V_{CC}=2.3V to 2.7V	1.7		
		V_{CC}=3V to 3.6V	2		
		V_{CC}=4.5V to 5.5V	0.7×V_{CC}		
Low-level input voltage	V_{IL}	V_{CC}=1.65V to 1.95V		0.35×V_{CC}	V
		V_{CC}=2.3V to 2.7V		0.7	
		V_{CC}=3V to 3.6V		0.8	
		V_{CC}=4.5V to 5.5V		0.3×V_{CC}	
Input voltage	V_I		0	5.5	V
Output voltage	V_O		0	V_{CC}	V
Input transition rise or fall		V_{CC}=1.8V±0.15V,2.5V±0.2V		20	ns/V
	△t/△V	V_{CC}=3.3V±0.3V		10	
		V_{CC}=5V±0.5V		5	
Operating temperature	T_A		-40	125	℃

(1) All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation.

DC Characteristics

PARAMETER	TEST CONDITIONS	VCC	TEMP	MIN(2)	TYP(3)	MAX(2)	UNIT
V_{OH}	I_{OH}=-100μA	1.65V to 5.5V	Full	V_{CC}-0.1			V
	I_{OH}=-4mA	1.65V		1.2			
	I_{OH}=-8mA	2.3V		1.9			
	I_{OH}=-16mA			2.4			
	I_{OH}=-24mA	3V		2.3			
	I_{OH}=-32mA	4.5V		3.8			
V_{OL}	I_{OL}=100μA	1.65V to 5.5V	Full			0.1	V
	I_{OL}=4mA	1.65V				0.45	
	I_{OL}=8mA	2.3V				0.3	
	I_{OL}=16mA					0.4	
	I_{OL}=24mA	3V				0.55	
	I_{OL}=32mA	4.5V				0.55	
I_I A or B inputs	V_I=5.5V or GND	0V to 5.5V	+25℃		±0.1		μA
			Full			±5	
I_{off}	V_I or V_O=5.5V	0	+25℃		±0.1		μA
			Full			±10	
I_{CC}	V_I=5.5V or GND,I_O=0	1.65V to 5.5V	+25℃		0.1		μA
			Full			10	
△I_{CC}	One input at V_{CC}-0.6V, Other inputs at V_{CC} or GND	3V to 5.5V	Full			500	μA
C_i(Input Capacitance)	V_I=V_{CC} or GND	3.3V	+25℃		4		pF

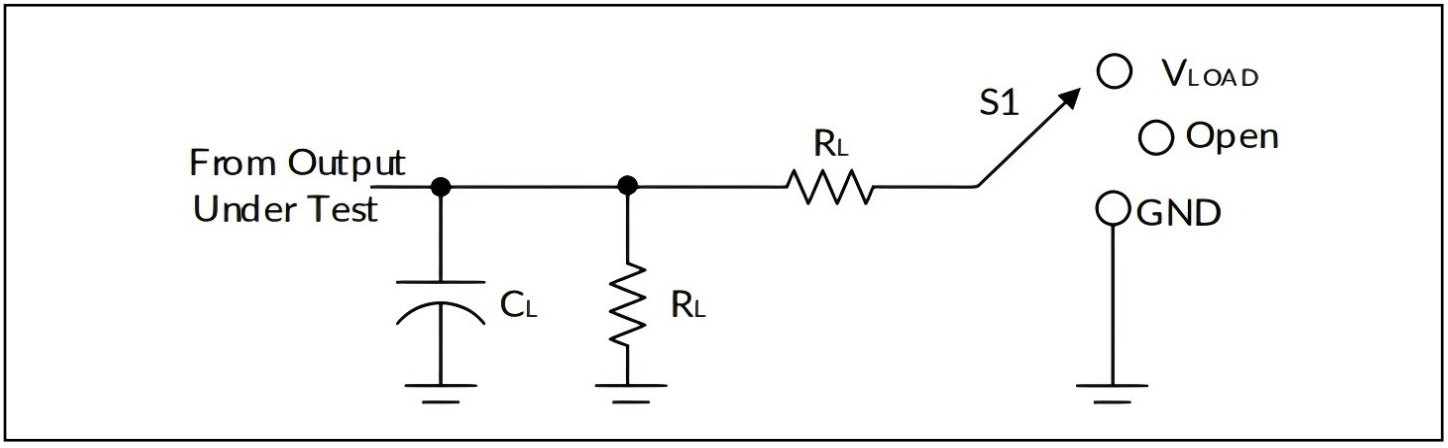
(1) All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation.
(2) Limits are 100% production tested at 25°C. Limits over the operating temperature range are ensured through correlations using statistical quality control (SQC) method.
(3) Typical values represent the most likely parametric norm as determined at the time of characterization. Actual typical values may vary over time and will also depend on the application and configuration.

AC Characteristics

PARAMETER	SYMBOL	TEST CONDITIONS		MIN(2)	TYP(3)	MAX(2)	UNIT
Propagation Delay	t_{pd}	V_{cc}=1.8V±0.15V	C_L=30pF,R_L=1kΩ		13.3		ns
		V_{cc}=2.5V±0.2V	C_L=30pF,R_L=500Ω		5.3		
		V_{cc}=3.3V±0.3V	C_L=50pF,R_L=500Ω		4.1		
		V_{cc}=5V±0.5V	C_L=50pF,R_L=500Ω		3.6		
Power dissipation capacitance	C_{pd}	V_{cc}=1.8V	f=10MHz		16		pF
		V_{cc}=2.5V			18		
		V_{cc}=3.3V			18		
		V_{cc}=5V			20		

(1) All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation.
(2) This parameter is ensured by design and/or characterization and is not tested in production.
(3) Typical values represent the most likely parametric norm as determined at the time of characterization. Actual typical values may vary over time and will also depend on the application and configuration.

PARAMETER MEASUREMENT INFORMATION



TEST	S1
t_{PLH}/t_{PHL}	Open
t_{pLz}/t_{pzL}	V_{LOAD}
t_{pHz}/t_{pZH}	GND

V_{CC}	INPUTS		V_M	V_{LOAD}	C_L	R_L	V_Δ
	V_I	t_r/t_f					
1.8V±0.15V	V_{CC}	≤2ns	$V_{CC}/2$	$2\times V_{CC}$	30pF	1kΩ	0.15V
2.5V±0.2V	V_{CC}	≤2ns	$V_{CC}/2$	$2\times V_{CC}$	30pF	500Ω	0.15V
3.3V±0.3V	3V	≤2.5ns	1.5V	6V	50pF	500Ω	0.3V
5V±0.5V	V_{CC}	≤2.5ns	$V_{CC}/2$	$2\times V_{CC}$	50pF	500Ω	0.3V

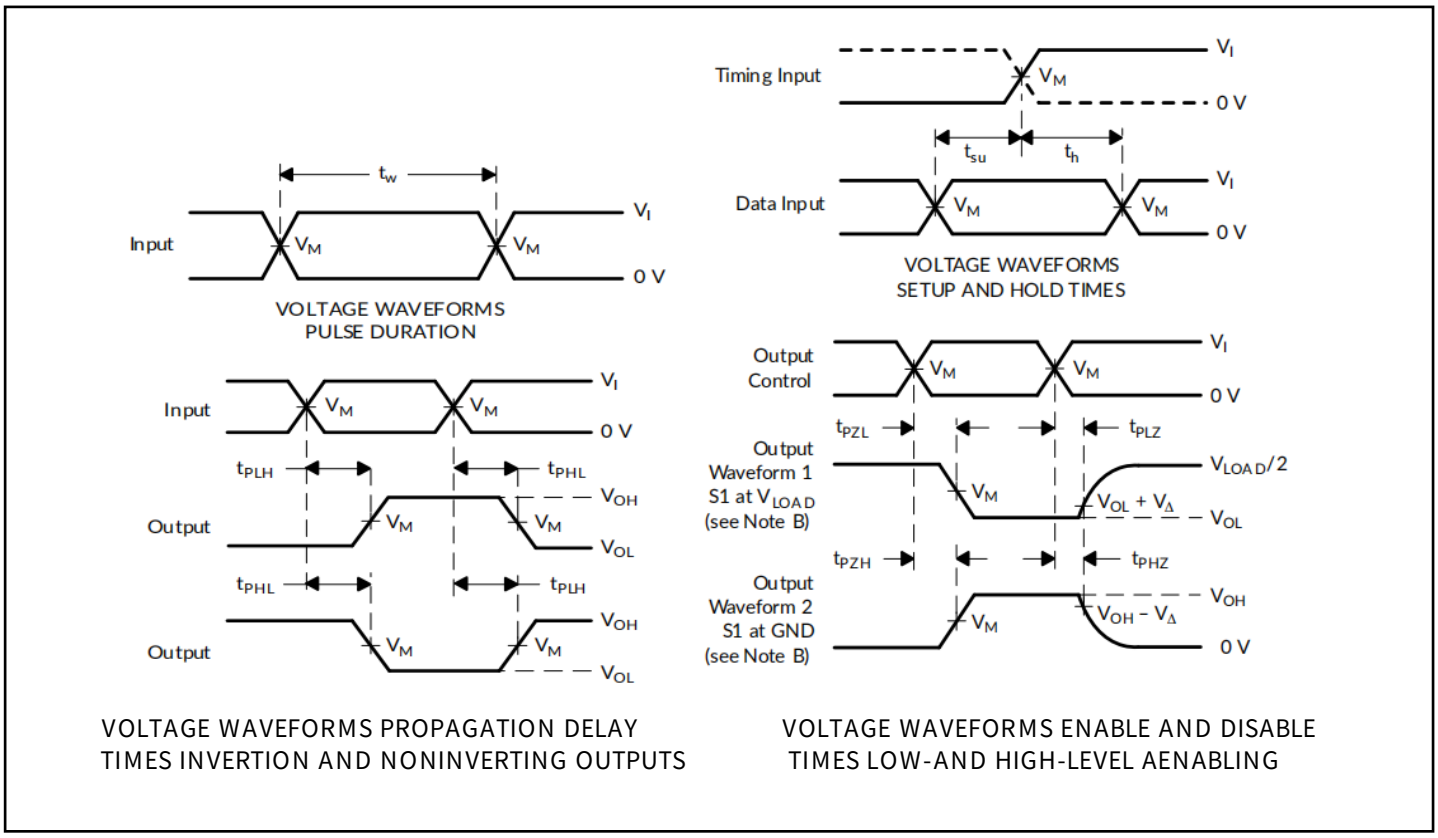


Figure 1. Load Circuit and Voltage Waveforms

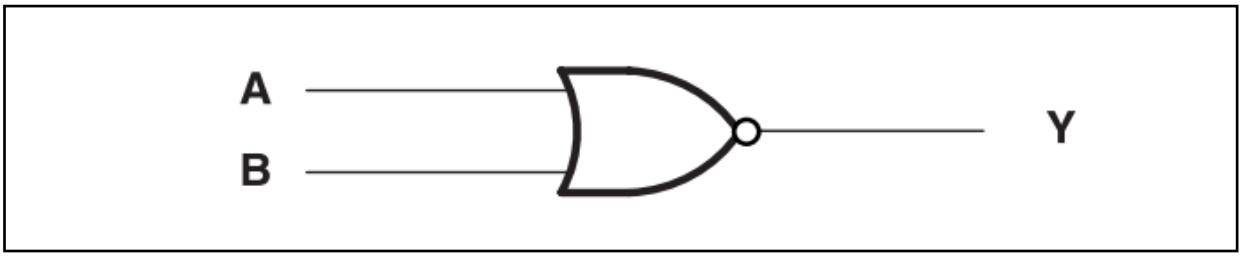
NOTES: A. CL includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, ZO = 50Ω.
D. The outputs are measured one at a time, with one transition per measurement.
E. t_{PLZ} and t_{PHZ} are the same as t_{dis}.
F. t_{PZL} and t_{PZH} are the same as t_{en}.
G. t_{PLH} and t_{PHL} are the same as t_{pd}.
H. All parameters and waveforms are not applicable to all devices.

DETAILED DESCRIPTION

Overview

The SN74LVC1G02 device contains one 2-input positive-NOR gate and performs the Boolean function Y=A+B or Y=A•B. This device is fully specified for partial-power-down applications using I_{off}. The I_{off} circuitry disables
the outputs, preventing damaging current backflow through the device when it is powered down.

Functional Block Diagram



Feature Description

- Wide operating voltage range.
  - Operates from 1.65 V to 5.5 V.
- Allows down voltage translation.
- Inputs accept voltages to 5.5 V.
- Ioff feature allows voltages on the inputs and outputs, when V_{cc} is 0 V.

APPLICATION AND IMPLEMENTATION

Application Information

The SN74LVC1G02 is a high drive CMOS device that can be used for implement NOR logic with a high output drive, such as an LED application. It can produce 24mA of drive current at 3.0V making it Ideal for driving multiple outputs and good for high speed applications up to 100MHz. The inputs are 5.5V tolerant allowing translation down to V_{cc}.

Design Requirements

This device uses CMOS technology and has balanced output drive. Care should be taken to avoid bus contention because it can drive currents that would exceed maximum limits. The high drive will also create fast edges into light loads, so routing and load conditions should be considered to prevent ringing.

POWER SUPPLY RECOMMENDATIONS

The power supply pin should have a good bypass capacitor to prevent power disturbance. For devices with a single supply, a 0.1 μF capacitor is recommended and if there are multiple V_{CC} terminals then 0.01 μF or 0.022 μF capacitors are recommended for each power terminal. It is acceptable to parallel multiple bypass caps to reject different frequencies of noise. The 0.1 μF and 1 μF capacitors are commonly used in parallel. The bypass capacitor should be installed as close to the power terminal as possible.

LAYOUT

Layout Guidelines

When using multiple bit logic devices inputs should not ever float. In many cases, functions or parts of functions of digital logic devices are unused; for example, when only two inputs of a triple -input AND gate are used or only 3 of the 4 buffer gates are used. Such input pins should not be left unconnected because the undefined voltages at the outside connections result in undefined operational states. Specified below are the rules that must be observed under all circumstances. All unused inputs of digital logic devices must be connected to a high or low bias to prevent them from floating. The logic level that should be applied to any particular unused input depends on the function of the device. Generally, they will be tied to GND or V_{CC} whichever makemore sense or is more convenient

Layout Example

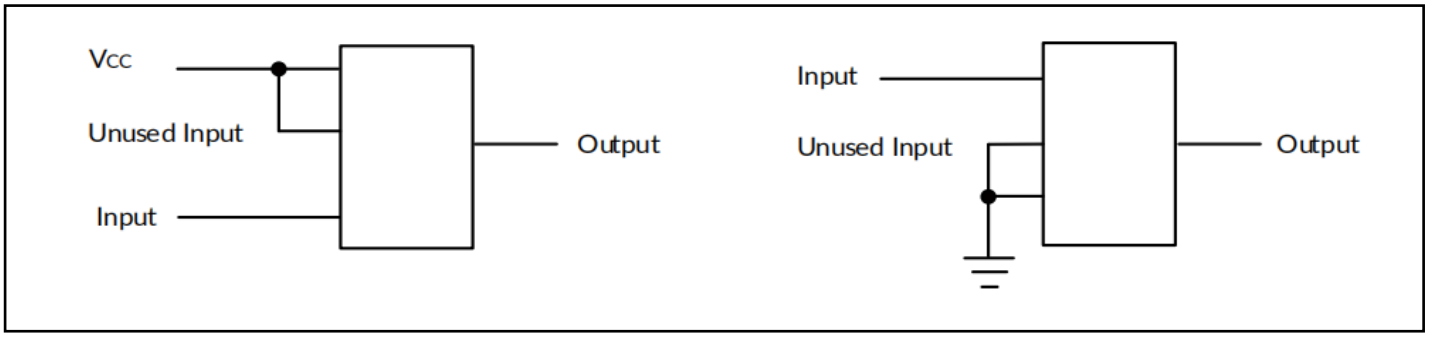


Figure 2. Layout Diagram

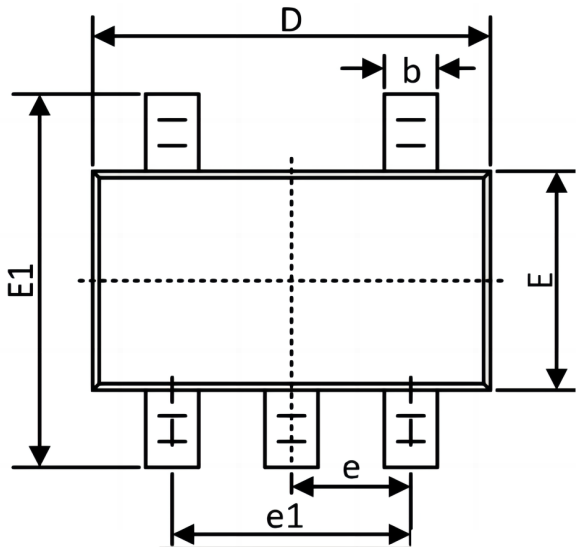
Order information

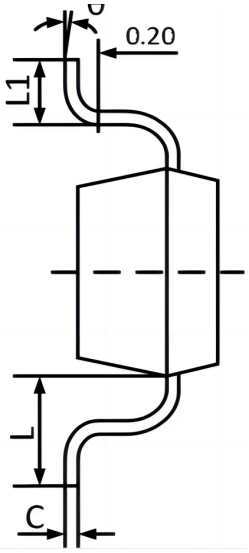
Order Number	Package	Package Quantity	Marking On The park	Temperature
SN74LVC1G02DCKR-TUDI	SC70-5	Tape,Reel,3000	ICBK	-40°C~125°C
SN74LVC1G02DBVR-TUDI	SOT23-5	Tape,Reel,3000	C02J	

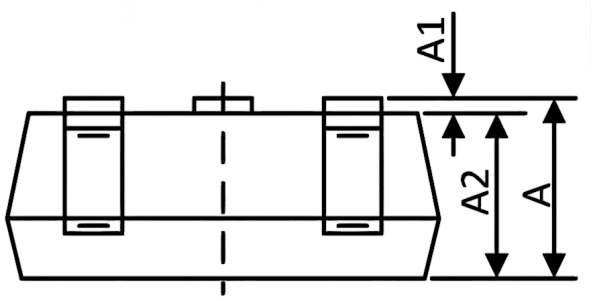
Revision history

Revison Number	Date	Revision	Page
V1.0	2018/7/10	New	1-15

Package SOT23-5

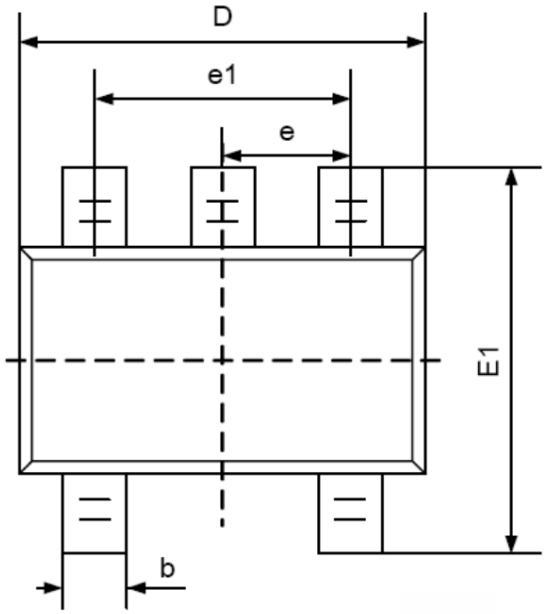


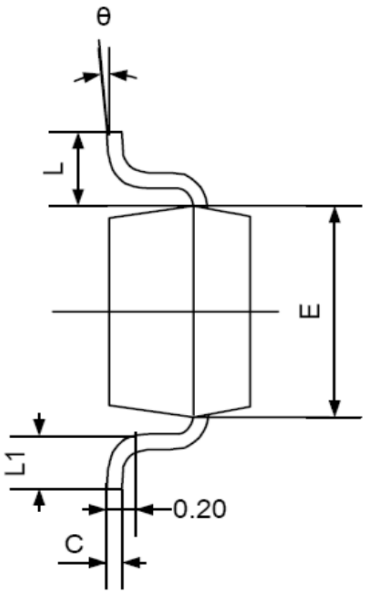


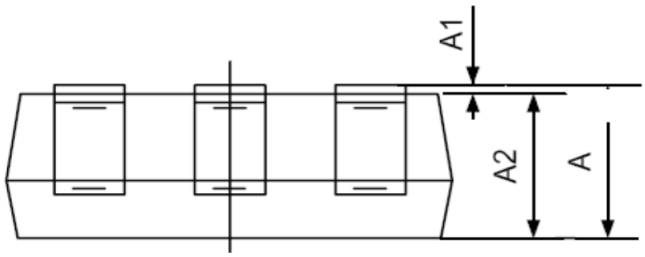


Symbol	Dimensions In Millimeters		Dimensions In Inches	
	MIN	MAX	MIN	MAX
A	1.050	1.250	0.041	0.049
A1	0.000	0.100	0.000	0.004
A2	1.050	1.150	0.041	0.045
b	0.300	0.400	0.012	0.016
C	0.100	0.200	0.004	0.008
D	2.820	3.020	0.111	0.119
E	1.500	1.700	0.059	0.067
E1	2.650	2.950	0.104	0.116
e	0.950TYP		0.037TYP	
e1	1.800	2.000	0.071	0.079
L	0.700REF		0.028REF	
L1	0.300	0.600	0.012	0.024
θ	0°	8°	0°	8°

Package SC70-5







Symbol	DimensionsIn Millimeters		DimensionsIn Inches	
	Min	Max	Min	Max
A	0.900	1.100	0.035	0.043
A1	0.000	0.100	0.000	0.004
A2	0.900	1.000	0.035	0.039
b	0.150	0.350	0.006	0.014
C	0.080	0.150	0.003	0.006
D	2.000	2.200	0.079	0.087
E	1.150	1.350	0.045	0.053
E1	2.150	2.450	0.085	0.096
e	0.650TYP		0.026TYP	
e1	1.200	1.400	0.047	0.055
L	0.525REF		0.021REF	
L1	0.260	0.460	0.010	0.018
θ	0°	8°	0°	8°

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