



钜地半导体
Tudi Semiconductor

Product Specification

TUDI-SN74LVC2G34

Dual Buffer Gate

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用芯智造 · 卓越品质

**semiconductor device
manufacturer**

- Design
- research and development
- production
- and sales



FEATURES

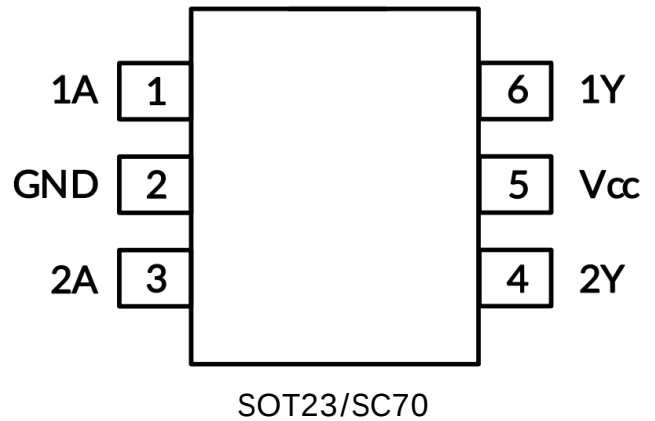
- Operating Voltage Range: 1.65V to 5.5V
- Low Power Consumption: 0.1 μ A (TYP)
- Operating Temperature Range:
-40°C to +125°C
- Inputs Accept Voltage to 5.5V
- High Output Drive: $\pm$ 24mA at V_{CC} =3.0V
- I_{off} Supports Partial-Power-Down Mode Operation
- Micro Size Packages: SOT23-6, SC70-6

APPLICATIONS

- AC Receiver
- Blu-ray Players and Home Theaters
- Desktops or Notebook PCs
- Digital Video Cameras (DVC)
- Mobile Phones
- Personal Navigation Device (GPS)
- Portable Media Player

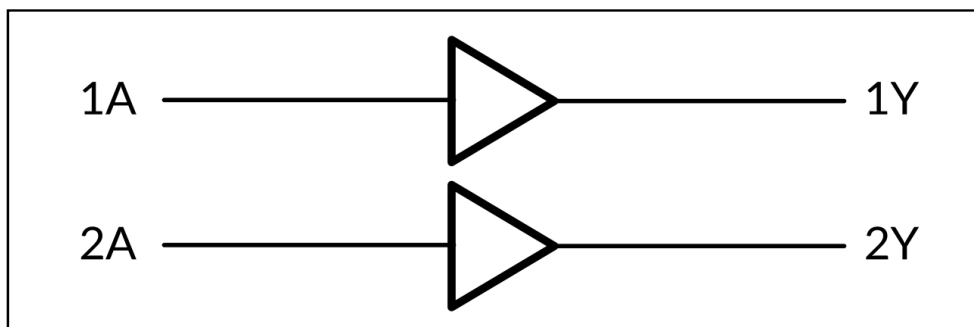
DESCRIPTIONS

The SN74LVC2G34 dual buffer gate is designed for 1.65V to 5.5V V_{CC} operation. The SN74LVC2G34 device performs the Boolean function $Y=A$ in positive logic. The CMOS device has high output drive while maintaining low static power dissipation over a broad V_{CC} operating range. The SN74LVC2G34 is available in Green SOT23-6 and SC70-6 packages. It operates over an ambient temperature range of -40°C to +125°C





LOGIC SYMBOL



FUNCTION TABLE

INPUT	OUTPUT
A	Y
H	H
L	L

Y=A

H=High Voltage Level

L=Low Voltage Level

PIN CONFIGURATION AND FUNCTIONS

PIN	NAME	I/O	FUNCTION
1	1A	I	Input 1
2	GND	P	Ground
3	2A	I	Input 2
4	2Y	O	Output 2
5	V _{CC}	P	Supply Power
6	1Y	O	Output 1



Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted) (1) (2)

		MIN	MAX	UNIT
V_{CC}	Supply voltage range	-0.5	6.5	V
V_I	Input voltage range(2)	-0.5	6.5	V
V_O	Voltage range applied to any output in the high-impedance or power-off state(2)	-0.5	6.5	V
V_O	Voltage range applied to any output in the high or low state (2)(3)	-0.5	$V_{CC}+0.5$	V
I_{IK}	Input clamp current $V_I < 0$		-50	mA
I_{OK}	Output clamp current $V_O < 0$		-50	mA
I_O	Continuous output current		± 50	mA
	Continuous current through V_{CC} or GND		± 100	mA

Package Thermal Impedance

	PARAMETER		MIN	MAX	UNIT
θ_{JA}	Package thermal impedance (4)	SOT23-6		230	/W
		SC70-6		265	

Temperature

	PARAMETER	MIN	MAX	UNIT
Temperature	Junction temperature, T_J (5)	-65	150	
	Storage temperature, T_{stg}	-65	150	



ESD Ratings

The following ESD information is provided for handling of ESD-sensitive devices in an ESD protected area only.

	VALUE	UNIT
Human-Body Model(HBM)	± 4000	V
Charged-Device Model (CDM)	±1500	
Machine Model(MM)	±200	

ESD SENSITIVITY CAUTION



ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

NOTE:

- (1) Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under Recommended Operating Conditions is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) The input and output negative-voltage ratings may be exceeded if the input and output current ratings are observed.
- (3) The value of V_{CC} is provided in the Recommended Operating Conditions table.
- (4) The package thermal impedance is calculated in accordance with JEDEC-51.
- (5) The maximum power dissipation is a function of $T_{J(MAX)}$, $R_{\theta JA}$, and T_A . The maximum allowable power dissipation at any ambient temperature is $P_D = (T_{J(MAX)} - T_A) / R_{\theta JA}$. All numbers apply for packages soldered directly onto a PCB.



ELECTRICAL CHARACTERISTICS

over recommended operating free-air temperature range (TYP values are at $T_A = +25^{\circ}\text{C}$, Full=-40°C to 125°C, unless otherwise noted.)⁽¹⁾

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	MAX	UNIT
Supply Voltage	V_{CC}	Operating	1.65	5.5	V
		Data retention only	1.5		
High-Level Input Voltage	V_{IH}	$V_{CC}=1.65\text{V to }1.95\text{V}$	$0.65 \times V_{CC}$		V
		$V_{CC}=2.3\text{V to }2.7\text{V}$	1.7		
		$V_{CC}=3\text{V to }3.6\text{V}$	2		
		$V_{CC}=4.5\text{V to }5.5\text{V}$	$0.7 \times V_{CC}$		
Low-Level Input Voltage	V_{IL}	$V_{CC}=1.65\text{V to }1.95\text{V}$		$0.35 \times V_{CC}$	V
		$V_{CC}=2.3\text{V to }2.7\text{V}$		0.7	
		$V_{CC}=3\text{V to }3.6\text{V}$		0.8	
		$V_{CC}=4.5\text{V to }5.5\text{V}$		$0.3 \times V_{CC}$	
Input Voltage	V_I		0	5.5	V
Output Voltage	V_O		0	V_{CC}	V
Input Transition Rise or Fall	t/V	$V_{CC}=1.8\text{V} \pm 0.15\text{V},$ $2.5\text{V} \pm 0.2\text{V}$		20	ns/V
		$V_{CC}=3.3\text{V} \pm 0.3\text{V}$		10	
		$V_{CC}=5\text{V} \pm 0.5\text{V}$		5	
Operating Temperature	T_A		-40	+125	

(1) All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation.



DC Characteristics

PARAMETER	TEST CONDITIONS	V _{CC}	TEMP	MIN(2)	TYP(3)	MAX(2)	UNIT
V _{OH}	I _{OH} = -100μA	1.65V to 5.5V	Full	V _{CC} -0.1			V
	I _{OH} = -4mA	1.65V		1.2			
	I _{OH} = -8mA	2.3V		1.9			
	I _{OH} = -16mA	3V		2.4			
	I _{OH} = -24mA			2.3			
	I _{OH} = -32mA	4.5V		3.8			
V _{OL}	I _{OL} =100μA	1.65V to 5.5V	Full			0.1	V
	I _{OL} =4mA	1.65V				0.45	
	I _{OL} =8mA	2.3V				0.3	
	I _{OL} =16mA	3V				0.4	
	I _{OL} =24mA					0.55	
	I _{OL} =32mA	4.5V				0.55	
I _I A inputs	V _I =5.5V or GND	0V to 5.5V	+25		±0.1		μA
			Full			±5	
I _{off}	V _I or V _O =5.5V	0	+25		±0.1		μA
			Full			±10	
I _{CC}	V _I =5.5V or GND, I _O =0	1.65V to 5.5V	+25		0.1		μA
			Full			10	
I _{CC}	One input at V _{CC} -0.6V, Other inputs at V _{CC} or GND	3V to 5.5V	Full			500	μA
C _i (Input Capacitance)	V _I =V _{CC} or GND	3.3V	+25		4		pF

(1) All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation.

(2) Limits are 100% production tested at 25°C. Limits over the operating temperature range are ensured through correlations using statistical quality control (SQC) method.

(3) Typical values represent the most likely parametric norm as determined at the time of characterization. Actual typical values may vary over time and will also depend on the application and configuration.



AC Characteristics

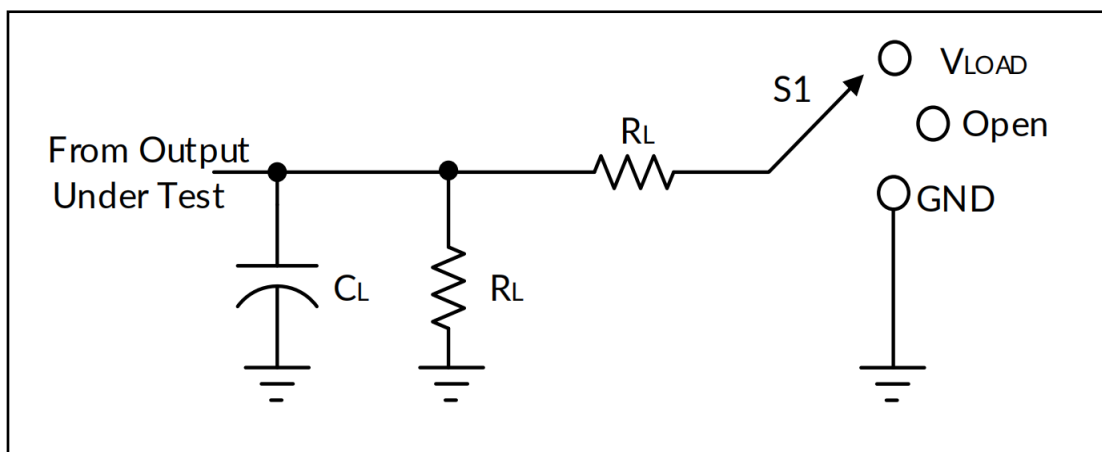
PARAMETER	SYMBOL	TEST CONDITIONS		MIN(2)	TYP(3)	MAX(2)	UNIT
Propagation Delay	t_{pd}	$V_{CC}=1.8V\pm0.15V$	$C_L=30pF, R_L=1k\Omega$		13.3		ns
		$V_{CC}=2.5V\pm0.2V$	$C_L=30pF, R_L=500\Omega$		5.3		
		$V_{CC}=3.3V\pm0.3V$	$C_L=50pF, R_L=500\Omega$		4.2		
		$V_{CC}=5V\pm0.5V$	$C_L=50pF, R_L=500\Omega$		3.4		
Power Dissipation Capacitance	C_{pd}	$V_{CC}=1.8V$	$f=10MHz$		16		pF
		$V_{CC}=2.5V$			18		
		$V_{CC}=3.3V$			18		
		$V_{CC}=5V$			20		

(1) All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation.

(2) This parameter is ensured by design and/or characterization and is not tested in production.

(3) Typical values represent the most likely parametric norm as determined at the time of characterization. Actual typical values may vary over time and will also depend on the application and configuration.

PARAMETER MEASUREMENT INFORMATION



TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	V_{LOAD}
t_{PHZ}/t_{PZH}	GND



INPUTS

V_{CC}	V_I	t_r/t_f	V_M	V_{LOAD}	C_L	R_L	V
$1.8V \pm 0.15V$	V_{CC}	$\leq 2ns$	$V_{CC}/2$	$2 \times V_{CC}$	30pF	1k Ω	0.15V
$2.5V \pm 0.2V$	V_{CC}	$\leq 2ns$	$V_{CC}/2$	$2 \times V_{CC}$	30pF	500 Ω	0.15V
$3.3V \pm 0.3V$	3V	$\leq 2.5ns$	1.5V	6V	50pF	500 Ω	0.3V
$5V \pm 0.5V$	V_{CC}	$\leq 2.5ns$	$V_{CC}/2$	$2 \times V_{CC}$	50pF	500 Ω	0.3V

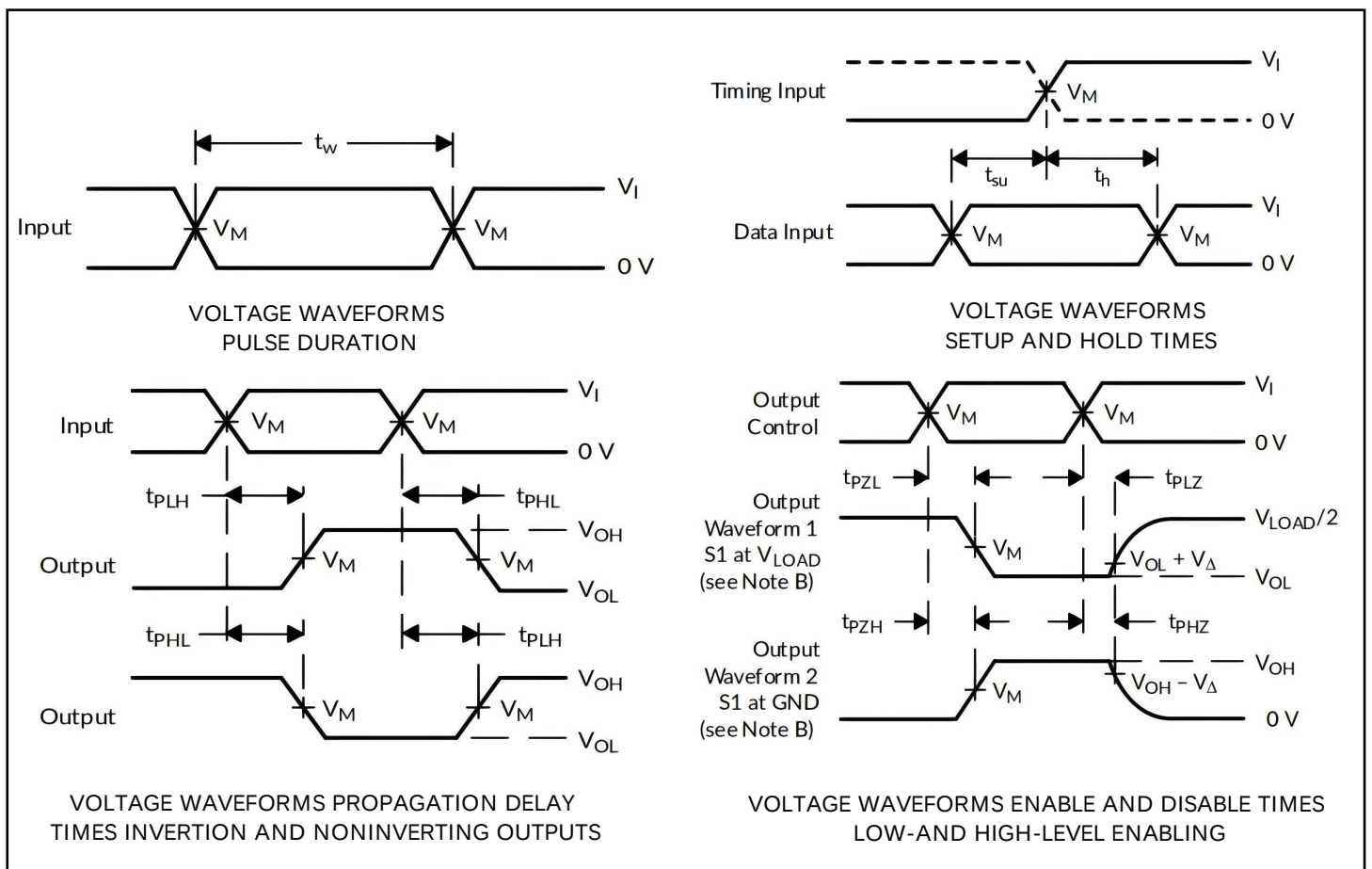


Figure 1. Load Circuit and Voltage Waveforms

NOTES: A. C_L includes probe and jig capacitance.

B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.

C. All input pulses are supplied by generators having the following characteristics: $PRR \leq 10\text{ MHz}$, $Z_o = 50\ \Omega$.

D. The outputs are measured one at a time, with one transition per measurement.

E. t_{PLZ} and t_{PHZ} are the same as t_{dis} .

F. t_{PZL} and t_{PZH} are the same as t_{en} .

G. t_{PLH} and t_{PHL} are the same as t_{pd} .

H. All parameters and waveforms are not applicable to all devices

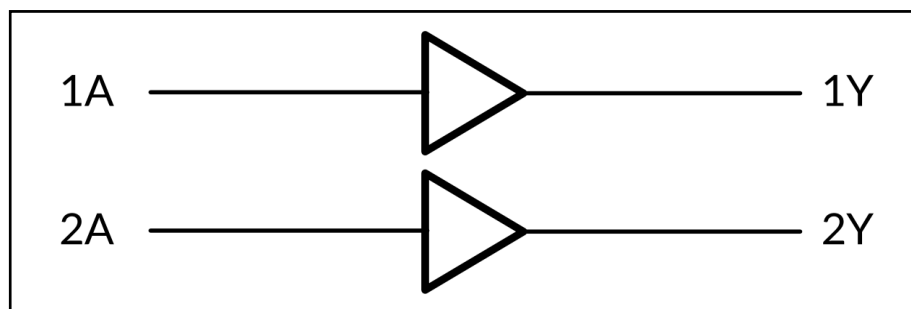


DETAILED DESCRIPTION

Overview

The SN74LVC2G34 device contains one buffer gate device and performs the Boolean function $Y = A$. This device is fully specified for partial-power-down applications using I_{off} . The I_{off} circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down

Functional Block Diagram



Feature Description

- Wide operating voltage range.
 - Operates from 1.65 V to 5.5 V.
- Allows down voltage translation.
- Inputs accept voltages to 5.5 V.
- I_{off} feature allows voltages on the inputs and outputs when V_{cc} is 0 V.

APPLICATION AND IMPLEMENTATION

Application Information

The SN74LVC2G34 is a high drive CMOS device that can be used as a buffer with a high output drive, such as an LED application. It can produce 24 mA of drive current at 3.0 V making it ideal for driving multiple outputs and good for high speed applications up to 100MHz. The inputs are 5.5 V tolerant allowing it to translate down to V_{cc} .

Design Requirements

This device uses CMOS technology and has balanced output drive. Care should be taken to avoid bus contention because it can drive currents that would exceed maximum limits. The high drive will also create fast edges into light loads so routing and load conditions should be considered to prevent ringing.



POWER SUPPLY RECOMMENDATIONS

The power supply pin should have a good bypass capacitor to prevent power disturbance. For devices with a single supply, a $0.1\mu\text{F}$ capacitor is recommended and if there are multiple V_{CC} terminals then $0.01\mu\text{F}$ or $0.022\mu\text{F}$ capacitors are recommended for each power terminal. It is acceptable to parallel multiple bypass caps to reject different frequencies of noise. The $0.1\mu\text{F}$ and $1\mu\text{F}$ capacitors are commonly used in parallel. The bypass capacitor should be installed as close to the power terminal as possible.

LAYOUT

Layout Guidelines

When using multiple bit logic devices inputs should not ever float. In many cases, functions or parts of functions of digital logic devices are unused; for example, when only two inputs of a triple-input AND gate are used or only 3 of the 4 buffer gates are used. Such input pins should not be left unconnected because the undefined voltages at the outside connections result in undefined operational states. Specified below are the rules that must be observed under all circumstances. All unused inputs of digital logic devices must be connected to a high or low bias to prevent them from floating. The logic level that should be applied to any particular unused input depends on the function of the device. Generally, they will be tied to GND or V_{CC} whichever make more sense or is more convenient.

Layout Example

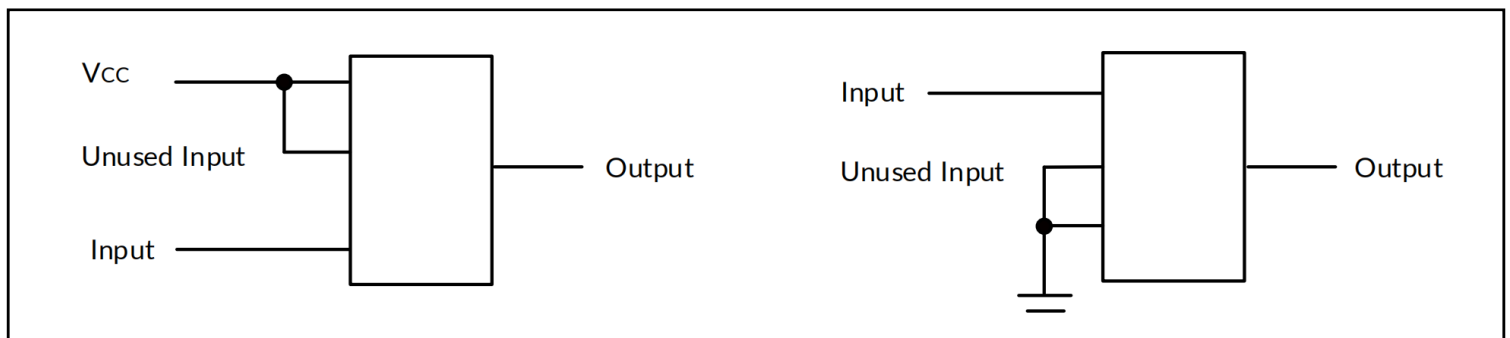


Figure 2. Layout Diagram



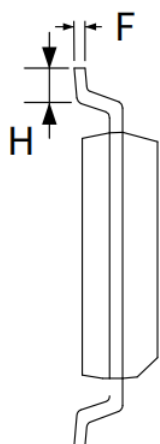
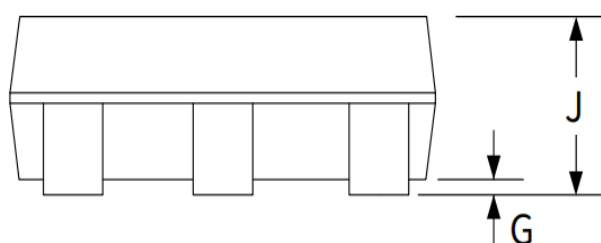
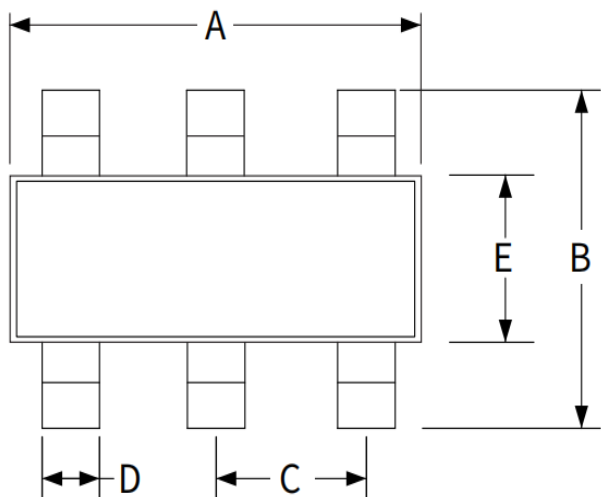
ORDERING INFORMATION

Order Number	Package	Package Quantity	Marking On The park	Temperature
SN74LVC2G34DCKR-TUDI	SC70-6	Tape,Reel,3000	C9F	-40°C~125°C
SN74LVC2G34DBVR-TUDI	SOT23-6	Tape,Reel,3000	C345	

Revision history

	Date	Revision	Page
V1.0	2018/4/5	New	1-15

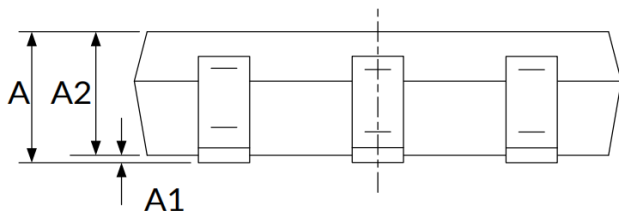
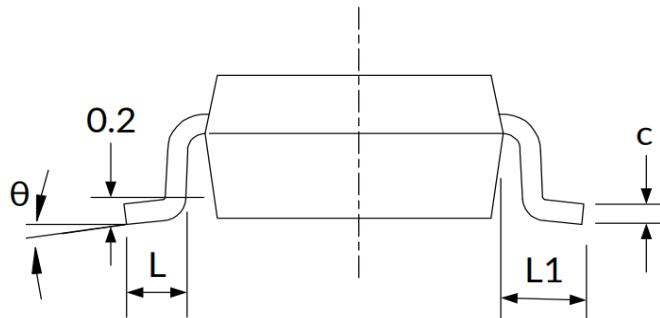
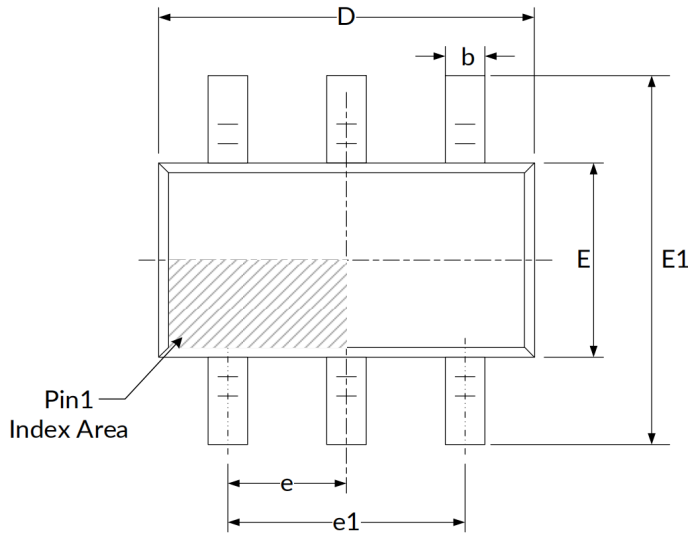
Package SOT23-6



Symbol	Dimen Millimeters		sions Inches	
	Min.	Max.	Min.	Max.
A	2.80	3.00	0.110	0.118
B	2.60	3.00	0.102	0.118
C	0.93	0.97	0.037	0.038
D	0.41		0.016	
E	1.50	1.70	0.059	0.067
F	0.11	0.19	0.004	0.007
G	-	0.10	-	0.004
H	0.40	-	0.016	-
J	1.00	1.20	0.035	0.057



Package SC70-6



Symbol	DimensionsIn Millimeters			
	DimensionsIn Inches			
	Min	Max	Min	Max
A(1)	0.900	1.100	0.035	0.043
A1	0.000	0.100	0.000	0.004
A2	0.900	1.000	0.035	0.039
b	0.150	0.350	0.006	0.014
C	0.080	0.150	0.003	0.006
D(1)	2.000	2.200	0.079	0.087
E(1)	1.150	1.350	0.045	0.053
E1	2.150	2.450	0.085	0.096
e	0.650(BSC)(2)			
e1	1.300(BSC)(2)		0.051(BSC)(2)	
L	0.260	0.460	0.01	0.018
L1	0.525		0.021	
θ	0°	8°	0°	8°



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