TDDR4008JA
DDR4 DRAM 1GB（512M×16bit）

General Description

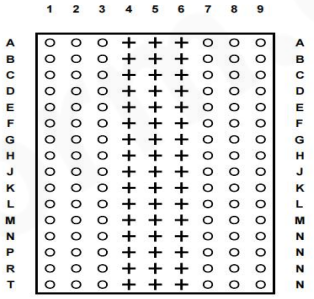
This document describes Biwin's TGDR4008JA 8Gb DDR4-3200 DRAM product comply with Commercial-Level grade.

The transfer rates of 8Gb DDR4 can be up to 3200Mbps for general applications which requires large memory density and high bandwidth. The chip is designed to comply with the following key DDR4 SDRAM feature such as posted CAS, Programmable CWL, Internal (Self) Calibration, On Die Termination supported and Asynchronous Reset.

Features

- 96 Ball（9*14mm）
- Fast data transfer rates: PC4-3200
- 8Gb (512M x 16bit)
- VDD = VDDQ = 1.2V +/- 0.06V
- VPP = 2.5V (2.375V~2.75V)
- 8Gb DDR4 SDRAM x8 = 16 Banks (4 bank group) / 8Gb DDR4 SDRAM x16 = 8 Banks (2 bank group)
- 8-bit pre-fetch
- Burst length of 8 and burst chop of 4
- Bi-directional / Differential Data-Strobe
- On Die Termination supported
- Asynchronous Reset
- ZQ calibration supported
- Programmable CAS Latency (posted CAS): 10,11,12,13,14,15,16,17,18,19,20,21,22
- Low Power Self Refresh mode is supported
- PPR mode supported
- All of products are compliance with the RoHS directive

Options



- Operating temperature
  – Commercial (**0°C** ≤ T_{OPER} ≤ **+85°C**)
- Storage temperature
  – -55°C ≤ T_{STG} ≤ +100°C

Note：
1. PPR mode is only supported in X16 configuration
2. PPR mode is supported at Precharge ALL.
3. TEN mode is only supported in X16 configuration
4. TDQS mode is NOT supported in X8 configuration

Biwin Confidential

Contents

1. Ordering Information and Key Features

1）Ordering Information

Part Number	Capacity	Organization	Component Composition	Number of Rank
TDDR4008JA	8Gb	512M×16bit	NA	NA

Note :

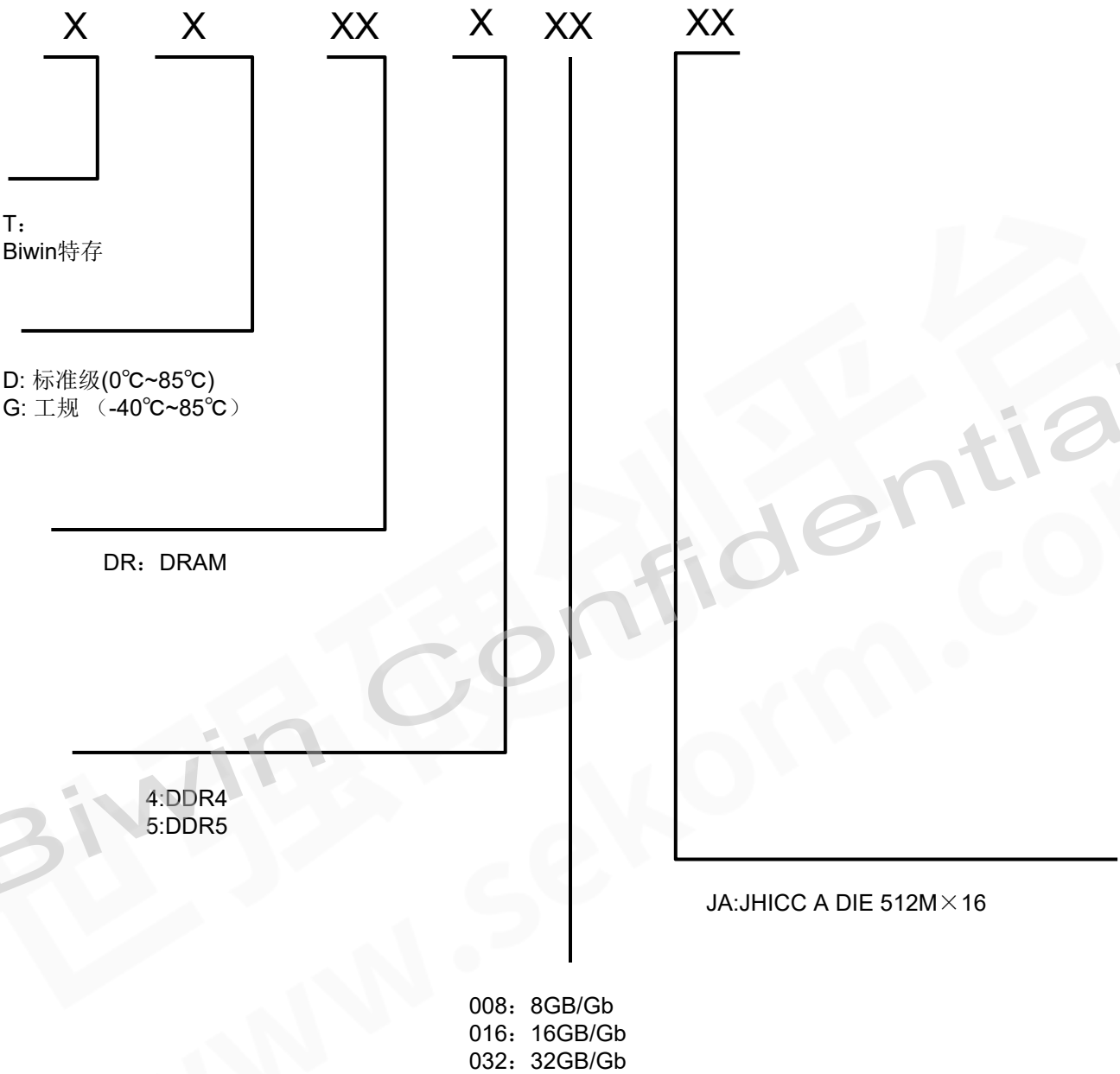
Average Refresh Cycle (Tcase of 0℃~ 95℃)
- 7.8 μs at 0℃ ~ 85℃
- 3.9 μs at 85℃ ~ 95℃.

2）Key Features

Grade	Speed (Mbps)	tCK (ns)	CAS Latency (tCK)	tRCD (ns)	tRP (ns)	tRAS (ns)	tRC (ns)	CL-tRCD-tRP
1600K	1600	1.25	11	13.75	13.75	35	48.75	11-11-11
1866M	1866	1.071	13	13.92	13.92	34	47.92	13-13-13
2133P	2133	0.937	15	14.04	14.04	33	47.06	15-15-15
2400T	2400	0.833	17	14.16	14.16	32	46.16	17-17-17
2666V	2666	0.75	19	14.25	14.25	32	46.25	19-19-19
2933Y	2933	0.682	21	14.32	14.32	32	46.32	21-21-21
3200AA	3200	0.625	22	13.75	13.75	32	45.75	22-22-22

2. 8Gb DDR4 Addressing

Parameter	512M×16bit
# of Bank Groups	2
BG Address	BG0
Bank Address in a BG	BA0~BA1
Row Address	A0~A15
Column Address	A0~A9
Page size	2KB



Biwin Confidential
www.sekorm.com

3. Absolute Maximum Ratings

Symbol	Parameter	Min	Max	Units	Notes
V_{DD}	V_{DD} supply voltage relative to V_{SS}	–0.3	1.5	V	
V_{DDQ}	V_{DDQ} supply voltage relative to V_{SS}	–0.3	1.5	V	
V_{PP}	Voltage on V_{PP} pin relative to V_{SS}	–0.3	3	V	
V_{IN}, V_{OUT}	Voltage on any pin relative to V_{SS}	–0.3	1.5	V	

4.Operating Conditions

Symbol	Parameter	Min	Nom	Max	Units	Notes
V_{DD}	Supply voltage	1.14	1.2	1.26	V	1,2,3
V_{DDQ}	Supply Voltage for Output	1.14	1.2	1.26	V	1,2,3
V_{PP}	Peak-to-Peak Voltage	2.375	2.5	2.75	V	3

Note:
1. Under all conditions V_{DDQ} must be less than or equal to V_{DD}.
2. V_{DDQ} tracks with V_{DD}. AC parameters are measured with V_{DD} and V_{DDQ} tied together.
3. DC bandwidth is limited to 2

BIWIN Confidential www.sekorm.com

5. Architecture

x16 Package Ball out (Top view) : 96ball FBGA Package

	1	2	3	4	5	6	7	8	9	
A	VDD	VSSQ	DQU0				DQSU_c	VSSQ	VDDQ	A
B	VPP	VSS	VDD				DQSU_t	DQU1	VDD	B
C	VDDQ	DQU4	DQU2				DQU3	DQU5	VSSQ	C
D	VDD	VSSQ	DQU6				DQU7	VSSQ	VDDQ	D
E	VSS	DMU_n/ DBIU_n	VSSQ				DML_n DBIL_n	VSSQ	VSS	E
F	VSSQ	VDDQ	DQSL_c				DQL1	VDDQ	ZQ	F
G	VDDQ	DQL0	DQSL_t				VDD	VSS	VDDQ	G
H	VSSQ	DQL4	DQL2				DQL3	DQL5	VSSQ	H
J	VDD	VDDQ	DQL6				DQL7	VDDQ	VDD	J
K	VSS	CKE	ODT				CK_t	CK_c	VSS	K
L	VDD	WE_n/ A14	ACT_n				CS_n	RAS_n/ A16	VDD	L
M	VREFCA	BG0	A10/ AP				A12/ BC_n	CAS_n/ A15	VSS	M
N	VSS	BA0	A4				A3	BA1	TEN	N
P	RESET_ n	A6	A0				A1	A5	ALERT_n	P
R	VDD	A8	A2				A9	A7	VPP	R
T	VSS	A11	PAR				NC	A13	VDD	T
	1	2	3	4	5	6	7	8	9	

Biwin Confidential

6. Pin Description

Symbol	Type	Description
CK_t, CK_c	Input	**Clock:** CK_t and CK_c are differential clock inputs. All address and control input signals are sampled on the crossing of the positive edge of CK_t and negative edge of CK_c. In connectivity test mode, the clock needs to be in differential inputs and the mrs command cannot be sent.
CKE	Input	**Clock Enable:** CKE HIGH activates, and CKE Low deactivates, internal clock signals and device input buffers and output drivers. Taking CKE Low provides Precharge Power- Down and Self-Refresh operation (all banks idle), or Active Power-Down (row Active in any bank). CKE is synchronous for Self-Refresh exit. After VREFCA and Internal DQ Vref have become stable during the power on and initialization sequence, they must be maintained during all operations (including Self-Refresh). CKE must be maintained high throughout read and write accesses. Input buffers, excluding CK_t, CK_c, ODT and CKE are disabled during power_x0002_down. Input buffers, excluding CKE, are disabled during self-refresh.
CS_n	Input	**Chip Select:** All commands are masked when CS_n is registered HIGH. CS_n provides for external Rank selection on systems with multiple Ranks. CS_n is considered part of the command code
ODT	Input	**On Die Termination:** ODT (registered HIGH) enables RTT_NOM termination resistance internal to the DDR4 SDRAM. When enabled, ODT is only applied to each DQ, DQS_t, DQS_c and DM_n/DBI_n/TDQS_t, NU/TDQS_c (When TDQS is enabled via Mode Register A11=1 in MR1) signal for x8 configurations. For x16 configuration ODT is applied to each DQ, DQSU_t, DQSU_c, DQSL_t, DQSL_c, DMU_n, and DML_n signal. The ODT pin will be ignored if MR1 is programmed to disable RTT_NOM.RTT_NOM cannot be changed when ODT pin active;
ACT_n	Input	**Activation Command Input:** ACT_n defines the Activation command being entered along with CS_n. The input into RAS_n/A16, CAS_n/A15 and WE_n/A14 will be considered as Row Address A16, A15 and A14
RAS_n/A16 CAS_n/ A15 WE_n/A14	Input	**Command Inputs:** RAS_n/A16, CAS_n/A15 and WE_n/A14 (along with CS_n) define the command being entered. Those pins have multi function. For example, for activation with ACT_n Low, those are Addressing like A16,A15 and A14 but for non-activation command with ACT_n High, those are Command pins for Read, Write and other command defined in command truth table
DM_n/DBI_n/ TDQS_t, (DMU_n/ DBIU_n), (DML_n/ DBIL_n)	Input/Output	**Input Data Mask and Data Bus Inversion:** DM_n is an input mask signal for write data. Input data is masked when DM_n is sampled LOW coincident with that input data during a Write access. DM_n is sampled on both edges of DQS. DM is muxed with DBI function by Mode Register A10, A11, A12 setting in MR5. For x8 device, the function of DM or TDQS is enabled by Mode Register A11 setting in MR1. DBI_n is an input/output identifying whether to store/output the true or inverted data. If DBI_n is LOW, the data will be stored/output after inversion inside the DDR4 SDRAM and not inverted if DBI_n is HIGH. TDQS is only supported in X8
BG0 - BG1	Input	**Bank Group Inputs:** BG0 - BG1 define to which bank group an Active, Read, Write or Precharge command is being applied. BG0 also determines which mode register is to be accessed during a MRS cycle. X4/8 have BG0 and BG1 but X16 has only BG0

Biwin Confidential

6. Pin Description

Symbol	Type	Description
BA0 - BA1	Input	**Bank Address Inputs**: BA0 - BA1 define to which bank an Active, Read, Write or Precharge command is being applied. Bank address also determines which mode register is to be accessed during a MRS cycle.
A0 - A16	Input	**Address Inputs:** Provide the row address for ACTIVATE Commands and the column address for Read/Write commands to select one location out of the memory array in the respective bank. (A10/AP, A12/BC_n, RAS_n/A16, CAS_n/A15 and WE_n/A14 have additional functions, see other rows.The address inputs also provide the op-code during Mode Register Set commands.
A10 / AP	Input	Auto-precharge: A10 is sampled during Read/Write commands to determine whether Auto-precharge should be performed to the accessed bank after the Read/Write operation. (HIGH: Auto precharge; LOW: no Autop recharge).A10 is sampled during a Precharge command to determine whether the Precharge applies to one bank (A10 LOW) or all banks (A10 HIGH). If only one bank is to be precharged, the bank is selected by bank addresses
A12 / BC_n	Input	**Burst Chop:** A12 / BC_n is sampled during Read and Write commands to determine if burst chop (on-the-fly) will be performed. (HIGH, no burst chop; LOW: burst chopped). See command truth table for details
RESET_n	Input	**Active Low Asynchronous Reset**: Reset is active when RESET_n is LOW, and inactive when RESET_n is HIGH. RESET_n must be HIGH during normal operation. RESET_n is a CMOS rail to rail signal with DC high and low at 80% and 20% of VDD
DQ	Input/Output	**Data Input/ Output**: Bi-directional data bus. If CRC is enabled via Mode register then CRC code is added at the end of Data Burst. Any DQ from DQ0~DQ3 may indicate the internal Vref level during test via Mode Register Setting MR4 A4=High. During the mode, RTT value should be set to Hi-Z. Refer to vendor specific datasheets to determine which DQ is used.
DQS_t, DQS_c, DQSU_t, DQSU_c, DQSL_t, DQSL_c	Input/Output	**Data Strobe**: output with read data, input with write data. Edge-aligned with read data, centered in write data. For the x16, DQSL corresponds to the data on DQL0-DQL7; DQSU corresponds to the data on DQU0-DQU7. The data strobe DQS_t, DQSL_t and DQSU_t are paired with differential signals DQS_c, DQSL_c, and DQSU_c, respectively, to provide differential pair signaling to the system during reads and writes. DDR4 SDRAM supports differential data strobe only and does not support single-ended
TDQS_t, TDQS_c	Input	**Termination Data Strobe:** TDQS_t/TDQS_c is applicable for x8 DRAMs only. When enabled via Mode Register A11 = 1 in MR1, the DRAM will enable the same termination resistance function on TDQS_t/TDQS_c that is applied to DQS_t/DQS_c. When disabled via mode register A11 = 0 in MR1, DM/DBI/TDQS will provide the data mask function or Data Bus Inversion depending on MR5; A11,12,10 and TDQS_c is not used. x4/x16 DRAMs must disable the TDQS function via mode register A11 = 0 in MR1.

Biwin Confidential

7. Pin Description

Symbol	Type	Description
PAR	Input	**Command and Address Parity Input:** DDR4 Supports Even Parity check in DRAM with MR setting. Once it's enabled via Register in MR5, then DRAM calculates Parity with ACT_n, RAS_n/A16, CAS_n/A15, WE_n/A14, BG0-BG1, BA0-BA1, A17-A0. Command and address inputs shall have parity check performed when commands are latched via the rising edge of CK_t and when CS_n LOW
ALERT_n	Input / Output	**Alert:** It has multi functions such as CRC error flag, Command and Address Parity error flag as Output signal. If there is error in CRC, then Alert_n goes LOW for the period time interval and goes back HIGH. If there is error in Command Address Parity Check, then Alert_n goes LOW for relatively long period until on going DRAM internal recovery transaction to complete. During Connectivity Test mode, this pin works as input. Using this signal or not is dependent on system. In case of not connected as Signal,ALERT_n Pin must be bounded to VDD on board.
TEN	Input	**Connectivity Test Mode Enable:** Required on X16 devices and not support on x4/x8 densities. HIGH in this pin will enable Connectivity Test Mode operation along with other pins. It is a CMOS rail to rail signal with AC high and low at 80% and 20% of VDD. Using this signal or not is dependent on System. This pin may be DRAM internally pulled low through a weak pull-down resistor to VSS
NC	–	**No connect:** No internal electrical connection is present.
VDDQ	Supply	**DQ Power Supply:** 1.2 V +/- 0.06V
VSSQ	Supply	**DQ Ground**
VDD	Supply	**Power Supply:** 1.2 V +/- 0.06 V
VSS	Supply	**Ground**
VPP	Supply	**DRAM Activating Power Supply:** 2.5V (2.375V min , 2.75V max)
VREFCA	Supply	**Reference voltage for CA**
ZQ	Supply	**Reference Pin for ZQ calibration**

BiwinConfidential

8. Basic Functionality

The DDR4 SDRAM is a high-speed dynamic random-access memory internally configured as sixteen-banks, 4 bank group with 4 banks for each bank group for x8 and eight-banks, 2 bank group with 4 banks for each bankgroup for x16 DRAM.

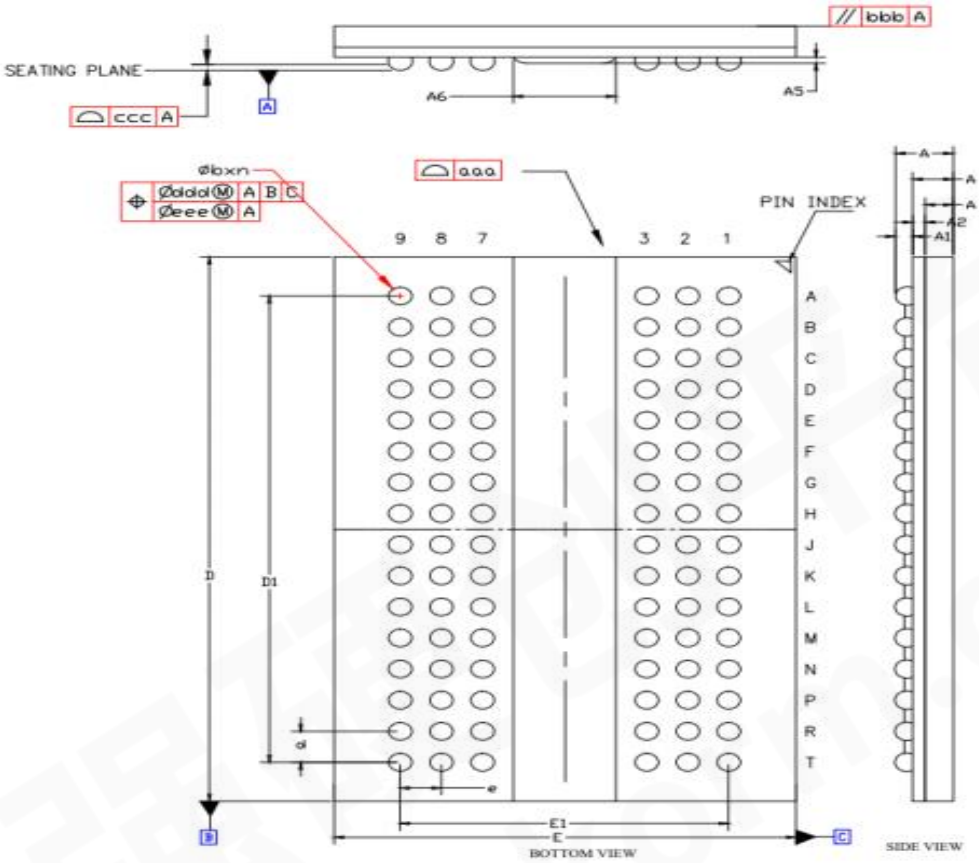
The DDR4 SDRAM uses an 8n prefetch architecture to achieve high-speed operation. The 8n prefetch architecture is combined with an interface designed to transfer two data words per clock cycle at the I/O pins. A single read or write operation for the DDR4 SDRAM consists of a single 8n-bit wide, four clock data transfer at the internal DRAM core and eight corresponding n-bit wide, one-half clock cycle data transfers at the I/O pins.

Read and write operation to the DDR4 SDRAM are burst oriented, start at a selected location, and continue for a burst length of eight or a ‘chopped’ burst of four in a programmed sequence. Operation begins with the registration of an ACTIVATE Command, which is then followed by a Read or Write command.

The address bits registered coincident with the ACTIVATE Command are used to select the bank and row to be activated (BG0- BG1 in x4/8 and BG0 in x16 select the bankgroup; BA0-BA1select the bank; A0-A17 select the row; refer to “DDR4 SDRAM Addressing” for specific requirements). The address bits registered coincident with the Read or Write command are used to select the starting column location for the burst operation, determine if the auto precharge command is to be issued (via A10), and select BC4 or BL8 mode ‘on the fly’ (via A12) if enabled in the mode register.

Prior to normal operation, the DDR4 SDRAM must be powered up and initialized in predefined manner.
The following sections provide detailed information covering device reset and initialization, register definition, command descriptions, and device operation

9. Dimensions(9*14)



	Symbol	Dimension in mm			Dimension in inch		
		Min	Normal	Max	Min	Normal	Max
TOTAL THICNESS	A	---	1.12	1.20	---	0.0441	0.0472
STAND OFF	A1	0.30	0.34	0.38	0.0118	0.0134	0.0150
SUBSTRATE THICKNESS	A2	0.20	0.23	0.26	0.0079	0.0091	0.0102
MOLD THICKNESS	A3	0.51	0.55	0.59	0.0201	0.0217	0.0232
SBT+MOLD THICKNESS	A4	0.73	0.78	0.83	0.0287	0.0307	0.0327
SLOT THICKNESS	A5	0.142	0.155	0.168	0.0056	0.0061	0.0066
SLOT WIDTH	A6	1.90	2.00	2.10	0.0748	0.0787	0.0827
BALL WIDTH	Φb	0.42	0.47	0.52	0.0165	0.0185	0.0205
BALL PITCH	d		0.8			0.0315	
	e		0.8			0.0315	
BALL COUNT	n			96			
BODY SIZE	D	13.90	14.00	14.10	0.5472	0.5512	0.5551
	E	8.90	9.00	9.10	0.3504	0.3543	0.3583
EDGE BALL CENTER TO CENTER	D1	11.90	12.00	12.10	0.4685	0.4724	0.4764
	E1	6.30	6.40	6.50	0.2480	0.2520	0.2559
PKG EDGE TOLERANCE	aaa		0.10			0.0039	
MOLD FLATNESS	bbb		0.10			0.0039	
COPLANRITY	ccc		0.10			0.0039	
BALL OFFSET(PACKAGE)	ddd		0.15			0.0059	
BALL OFFSET(BALL)	eee		0.05			0.0020	
JEDEC				MO-276(REF)			

Notes: All dimensions are in millimeters.

10. Speed Bins

DDR4-2133 Speed Bins and Operations

DDR4-2133 Speed Bin						Unit
CL-nRCD-nRP				15-15-15		
Parameter			Symbol	Min	Max	
Internal READ command to first data			tAA	14.06[14] (13.50)[5, 12]	18.00	ns
Internal READ command to first data with read DBI enabled			tAA DBI	tAA(MIN) + 3*n*CK	tAA(MAX) + 3*n*CK	ns
ACTIVATE to internal READ or WRITE delay time			tRCD	14.06 (13.50)[5, 12]	–	ns
PRECHARGE command period			tRP	14.06 (13.50)[5, 12]	–	ns
ACTIVATE-to-PRECHARGE command period			tRAS	33	9 x tREFI	ns
ACTIVATE-to-ACTIVATE or REFRESH command period			tRC	tRAS + tRP	–	ns
	Normal	Read DBI				
CWL=9	CL=9	CL=11	tCK(AVG)	1.5	1.6	ns
	CL=10	CL=12	tCK(AVG)	Reserved		ns
CWL=9, 11	CL=11	CL=13	tCK(AVG)	1.25	<1.5	ns
				1.25	<1.5	ns
	CL=12	CL=14	tCK(AVG)	1.25	<1.5	ns
CWL=10, 12	CL=13	CL=15	tCK(AVG)	1.071	<1.25	ns
	CL=14	CL=16	tCK(AVG)	1.071	<1.25	ns
CWL=11, 14	CL=14	CL=17	tCK(AVG)	Reserved		ns
	CL=15	CL=18	tCK(AVG)	0.937	<1.071	ns
	CL=16	CL=19	tCK(AVG)	0.937	<1.071	ns
CWL =12,16	CL=15	CL=18	tCK(AVG)	Reserved		ns
	CL=16	CL=19	tCK(AVG)	Reserved		ns
	CL=17	CL=20	tCK(AVG)	0.833	<0.937	ns
	CL=18	CL=21	tCK(AVG)	0.833	<0.937	ns
Supported CL Settings				10, (11), 12,(13),14,(15),16,(17),18		nCK
Supported CL Settings with DBI				12, (13), 14,(15),17,(18),19,(20),21		nCK
Supported CLW Settings				9, 10, 11, 12 , 14, 16		nCK

Biwin Confidential
www.biwin.com.cn

10. Speed Bins

DDR4-2400 Speed Bins and Operations

DDR4-2400 Speed Bin						Unit
CL-nRCD-nRP				17-17-17		
Parameter			Symbol	Min	Max	
Internal READ command to first data			tAA	14.16 (13.75)[5, 12]	18.00	ns
Internal READ command to first data with read DBI enabled			tAA DBI	tAA(MIN) + 3*n*CK	tAA(MAX) + 3*n*CK	ns
ACTIVATE to internal READ or WRITE delay time			tRCD	14.16 (13.75)[5, 12]	–	ns
PRECHARGE command period			tRP	14.16 (13.75)[5, 12]	–	ns
ACTIVATE-to-PRECHARGE command period			tRAS	32	9 x tREFI	ns
ACTIVATE-to-ACTIVATE or REFRESH command period			tRC	46.16 (45.75)[5,12]	–	ns
	Normal	Read DBI				
CWL=9	CL=9	CL=11 (Optional)[5]	tCK(AVG)	Reserved		ns
	CL=10	CL=12	tCK(AVG)	1.5	1.6	ns
CWL=9, 11	CL=10	CL=12	tCK(AVG)	Reserved		ns
	CL=11	CL=13	tCK(AVG)	1.25	<1.5	ns
	CL=12	CL=14	tCK(AVG)	1.25	<1.5	ns
CWL=10, 12	CL=12	CL=14	tCK(AVG)	Reserved		ns
	CL=13	CL=15	tCK(AVG)	1.071	<1.25	ns
	CL=14	CL=16	tCK(AVG)	1.071	<1.25	ns
CWL=11, 14	CL=14	CL=17	tCK(AVG)	Reserved		ns
	CL=15	CL=18	tCK(AVG)	0.937	<1.071	ns
	CL=16	CL=19	tCK(AVG)	0.937	<1.071	ns
CWL=12, 16	CL=15	CL=18	tCK(AVG)	Reserved		ns
	CL=16	CL=19	tCK(AVG)	Reserved		ns
	CL=17	CL=20	tCK(AVG)	0.833	<0.937	ns
	CL=18	CL=21	tCK(AVG)	0.833	<0.937	ns
Supported CL Settings				10, (11), 12,(13),14,(15),16,(17),18		nCK
Supported CL Settings with DBI				12, (13), 14,(15),17,(18),19,(20),21		nCK
Supported CLW Settings				9, 10, 11, 12, 14, 16		nCK

Biwin Confidential

10. Speed Bins

DDR4-2666 Speed Bins and Operations

DDR4-2666 Speed Bin						Unit
CL-nRCD-nRP				19-19-19		
Parameter			Symbol	Min	Max	
Internal READ command to first data			tAA	14.25 (13.75)[5, 12]	18.00	ns
Internal READ command to first data with read DBI enabled			tAA DBI	tAA(MIN) + 3*n*CK	tAA(MAX) + 3*n*CK	ns
ACTIVATE to internal READ or WRITE delay time			tRCD	14.25 (13.75)[5, 12]	–	ns
PRECHARGE command period			tRP	14.25 (13.75)[5, 12]	–	ns
ACTIVATE-to-PRECHARGE command period			tRAS	32	9 x tREFI	ns
ACTIVATE-to-ACTIVATE or REFRESH command period			tRC	46.25 (45.75)[5,12]	–	ns
	Normal	Read DBI				
CWL=9	CL=9	CL=11	tCK(AVG)	Reserved		ns
	CL=10	CL=12	tCK(AVG)	1.5	1.6	ns
CWL=9, 11	CL=10	CL=12	tCK(AVG)	Reserved		ns
	CL=11	CL=13	tCK(AVG)	1.25	<1.5	ns
	CL=12	CL=14	tCK(AVG)	1.25	<1.5	ns
CWL=10, 12	CL=12	CL=14	tCK(AVG)	Reserved		ns
	CL=13	CL=15	tCK(AVG)	1.071	<1.25	ns
	CL=14	CL=16	tCK(AVG)	1.071	<1.25	ns
CWL=11, 14	CL=14	CL=17	tCK(AVG)	Reserved		ns
	CL=15	CL=18	tCK(AVG)	0.937	<1.071	ns
	CL=16	CL=19	tCK(AVG)	0.937	<1.071	ns
CWL=12, 16	CL=15	CL=18	tCK(AVG)	Reserved		ns
	CL=16	CL=19	tCK(AVG)	Reserved		ns
	CL=17	CL=20	tCK(AVG)	0.833	<0.937	ns
	CL=18	CL=21	tCK(AVG)	0.833	<0.937	ns
CWL=14, 18	CL=17	CL=20	tCK(AVG)	Reserved		ns
	CL=18	CL=21	tCK(AVG)	Reserved		ns
	CL=19	CL=22	tCK(AVG)	0.75	<0.833	ns
	CL=20	CL=23	tCK(AVG)	0.75	<0.833	ns
Supported CL Settings				10, (11), 12,(13),14,(15),16,(17),18,19,20		nCK
Supported CL Settings with DBI				12, (13), 14,(15),17,(18),19,(20),21,22,23		nCK
Supported CLW Settings				9,10,11,12,14,16,18		nCK

BiwinConfidential

10. Speed Bins

DDR4-2933 Speed Bins and Operations

DDR4-2933 Speed Bin						Unit
CL-nRCD-nRP				21-21-21		
Parameter			Symbol	Min	Max	
Internal READ command to first data			tAA	14.32[14] (13.75)[5, 12]	18.00	ns
Internal READ command to first data with read DBI enabled			tAA DBI	tAA(MIN) + 4*n*CK	tAA(MAX) + 4*n*CK	ns
ACTIVATE to internal READ or WRITE delay time			tRCD	14.32 (13.75)[5, 12]	–	ns
PRECHARGE command period			tRP	14.32 (13.75)[5, 12]	–	ns
ACTIVATE-to-PRECHARGE command period			tRAS	32	9 x tREFI	ns
ACTIVATE-to-ACTIVATE or REFRESH command period			tRC	46.32 (45.75)[5,12]	–	ns
	Normal	Read DBI				
CWL=9	CL=9	CL=11	tCK(AVG)	Reserved		ns
	CL=10	CL=12	tCK(AVG)	1.5	1.6	ns
CWL=9, 11	CL=10	CL=12	tCK(AVG)	Reserved		ns
	CL=11	CL=13	tCK(AVG)	1.25	<1.5	ns
	CL=12	CL=14	tCK(AVG)	1.25	<1.5	ns
CWL=10, 12	CL=12	CL=14	tCK(AVG)	Reserved		ns
	CL=13	CL=15	tCK(AVG)	1.071	<1.25	ns
	CL=14	CL=16	tCK(AVG)	1.071	<1.25	ns
CWL=11, 14	CL=14	CL=17	tCK(AVG)	Reserved		ns
	CL=15	CL=18	tCK(AVG)	0.937	<1.071	ns
	CL=16	CL=19	tCK(AVG)	0.937	<1.071	ns
CWL=12, 16	CL=15	CL=18	tCK(AVG)	Reserved		ns
	CL=16	CL=19	tCK(AVG)	Reserved		ns
	CL=17	CL=20	tCK(AVG)	0.833	<0.937	ns
	CL=18	CL=21	tCK(AVG)	0.833	<0.937	ns
CWL=14, 18	CL=17	CL=20	tCK(AVG)	Reserved		ns
	CL=18	CL=21	tCK(AVG)	Reserved		ns
	CL=19	CL=22	tCK(AVG)	0.75	<0.833	ns
	CL=20	CL=23	tCK(AVG)	0.75	<0.833	ns

DDR4-2933 Speed Bin						Unit
CL-nRCD-nRP				21-21-21		
Parameter			Symbol	Min	Max	
CWL=16, 20	CL=19	CL=23	tCK(AVG)	Reserved		ns
	CL=20	CL=24	tCK(AVG)	Reserved		ns
	CL=21	CL=25	tCK(AVG)	0.682	<0.75	ns
	CL=22	CL=26	tCK(AVG)	0.682	<0.75	ns
Supported CL Settings				10, (11), 12, (13), 14, (15), 16, (17), 18, (19), 20, 21, 22		nCK
Supported CL Settings with DBI				12, (13), 14, (15), 16, (18), 19, (20), 21, (22), 23, 25, 26		nCK
Supported CLW Settings				9, 10, 11, 12, 14, 15, 16, 18, 20		nCK

BiwinConfidential

10. Speed Bins

DDR4-3200 Speed Bins and Operations

DDR4-3200 Speed Bin						Unit
CL-nRCD-nRP				22-22-22		
Parameter			Symbol	Min	Max	
Internal READ command to first data			tAA	13.75	18.00	ns
Internal READ command to first data with read DBI enabled			tAA DBI	tAA(MIN) + 4*n*CK	tAA(MAX) + 4*n*CK	ns
ACTIVATE to internal READ or WRITE delay time			tRCD	13.75	-	ns
PRECHARGE command period			tRP	13.75	-	ns
ACTIVATE-to-PRECHARGE command period			tRAS	32	9 x tREFI	ns
ACTIVATE-to-ACTIVATE or REFRESH command period			tRC	45.75	-	ns
	Normal	Read DBI				
CWL=9	CL=9	CL=11	tCK(AVG)	Reserved		ns
	CL=10	CL=12	tCK(AVG)	Reserved		ns
CWL=9, 11	CL=10	CL=12	tCK(AVG)	Reserved		ns
	CL=11	CL=13	tCK(AVG)	1.25	<1.5	ns
				(Optional)[5, 12]		ns
	CL=12	CL=14	tCK(AVG)	1.25	<1.5	ns
CWL=10, 12	CL=12	CL=14	tCK(AVG)	Reserved		ns
	CL=13	CL=15	tCK(AVG)	1.071	<1.25	ns
				(Optional)[5, 13]		ns
	CL=14	CL=16	tCK(AVG)	1.071	<1.25	ns
CWL=11, 14	CL=14	CL=17	tCK(AVG)	Reserved		ns
	CL=15	CL=18	tCK(AVG)	0.937	<1.071	ns
	CL=16	CL=19	tCK(AVG)	0.937	<1.071	ns
CWL=12, 16	CL=15	CL=18	tCK(AVG)	Reserved		ns
	CL=16	CL=19	tCK(AVG)	Reserved		ns
	CL=17	CL=20	tCK(AVG)	0.833	<0.937	ns
	CL=18	CL=21	tCK(AVG)	0.833	<0.937	ns
CWL=14, 18	CL=17	CL=20	tCK(AVG)	Reserved		ns
	CL=18	CL=21	tCK(AVG)	Reserved		ns
	CL=19	CL=22	tCK(AVG)	0.75	<0.833	ns
	CL=20	CL=23	tCK(AVG)	0.75	<0.833	ns
CWL=16, 20	CL=20	CL=24	tCK(AVG)	Reserved		ns
	CL=22	CL=26	tCK(AVG)	0.625	<0.75	ns
	CL=24	CL=28	tCK(AVG)	0.625	<0.75	ns

Supported CL Settings	10, 11, 12, 13, 14, 15, 16, 17, 18, 19, 20, 21, 22, 24	nCK
Supported CL Settings with DBI	12, 13, 14, 15, 16, 18, 19, 20, 21, 22, 23,24,25, 26,28	nCK
Supported CLW Settings	9, 10, 11, 12, 14, 15, 16, 18, 20	nCK

Biwin Confidential

Note：

Absolute Specification
- VDDQ = VDD = 1.20V +/- 0.06 V
- VPP = 2.5V +0.25/-0.125 V
- The values defined with above-mentioned table are DLL ON case

1. The CL setting and CWL setting result in tCK(avg).MIN and tCK(avg).MAX requirements. When making a
selection of tCK(avg), both need to be fulfilled: Requirements from CL setting as well as requirements from CWL
setting.
2. tCK(avg).MIN limits: Since CAS Latency is not purely analog - data and strobe output are synchronized by
the DLL - all possible intermediate frequencies may not be guaranteed. CL in clock cycle is calculated from tAA
following rounding algorithm defined in Section 15.5.
3. tCK(avg).MAX limits: Calculate tCK(avg) = tAA.MAX / CL SELECTED and round the resulting tCK(avg) down to the next valid speed bin (i.e. 1.5ns or 1.25ns or 1.071 ns or 0.937 ns or 0.833 ns). This result is tCK(avg).MAX corresponding to CL SELECTED.
4. “Reserved’ settings are not allowed. User must program a different value.
5. “Optional' settings allow certain devices in the industry to support this setting, however, it is not a mandatory
feature. Refer to supplier's data sheet and/or the DIMM SPD information if and how this setting is supported.
6. Any DDR4-2400 speed bin also supports functional operation at lower frequencies as shown in the table
which are not subject to Production Tests but verified by Design/Characterization.
7. Any DDR4-2666 speed bin also supports functional operation at lower frequencies as shown in the table
which are not subject to Production Tests but verified by Design/Characterization.
8. Any DDR4-2933 speed bin also supports functional operation at lower frequencies as shown in the table
which are not subject to Production Tests but verified by Design/Characterization.
9. Any DDR4-3200 speed bin also supports functional operation at lower frequencies as shown in the table
which are not subject to Production Tests but verified by Design/Characterization.
10. DDR4-1600 AC timing apply if DRAM operates at lower than 1600 MT/s data rate.
11. Parameters apply from tCK(avg)min to tCK(avg)max at all standard JEDEC clock period values as stated
in the Speed Bin Tables.
12. CL number in parentheses, it means that these numbers are optional.
13. DDR4 SDRAM supports CL=9 as long as a system meets tAA(min).
14. Each speed bin lists the timing requirements that need to be supported in order for a given DRAM to be JEDEC compliant. JEDEC compliance does not require support for all speed bins within a given speed. JEDEC compliance requires meeting the parameters for a least one of the listed speed bins.

Biwin Confidential

11. DRAM Component Operating Temperature Range

Symbol	Parameter	Rating	Units
TOPER	Normal Operating Temperature Range	-40 to 85	℃

Note:

1. Operating Temperature TOPER is the case surface temperature on the center/top side of the DRAM. For measurement conditions, please refer to the JEDEC document JESD51-2.
2. The Normal Temperature Range specifies the temperatures where all DRAM specifications will be supported. During operation, the DRAM case temperature must be maintained between 0-85℃ under all operating conditions.

12. Package Electrical Specifications（×16）

Symbol	Parameter	DDR4 1600-DDR4 3200		Unit	Note
		Min	Max		
Z_{IO}	Input/output Zpkg	45	85	Ω	1
T_{dIO}	Input/output Pkg Delay	14	45	ps	1
L_{IO}	Input/Output Lpkg	-	3.4	nH	1,2
C_{IO}	Input/Output Cpkg	-	0.82	pF	1,3
$Z_{IO\ DQS}$	DQS_t, DQS_c Zpkg	45	85	Ω	1
$T_{dIO\ DQS}$	DQS_t, DQS_c Pkg Delay	14	45	ps	1
$L_{IO\ DQS}$	DQS Lpkg	-	3.4	nH	1,2
$C_{IO\ DQS}$	DQS Cpkg	-	0.82	pF	1,3
$DZ_{DIO\ DQS}$	Delta Delay DQSU_t, DQSU_c	-	10	Ω	-
	Delta Delay DQSL_t, DQSL_c	-	10	Ω	-
$D_{TdDIO\ DQS}$	Delta Delay DQSU_t, DQSU_c	-	5	ps	-
	Delta Delay DQSL_t, DQSL_c	-	5	ps	-
$Z_{I\ CTRL}$	Input CTRL pins Zpkg	50	90	Ω	1
$T_{dI\ CTRL}$	Input CTRL pins Pkg Delay	14	42	ps	1
$L_{i\ CTRL}$	Input CTRL Lpkg	-	3.4	nH	1,2
$C_{i\ CTRL}$	Input CTRL Cpkg	-	0.7	pF	1,3
$Z_{IADD\ CMD}$	Input- CMD ADD pins Zpkg	50	90	Ω	1
Td_{IADD_CMD}	Input- CMD ADD pins Pkg Delay	14	52	ps	1
$L_{iADD\ CMD}$	Input CMD ADD Lpkg	-	3.9	nH	1,2

Biwin Confidential

Symbol	Parameter	DDR4 1600-DDR4 3200		Unit	Note
		Min	Max		
$C_{iADD\ CMD}$	Input CMD ADD Cpkg	-	0.86	pF	1,3
Z_{CK}	CLK_c Zpkg	50	90	Ω	1
Td_{CK}	CLK_c Pkg Delay	14	42	ps	1
$L_{i\ CLK}$	Input CLK Lpkg	-	3.4	nH	1,2
$C_{i\ CLK}$	Input CLK Cpkg	-	0.7	pF	1,3
DZ_{DCK}	Delta Zpkg CLK_c	-	10	Ω	-
DT_{dCK}	Delta Delay CLK_c	-	5	ps	-
Z_{OZQ}	ZQ Zpkg	-	100	Ω	-
Td_{OZQ}	ZQ Delay	20	90	ps	-
$Z_{O\ ALERT}$	ALERT Zpkg	40	100	Ω	-
$Td_{O\ ALERT}$	ALERT Delay	20	55	ps	-

Note:
1. Package implementations shall meet spec if the Zpkg and Pkg Delay fall within the ranges shown, and the maximum Lpkg and Cpkg do not exceed the maximum value shown.
2. It is assumed that Lpkg can be approximated as Lpkg = Zo*Td
3. It is assumed that Cpkg can be approximated as Cpkg = Td/Zo

13. Revision History

Date	Revision	Description
Sep -2024	V1.0	Initial release