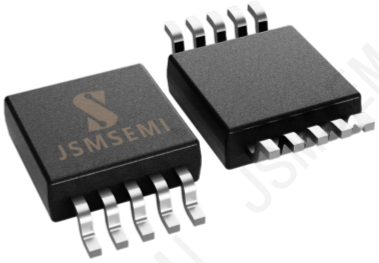
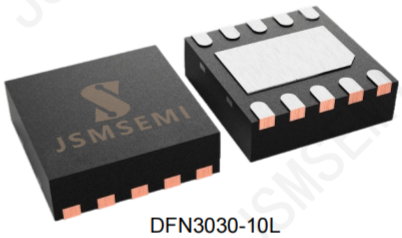
Description

The LM5106 is a high-voltage gate driver designed to drive both the high-side and low-side N-channel MOSFETs in a synchronous buck or half-bridge configuration. The floating high-side driver can work with rail voltages up to 100 V. The single control input is compatible with TTL signal levels and a single external resistor programs the switching transition dead-time through tightly matched turnon delay circuits. The robust level shift technology operates at high speed while consuming low power and provides clean output transitions. Undervoltage lockout (UVLO) disables the gate driver when either the low side or the bootstrapped high-side supply voltage is below the operating threshold. The LM5106 is offered in the 10-pin MSOP or the thermally enhanced 10-pin PDFN plastic package.



MSOP-10



DFN3030-10L

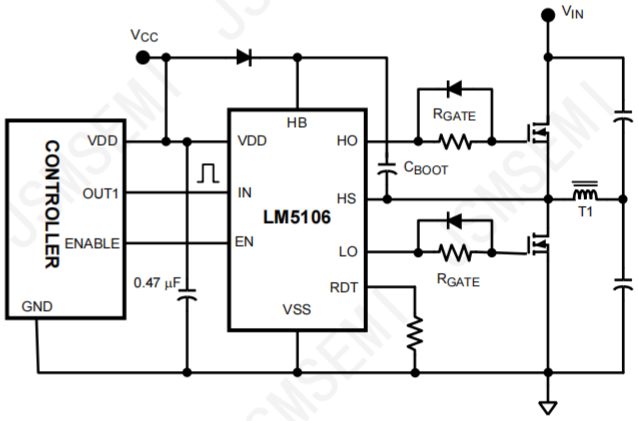
Features

- Drives Both a High-Side and Low-Side N-Channel MOSFET
- 4.5A Peak Output Sink Current
- 4.5A Peak Output Source Current
- Bootstrap Supply Voltage Range up to 120V DC
- Single TTL Compatible Input
- Programmable Turnon Delays (Dead-Time)
- Enable Input Pin
- Fast Turnoff Propagation Delays (130ns Typical)
  16ns Rise and 10ns Fall Time
- Supply Rail Undervoltage Lockout
- Low Power Consumption
- PDFN4040-10L Package and MSOP-10 Package

Applications

- Solid-State Motor Drives
- Half-Bridge and Full-Bridge Power Converters
- Two Switch Forward Power Converters

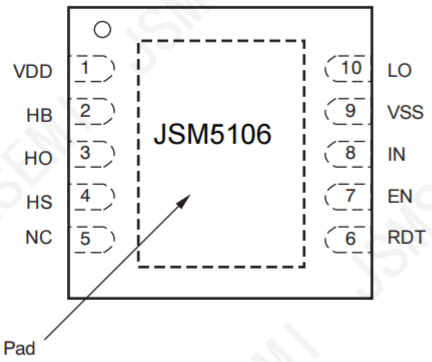
Simplified Schematic



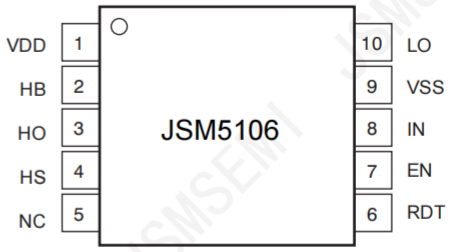
Ordering Information

Order number	Package	Marking	Operation Temperature Range	MSL Grade	Ship,Quantity	Green
LM5106MMX/NOPB-JSM	MSOP-10	JSM5106	-40 to 125°C	3	TR&5000	Rohs
LM5106SDX/NOPB-JSM	DFN4040-10L	JSM5106	-40 to 125°C	3	TR&5000	Rohs

Pin Configuration and Functions



Top View: DFN4040-10L



Top View: MSOP-10

Pin Functions

PIN		DESCRIPTION	APPLICATION INFORMATION
NO.	NAME		
1	VDD	Positive gate drive supply	Decouple VDD to VSS using a low ESR/ESL capacitor, placed as close to the IC as possible.
2	HB	High-side gate driver bootstrap rail	Connect the positive terminal of bootstrap capacitor to the HB pin and connect negative terminal to HS. The Bootstrap capacitor should be placed as close to IC as possible.
3	HO	High-side gate driver output	Connect to the gate of high-side N-MOS device through a short, low inductance path.
4	HS	High-side MOSFET source connection	Connect to the negative terminal of the booststrap capacitor and to the source of the high-side N-MOS device.
5	NC	Not connected	
6	RDT	Dead-time programming pin	A resistor from RDT to VSS programs the turnon delay of both the high- and low-side MOSFETs. The resistor should be placed close to the IC to minimize noise coupling from adjacent PC board traces.
7	EN	Logic input for driver Disable/Enable	TTL compatible threshold with hysteresis. LO and HO are held in the low state when EN is low.
8	IN	Logic input for gate driver	TTL compatible threshold with hysteresis. The high-side MOSFET is turned on and the low-side MOSFET turned off when IN is high.
9	VSS	Ground return	All signals are referenced to this ground.
10	LO	Low-side gate driver output	Connect to the gate of the low-side N-MOS device with a short, low inductance path.
—	EP	Exposed Pad	The exposed pad has no electrical contact. Connect to system ground plane for reduced thermal resistance.

Specifications

Absolute Maximum Ratings

	MIN	MAX	UNIT
V_{DD} to V_{SS}	–0.3	20	V
HB to HS	–0.3	20	V
IN and EN to V_{SS}	–0.3	V_{DD} + 0.3	V
LO to V_{SS}	–0.3	V_{DD} + 0.3	V
HO to V_{SS}	HS – 0.3	HB + 0.3	V
HS to V_{SS}		100	V
HB to V_{SS}		120	V
RDT to V_{SS}	–0.3	5	V
Junction Temperature		150	°C
Storage temperature range, T_{stg}	–55	150	°C

ESD Ratings

		VALUE	UNIT
V_{ESD}	Human-Body Model (HBM)	2000	V
	Charged-Device Model (CDM)	1000	V

Recommended Operating Conditions

	MIN	MAX	UNIT
V_{DD}	8	15	V
HS	–5	100	V
HB	HS + 8	HS + 15	V
HS Slew Rate		< 50	V/ns
Junction Temperature	–40	125	°C

Thermal Information

THERMAL METRIC		LM5106		UNIT
		DFN	MSOP	
		10 PINS	10 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	165	32.9	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	58.9	38.1	
$R_{\theta JB}$	Junction-to-board thermal resistance	54.4	14.9	
ψ_{JT}	Junction-to-top characterization parameter	6.2	0.4	
ψ_{JB}	Junction-to-board characterization parameter	83.6	15.2	
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	4.4	

Electrical Characteristics

MIN and MAX limits apply over the full operating junction temperature range. Unless otherwise specified, T_J = +25°C, V_{DD} = HB = 15V, V_{SS} = HS = 0 V, EN = 5 V. No load on LO or HO. RDT= 100kΩ.

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY CURRENTS						
I_{DD}	V_{DD} Quiescent Current	IN = EN = 0 V		0.24	0.4	mA
I_{DDO}	V_{DD} Operating Current	f = 500 kHz		2.1	3.5	mA
I_{HB}	Total HB Quiescent Current	IN = EN = 0 V		0.04	0.09	mA
I_{HBO}	Total HB Operating Current	f = 500 kHz		1.5	3	mA
I_{HBS}	HB to V_{SS} Current, Quiescent	HS = HB = 100 V		0.1	10	μA
I_{HBSO}	HB to V_{SS} Current, Operating	f = 500 kHz		0.5		mA
INPUT IN and EN						
V_{IL}	Low Level Input Voltage Threshold		0.8	1.8		V
V_{IH}	High Level Input Voltage Threshold			2.2	2.7	V
R_{pd}	Input Pulldown Resistance Pin IN and EN		100	200	500	kΩ
DEAD-TIME CONTROLS						
VRDT	Nominal Voltage at RDT		1.2	1.5	1.8	V
IRDT	RDT Pin Current Limit	RDT = 0 V	0.45	0.9	1.6	mA
UNDERVOLTAGE PROTECTION						
V_{DDR}	V_{DD} Rising Threshold			4.5		V
V_{DDH}	V_{DD} Threshold Hysteresis			0.5		V
V_{HBR}	HB Rising Threshold			4.2		V
V_{HBH}	HB Threshold Hysteresis			0.3		V
LO GATE DRIVER						
V_{OLL}	Low-Level Output Voltage	I_{LO} = 10 mA			0.1	V
V_{OHL}	High-Level Output Voltage	I_{LO} = –10 mA, V_{OHL} = V_{DD} – V_{LO}			0.1	V
I_{OHL}	Peak Pullup Current	LO = 0 V		4.5		A
I_{OLL}	Peak Pulldown Current	LO = 15V		4.5		A
HO GATE DRIVER						
V_{OLH}	Low-Level Output Voltage	I_{HO} = 100 mA			0.1	V
V_{OHH}	High-Level Output Voltage	I_{HO} = –100 mA, V_{OHH} = HB – HO			0.1	V
I_{OHH}	Peak Pullup Current	HO = 0 V		4.5		A
I_{OLH}	Peak Pulldown Current	HO = 12 V		4.5		A

Switching Characteristics

MIN and MAX limits apply over the full operating junction temperature range. Unless otherwise specified, T_J = +25°C, V_{DD} = HB = 15 V, V_{SS} = HS = 0 V, No Load on LO or HO.

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{LPHL}	Lower Turn-Off Propagation Delay			132	180	ns
t_{HPHL}	Upper Turn-Off Propagation Delay			160	210	
t_{LPLH}	Lower Turn-On Propagation Delay	RDT = 100k	560	680	800	
t_{HPLH}	Upper Turn-On Propagation Delay	RDT = 100k	800	1000	1200	
t_{LPLH}	Lower Turn-On Propagation Delay	RDT = 10k	190	290	390	
t_{HPLH}	Upper Turn-On Propagation Delay	RDT = 10k	150	250	350	
t_{en}, t_{sd}	Enable and Shutdown propagation delay			150		
DT1, DT2	Dead-time LO OFF to HO ON & HO OFF to LO ON	RDT = 100k		850,500		
		RDT = 10k		120,130		
MDT	Dead-time matching	RDT = 100k			500	
t_R	Either Output Rise Time			16		
t_F	Either Output Fall Time			10		

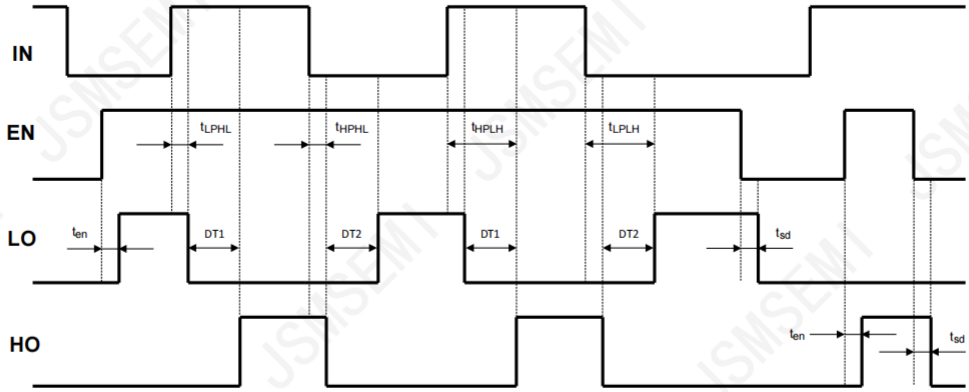


Figure 1. LM5106 Input - Output Waveforms

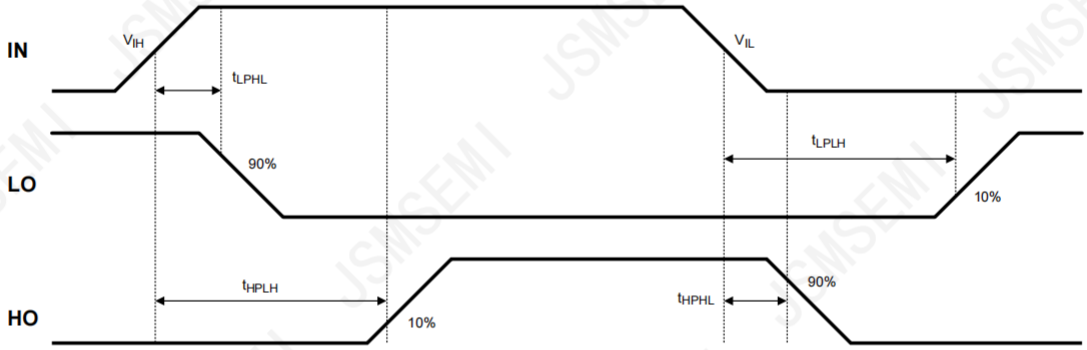


Figure 2. LM5106 Switching Time Definitions: t_{LPLH}, t_{LPHL}, t_{HPLH}, t_{HPHL}

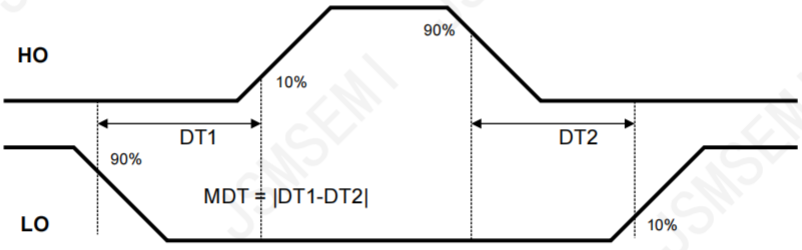


Figure 3. LM5106 Dead-time: DT

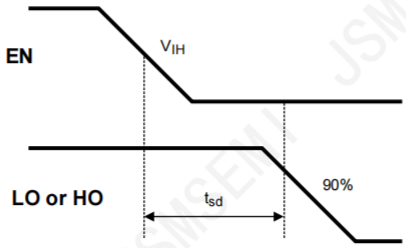


Figure 4. LM5106 Enable: t_{sd}

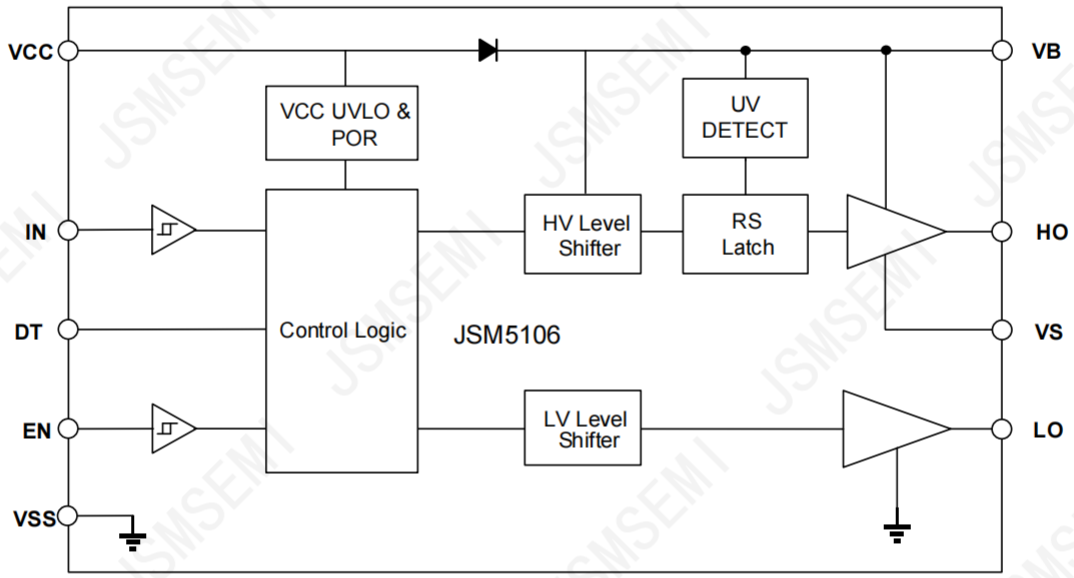
Detailed Description

Overview

The LM5106 is a single PWM input gate driver with Enable that offers a programmable dead-time. The dead-time is set with a resistor at the RDT pin and can be adjusted from 100 ns to 600 ns. The wide dead-time programming range provides the flexibility to optimize drive signal timing for a wide range of MOSFETs and applications.

The RDT pin is biased at 3 V and current limited to 1 mA maximum programming current. The time delay generator will accommodate resistor values from 5k to 100k with a dead-time time that is proportional to the RDT resistance. Grounding the RDT pin programs the LM5106 to drive both outputs with minimum dead-time.

Functional Block Diagram



Feature Description

Start-up and UVLO

Both top and bottom drivers include undervoltage lockout (UVLO) protection circuitry which monitors the supply voltage (V_{DD}) and bootstrap capacitor voltage (HB – HS) independently. The UVLO circuit inhibits each driver until sufficient supply voltage is available to turn on the external MOSFETs, and the UVLO hysteresis prevents chattering during supply voltage transitions. When the supply voltage is applied to the V_{DD} pin of the LM5106, the top and bottom gates are held low until V_{DD} exceeds the UVLO threshold, typically about 6.9 V. Any UVLO condition on the bootstrap capacitor will disable only the high-side output (HO).

Device Functional Modes

EN	IN Pin	LO Pin	HO Pin
L	Any	L	L
H	H	L	H
H	L	H	L

Application Information

The LM5106 is one of the latest generation of high-voltage gate drivers which are designed to drive both the high-side and low-side N-channel MOSFETs in a half-bridge/full bridge configuration or in a synchronous buck circuit. The floating high-side driver can operate with supply voltages up to 110 V. This allows for N-channel MOSFET control in half-bridge, full-bridge, push-pull, two switch forward and active clamp topologies.

The outputs of the LM5106 are controlled from a single input. The rising edge of each output can be delayed with a programming resistor.

Table 1. Highlights

FEATURE	BENEFIT
Programmable Turnon Delay	Allows optimization of gate drive timings in bridge topologies
Enable Pin	Reduces operating current when disabled to improved power system standby power
Low Power Consumption	Improves light load efficiency figures of the power stage.

Typical Application

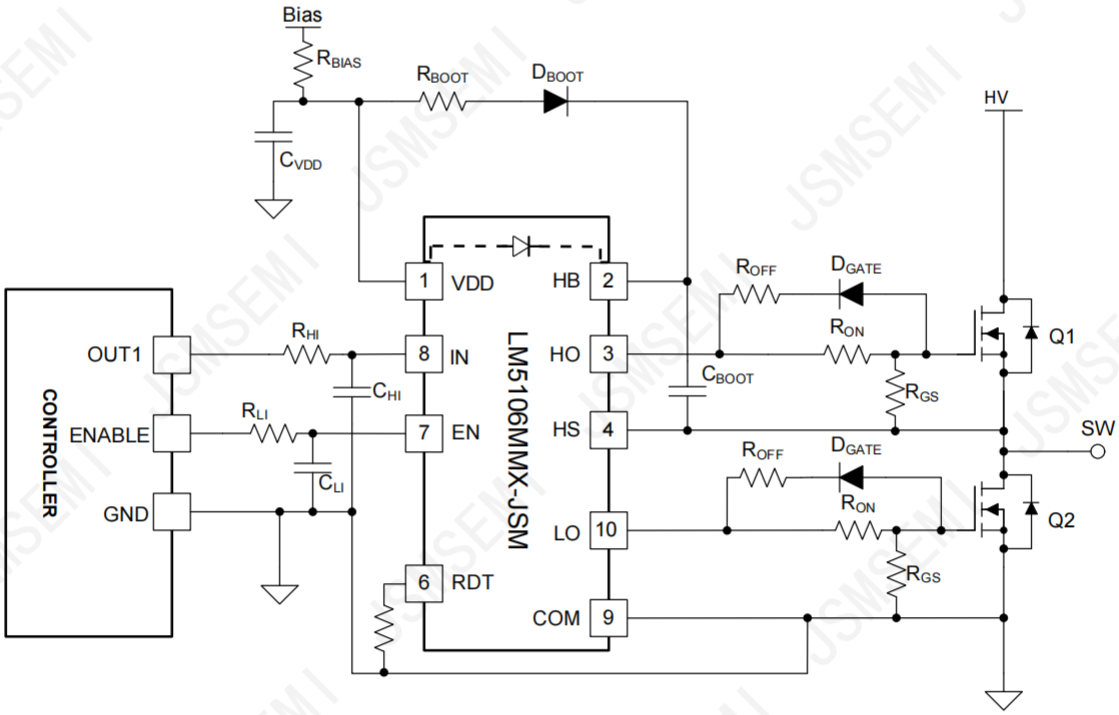


Figure 7. LM5106 Driving MOSFETs Connected in Half-Bridge Configuration

Power Supply Recommendations

Power Dissipation Considerations

The total IC power dissipation is the sum of the gate driver losses and the bootstrap diode losses. The gate driver losses are related to the switching frequency (f), output load capacitance on LO and HO (C_L), and supply voltage (V_{DD}) and can be roughly calculated as:

$$P_{DGATES} = 2 \cdot f \cdot C_L \cdot V_{DD}^2 \quad (1)$$

There are some additional losses in the gate drivers due to the internal CMOS stages used to buffer the LO and HO outputs. At higher frequencies and load capacitance values,the power dissipation is dominated by the power losses driving the output loads and agrees well with the Equation 1.

Layout

Layout Guidelines

The optimum performance of high- and low-side gate drivers cannot be achieved without taking due considerations during circuit board layout. The following points are emphasized:

1. Low ESR / ESL capacitors must be connected close to the IC between VDD and VSS pins and between HB and HS pins to support high peak currents being drawn from VDD and HB during the turnon of the external MOSFETs.
2. To prevent large voltage transients at the drain of the top MOSFET, a low ESR electrolytic capacitor and a good quality ceramic capacitor must be connected between the MOSFET drain and ground (VSS).
3. To avoid large negative transients on the switch node (HS) pin, the parasitic inductances between the source of the top MOSFET and the drain of the bottom MOSFET (synchronous rectifier) must be minimized.
4. Grounding considerations:
   – The first priority in designing grounding connections is to confine the high peak currents that charge and discharge the MOSFET gates to a minimal physical area. This will decrease the loop inductance and minimize noise issues on the gate terminals of the MOSFETs. The gate driver should be placed as close as possible to the MOSFETs.
   – The second consideration is the high current path that includes the bootstrap capacitor, the bootstrap diode, the local ground referenced bypass capacitor, and the low-side MOSFET body diode. The bootstrap capacitor is recharged on a cycle-by-cycle basis through the bootstrap diode from the ground referenced VDD bypass capacitor. The recharging occurs in a short time interval and involves high peak current. Minimizing this loop length and area on the circuit board is important to ensure reliable operation.
5. The resistor on the RDT pin must be placed very close to the IC and separated from the high current paths to avoid noise coupling to the time delay generator which could disrupt timer operation.

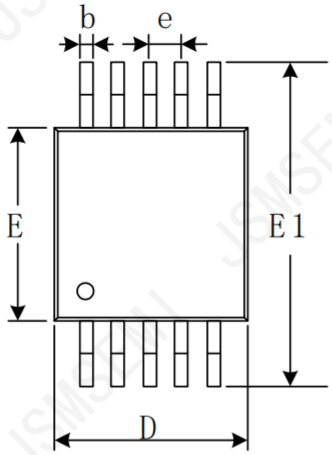
HS Transient Voltages Below Ground

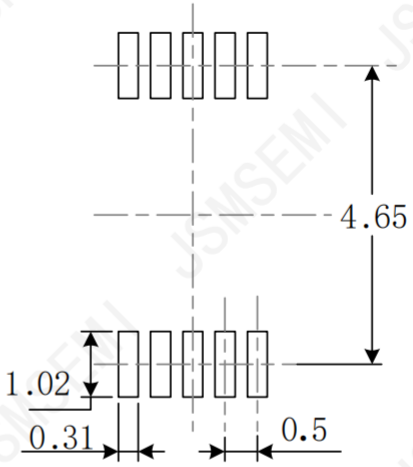
The HS node will always be clamped by the body diode of the lower external FET. In some situations, board resistances and inductances can cause the HS node to transiently swing several volts below ground. The HS node can swing below ground provided:

1. HS must always be at a lower potential than HO. Pulling HO more than –0.3 V below HS can activate parasitic transistors resulting in excessive current flow from the HB supply, possibly resulting in damage to the IC. The same relationship is true with LO and VSS. If necessary, a Schottky diode can be placed externally between HO and HS or LO and GND to protect the IC from this type of transient. The diode must be placed as close to the IC pins as possible in order to be effective.
2. HB to HS operating voltage should be 15 V or less. Hence, if the HS pin transient voltage is –5 V, VDD should be ideally limited to 10V to keep HB to HS below 15 V.
3. Low ESR bypass capacitors from HB to HS and from VCC to VSS are essential for proper operation. The capacitor should be located at the leads of the IC to minimize series inductance. The peak currents from LO and HO can be quite large. Any inductances in series with the bypass capacitor will cause voltage ringing at the leads of the IC which must be avoided for reliable operation.

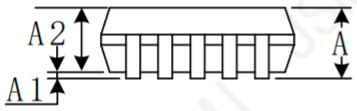
Package Information

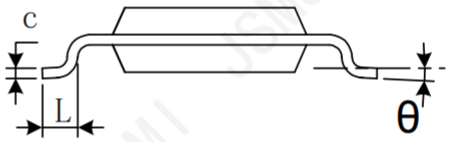
MSOP-10





RECOMMENDED LAND PATTERN (Unit: mm)



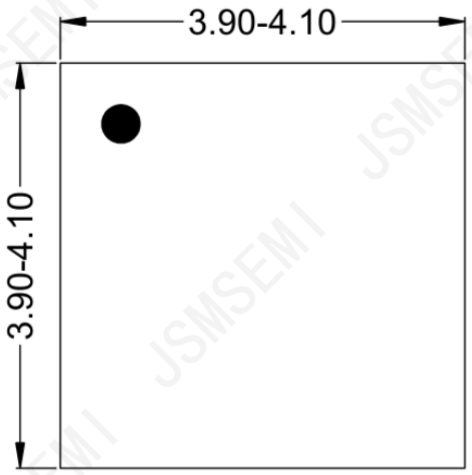


Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	0.820	1.100	0.032	0.043
A1	0.020	0.150	0.001	0.006
A2	0.750	0.950	0.030	0.037
b	0.180	0.280	0.007	0.011
c	0.090	0.230	0.004	0.009
D	2.900	3.100	0.114	0.122
e	0.50(BSC)		0.020(BSC)	
E	2.900	3.100	0.114	0.122
E1	4.750	5.050	0.187	0.199
L	0.400	0.800	0.016	0.031
θ	0°	6°	0°	6°

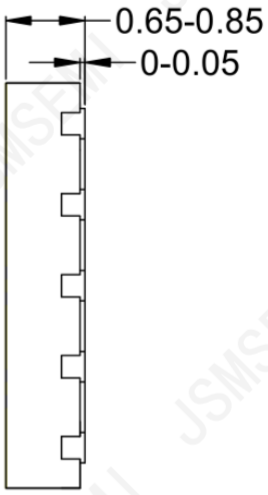
Package Information

PDFN4040-10L

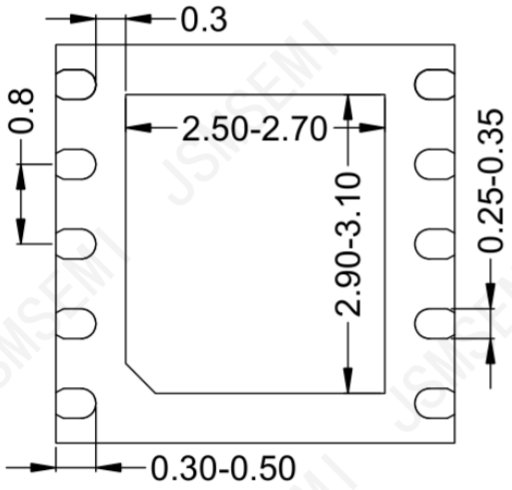
(Unit: mm)



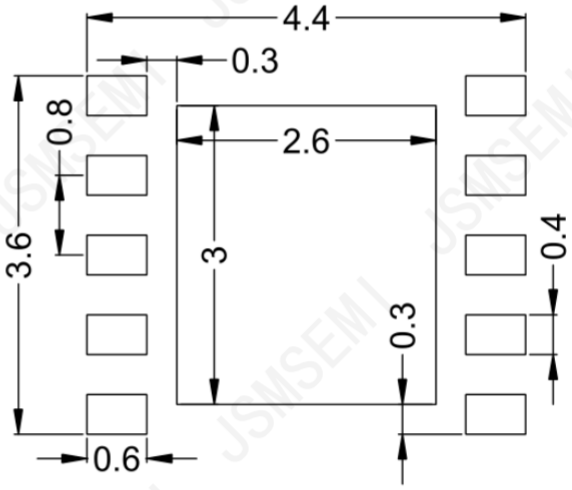
Top View



Side View



Bottom View



Recommended PCB layout
(only for reference)

Revision History

Rev.	Change	Date
V1.0	Initial version	6/27/2021

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